CompuScope 3200 product introduction

CompuScope 3200 is a PCI bus based board-level product that allows the user to capture up to 32 bits of single-ended CMOS/TTL or differential ECL/PECL digital data into on-board memory of up to 2 Gigabytes at clock rates up to 100 MHz.

CS3200 can also be configured, in software, to be 8, 16 or 32 bits wide, thereby allowing the user to maximize the use of acquisition memory for 8 or 16 bit inputs.

Multiple CompuScope 3200 cards can be used in Master/Slave configuration to provide wider input words of up to 256 bits.

INPUT CIRCUITRY
The input stage of the CS3200 consists of 34 high-speed comparators: 32 for data and one each for clock and trigger. The use of high-speed comparators with fully programmable thresholds allows the use of virtually any logic level: 5V TTL/CMOS, 3.3V CMOS, 2.7 V CMOS, ECL, PECL or even custom logic levels.

Inputs need to be driven by a source capable of driving a 50 Ω load. This is necessary in order to maintain good signal integrity.

For CMOS or TTL signal sources not capable of driving 50 Ω loads, a special *CMOS Buffer Board* is available from GaGe, which buffers the data with 50 Ω drivers. The input of the *CMOS Buffer Board* is a 68 pin IDC header for data, a BNC connector for Trigger and another BNC for Clock input. All input signals must be 0 to 3.3 V or 0 to 5V CMOS or TTL signals.

The output of the *CMOS Buffer Board* is a 68 pin MDR connector which connects to the CS3200 using a 6 foot long pleated foil cable, supplied with the CompuScope 3200.

Differential ECL or PECL signals are, by definition, capable of driving a 50 Ω load and interface seamlessly with CompuScope 3200.

CONFIGURABLE INPUT
The output of the on-board comparators is fed into an on-board FPGA, which maximizes the use of on-board memory for data from 8, 16 or 32 bits of width.

The presence of this FPGA also makes it possible to build customized digital acquisition systems, including front-end data processing, for specific requirements. Contact the factory for such custom applications.

Customers must decide at the time of placing an order whether they require a differential ECL/PECL input or single-ended CMOS/TTL input CompuScope 3200. This setting must be configured at the factory and cannot be modified in the field.

ON-BOARD MEMORY
CompuScope 3200 stores digital data in on-board acquisition memory, which is addressable through the PCI bus under software control.

The on-board memory is configured as a circular buffer, so it is possible to store both pre and post trigger data. In other words, it is possible to wait indefinitely for a trigger event and then capture digital data from both before and after this event.

The number of data words that can be captured into on-board memory is a function of the size of the memory and input width. For example, a 16 MB model provides 16 million samples of storage when the input is 8 bits wide. The same model provides 4 million samples of storage with 32 bit word width.

TRANSFERRING DATA TO PC MEMORY
CompuScope 3200 is fully capable of acting as a bus master to DMA captured data into user buffers.

EXTERNAL CLOCK
CompuScope 3200 allows the use of either internal or External Clocks. External Clock can be very useful in systems that require synchronous data capture. These applications include A/D Testing, Telecommunication, DSP Systems, Video, Ultrasonic Imaging etc.

The External Clock is carried on the 68 wire input connector. A high-speed comparator converts the input level of the clock to CMOS/TTL levels used by the on-board data latching and demultiplexing circuitry.

The maximum clock frequency of the input clock is 100 MHz. The driving circuitry on the user's circuit must be capable of driving a 50 Ω load.

CLOCK EDGE SELECTION
The user is allowed to select either the rising or falling edge of the input clock to latch the data.

This flexibility allows the user to apply the CompuScope 3200 in situations in which one of the clock edges and input data do not satisfy the timing requirements. In such cases, using the opposite edge of the clock may resolve the timing conflict.

CLOCK AND DATA TIMING
If the customer operates the CompuScope 3200 with an External Clock, it should be kept in mind that the maximum speed of the input clock is 100 MHz with a rise and fall time of 2.5 ns or less. The minimum clock frequency is zero, i.e. the clocks can be started and stopped at will, once the acquisition has started.

The setup and hold times of the data with respect to the active edge of the clock must satisfy the minimum requirements listed in the specifications.

CRYSTAL BASED TIMEBASE
CompuScope 3200 allows the use of both Internal or External Clock under software control.

When the internal clock is selected, the sampling clock is provided by a crystal controlled oscillator, thereby providing very good short and long term timing accuracy.

When an External Clock is used, the timing accuracy depends entirely on the quality of the External Clock supplied by the user.

INPUT CONNECTOR
The data is input to the CompuScope 3200 over a 68 wire *Pleated Foil* cable. The input connector is a 68-pin MDR socket (P/N 3M 10268-55H3VC). The mating connector is a 3M 10168-6000EC. The mating connector hood is a 3M 10368-A230-00.

Each CompuScope 3200 is supplied with a 6 foot *Pleated Foil* cable featuring the 3M 10168-6000EC connector.

TRIGGER
An External Trigger input is provided on the CompuScope 3200. The configuration of this input is set at the factory as either differential ECL/PECL or single-ended CMOS/TTL.

It is possible to trigger either on the rising or falling edge of this trigger input.

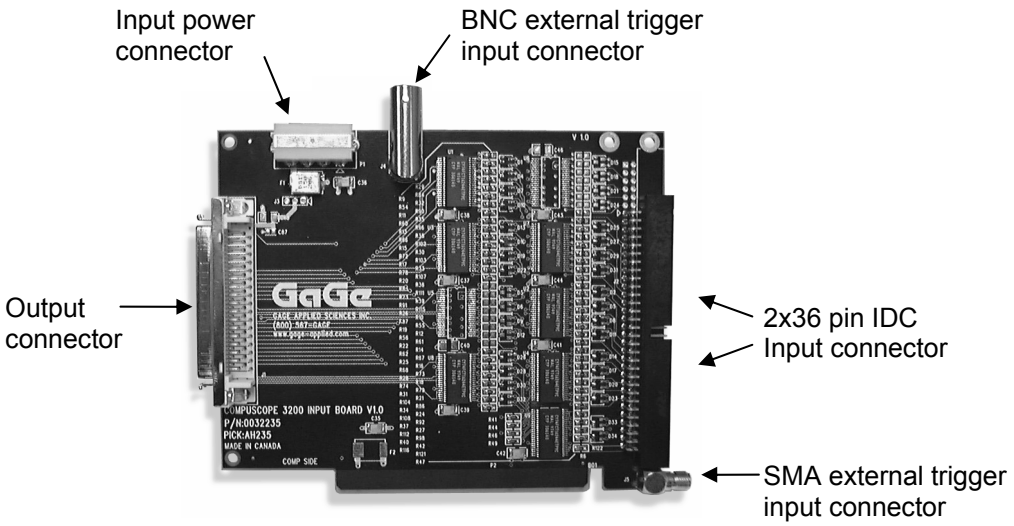
TRIGGER OUTPUT
A Trigger Output signal (5 Volt TTL) is also provided by the CompuScope 3200. This signal is synchronized to the clock that runs the demultiplexed memory counters whose source is either the internal clock of the external clock. As such, there can be a latency of as much as 8 clock cycles between a trigger input and a trigger output.

This Trigger Output can be used to synchronize an entire system to GaGe's internal clock.

BNC BREAKOUT BOARD
One of the popular accessories for CompuScope 3200 is a BNC Breakout Board which connects to the card using the pleated foil cable and allows the user to inject digital data, clock and trigger signals using BNC coaxial connectors. While the Breakout Board is a useful tool for system set-up, it should not be incorporated into final circuit design since the Breakout Board conductor trace lengths and impedances are not adequately controlled for the optimal transmission of high-speed signals.

INPUT BUFFER BOARD

The single-ended CompuScope 3200 card with CMOS/TTL inputs requires digital input signals that are able to drive the 50 Ohm load presented by the CS3200 and mating pleated foil cable. For users whose digital signals are incapable of driving such a load, the CompuScope 3200 Input Buffer Board is available. The Input Buffer board presents a standard high impedance TTL load to the digital inputs and buffers the signals so that they can drive the 50 Ohm load of the CS3200. The output connector of the buffer board mates with the pleated foil cable that is shipped with the CS3200.



Power Connector:

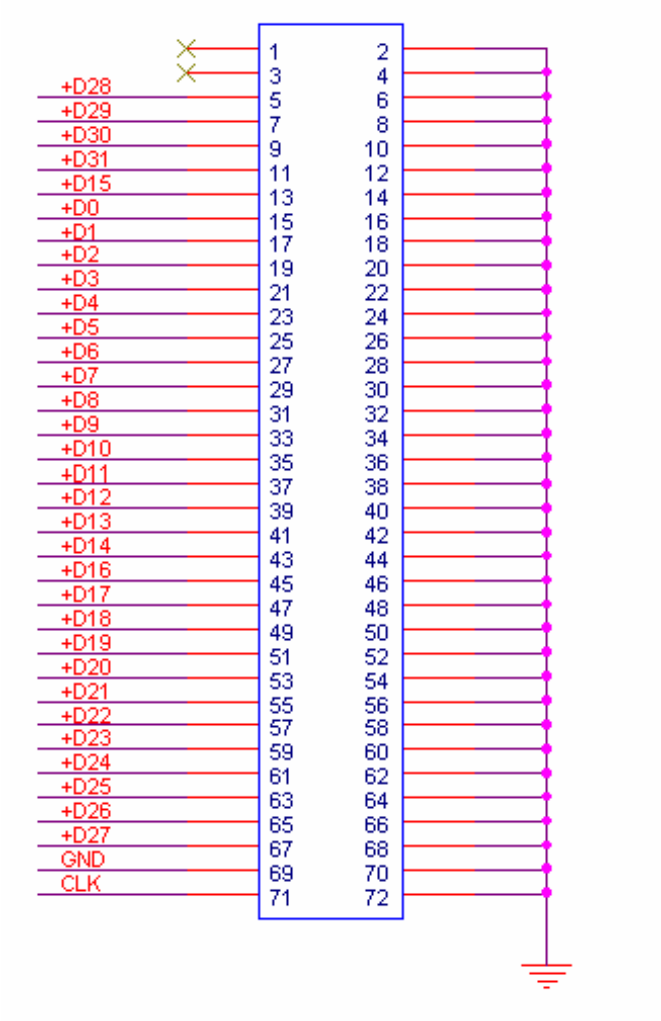
DC power for the buffer board is provided by a standard 4-pin Molex connector from a PC power supply. Connectors of this type are used to power internal PC peripherals such as hard disk drives.

External Trigger Connectors

The external trigger signal for the buffer board (which is passed along to the CS3200) can be introduced to either the BNC or SMA connector on the buffer board. Signals should not simultaneously be introduced to both BNC and SMA external trigger inputs.

Input Connector:

The input for digital signals to the buffer board is a 2x36 pin IDH type receptacle. This receptacle mates with a 2x36 pin IDC type connector. Data inputs to the buffer board must be TTL and the CS3200 must be configured for TTL inputs from software in order for the buffer board/CS3200 combination to operate correctly. Input wires to the buffer board should be kept as short as possible (ideally less than one inch) in order to avoid signal reflections. The pin assignments on the IDH receptacle are shown in the diagram below.


+D28
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+D31
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+D0
+D1
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+D24
+D25
+D26
+D27
GND
CLK
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
21 22
23 24
25 26
27 28
29 30
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CompuScope 3200 connectors and headers

CompuScope 3200 accepts digital data using a connector designed specially for ultra-fast digital signal transmission.

A Trigger Out signal is also available on a BNC connector in order to synchronize CS3200 to the rest of the test system.

The connectors and headers on the CS3200 card are shown below:

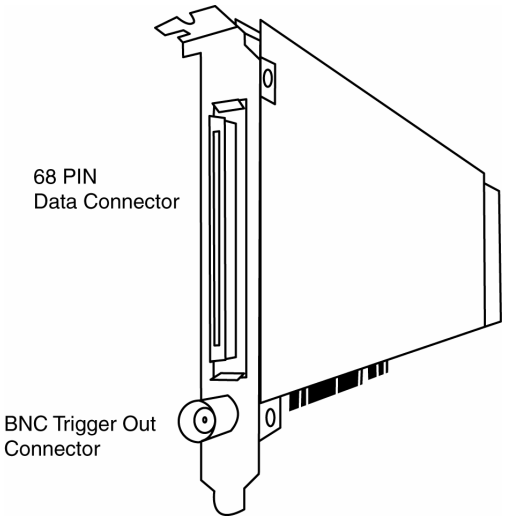

Figure 1a: CS3200 connectors

*Figure 1b: Master/Slave connector**

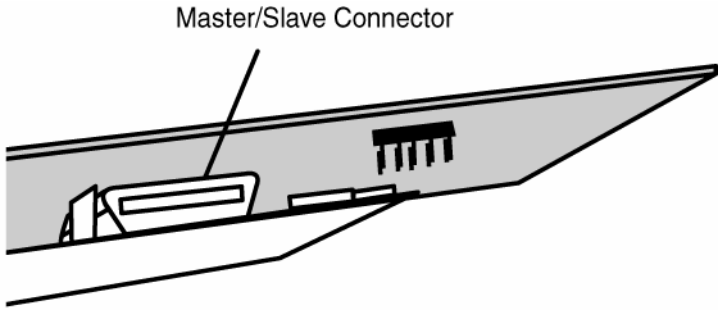

Figure 1: Connectors on CS3200

- **Digital input MDR** connector is used to input up to 32 bits of single-ended or differential digital data lines, one clock input and one trigger input, all with 50 Ω characteristic impedance.

  This connector is designed to provide "equivalent to coax" performance by using copper conductors encapsulated in a specially formulated Teflon to provide the appropriate dielectric constant. This assembly is wrapped in a pleated copper foil, resulting in a 50 Ω transmission line impedance for each of the 68 conductors in the cable.

  For more information on the technology used in this connector, please visit www.mmm.com.

- **Trigger Out BNC** connector is used to output a 0 to 5 Volt, TTL signal which signifies that a trigger event has occurred on the CS3200.

Master/Slave Pinout

The Master/Slave connector on the top-left corner of the card is used to pass all the signals necessary to synchronize the Slave cards with the Master.

Clock Output connector

In some select cases, a user may want to drive the rest of the test system with the internal clock of the CS3200. A Clock Output Upgrade must be purchased in order to have access to this signal.

A small, RF co-axial connector is available on the card, to which a 50 Ω cable can be attached to bring out a 5 Volt CMOS clock signal capable of driving a 50 Ω load.

This upgrade is supplied with a cable that connects to the on-board RF connector on one end and a BNC connector mounted on a card bracket on the other. Note that an extra bracket is required to bring this signal outside the chassis.

- Note that in Master/Slave systems, the Clock Output signal is output from the Master card only.

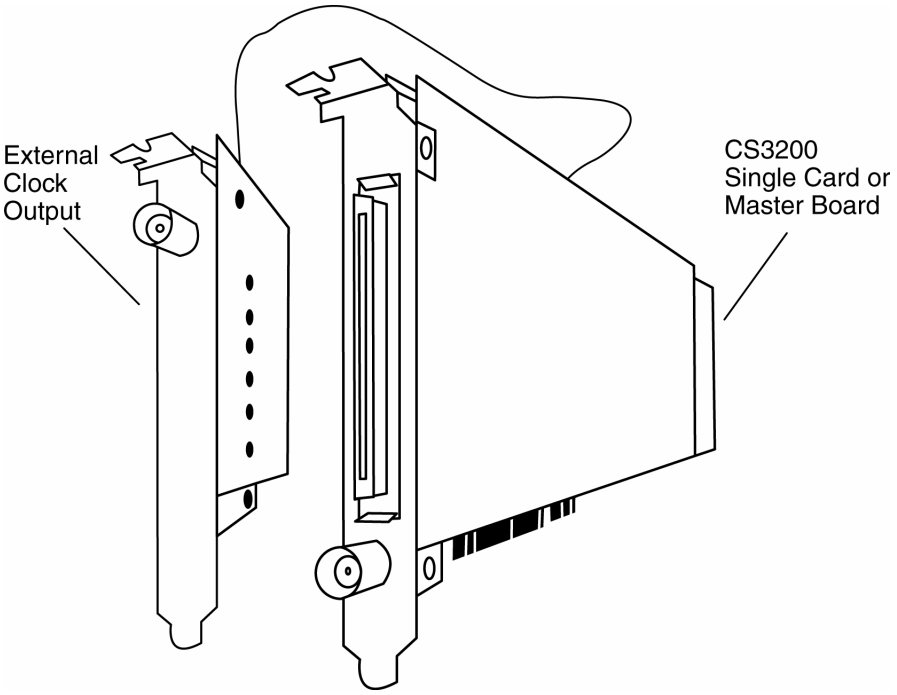

Figure 2: External Clock connector, single-card system or Master card

CompuScope 3200 triggering

Triggering allows the CompuScope 3200 to capture digital data just before or after an external event or a software command. CS3200 supports both pre- and post-trigger data capture.

CompuScope 3200 allows the user to trigger the system on:

- External Trigger
- Software Trigger

The user can also specify whether to trigger on the rising or falling edge of the External Trigger signal.

Trigger Bus for Master/Slave systems

In a Master/Slave system, a trigger signal on the Master card forces all Slave cards to trigger as well.

A CompuScope 3200 Master/Slave system cannot trigger off of the External Trigger input of a Slave card.

CompuScope 3200 digital input

CompuScope 3200 is available with two different input configurations:

- Single-Ended, TTL/CMOS Inputs
- Differential, ECL/PECL Inputs

Users must specify one or the other at the time of placing an order. The two configurations cannot be changed via software commands and require considerable changes to the input circuitry. As such, this change cannot be made in the field and must be done at the factory.

Pin layout on CS3200 connector – Single-ended, TTL/CMOS inputs

CS3200 connector pin layout (Single-ended, TTL/CMOS inputs)			
1	CLK	35	GND
2	D0	36	GND
3	D1	37	GND
4	D2	38	GND
5	D3	39	GND
6	D4	40	GND
7	D5	41	GND
8	D6	42	GND
9	D7	43	GND
10	D8	44	GND
11	D9	45	GND
12	D10	46	GND
13	D11	47	GND
14	D12	48	GND
15	D13	49	GND
16	D14	50	GND
17	D15	51	GND
18	D16	52	GND
19	D17	53	GND
20	D18	54	GND
21	D19	55	GND
22	D20	56	GND
23	D21	57	GND
24	D22	58	GND
25	D23	59	GND
26	D24	60	GND
27	D25	61	GND
28	D26	62	GND
29	D27	63	GND
30	D28	64	GND
31	D29	65	GND
32	D30	66	GND
33	D31	67	GND
34	TRIG IN	68	GND

Pin layout on CS3200 connector – Differential, ECL/PECL inputs

CS3200 connector pin layout (Differential, ECL/PECL inputs)			
1	CLK+	35	CLK-
2	D0+	36	D0-
3	D1+	37	D1-
4	D2+	38	D2-
5	D3+	39	D3-
6	D4+	40	D4-
7	D5+	41	D5-
8	D6+	42	D6-
9	D7+	43	D7-
10	D8+	44	D8-
11	D9+	45	D9-
12	D10+	46	D10-
13	D11+	47	D11-
14	D12+	48	D12-
15	D13+	49	D13-
16	D14+	50	D14-
17	D15+	51	D15-
18	D16+	52	D16-
19	D17+	53	D17-
20	D18+	54	D18-
21	D19+	55	D19-
22	D20+	56	D20-
23	D21+	57	D21-
24	D22+	58	D22-
25	D23+	59	D23-
26	D24+	60	D24-
27	D25+	61	D25-
28	D26+	62	D26-
29	D27+	63	D27-
30	D28+	64	D28-
31	D29+	65	D29-
32	D30+	66	D30-
33	D31+	67	D31-
34	TRIG IN+	68	TRIG IN-

Input comparators

The input stage for all inputs of the CS3200 is an EMI filter followed by a 50 Ω terminating resistor network wide bandwidth analog comparator.

For single-ended input models, one of the inputs to the comparator is the input signal and the other is a programmable voltage level generated by an on-board DAC (Digital to Analog Converter). This enables the input stage to handle different voltage level CMOS signals, e.g. 3.3 Volt, 5 Volt etc.

For differential input models, both inputs of the comparator are fed by the two differential signals corresponding to a particular input. For example, D0+ and D0- are fed into the inputs of the same comparator.

Front-end FPGA

At the heart of the CS3200 is a high-speed FPGA: all data lines, trigger and clock signals received from the outside world are injected into it; all data demultiplexing is done inside it; all acquisition control state machines exist in it; all sampling clock selection circuitry resides in it; all triggering is done within it; and all Master/Slave controls are handled inside it.

This design allows for tremendous flexibility in adapting the CS3200 for a number of customized applications that require not only fast digital data acquisition, but also some data manipulation. Contact the factory with your custom requirement.

This FPGA also allows the CS3200 to work in one of three input word widths of 32, 16 or 8 bits by demultiplexing (DMUX) the data.

CompuScope 3200 compliance statement

Category	Standards or description
EC Declaration of Conformity – EMC	Meets intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities: EN 61326 EMC requirements for Class A electrical equipment for measurement, control and laboratory use. [1, 2, 3] IEC61000-4-2 Electrostatic Discharge (Performance criterion B) IEC61000-4-3 RF Electromagnetic Field (Performance criterion A) IEC61000-4-4 Electrical Fast Transient/Burst Immunity (Performance criterion B) IEC61000-4-5 Power Line Surge Immunity (Performance criterion B) IEC61000-4-6 Conducted RF Immunity (Performance criterion A) IEC61000-4-11 Voltage Dips and Interruptions Immunity (Performance criterion B) EN 61000-3-2 AC Power Line Harmonic Emissions
Australia / New Zealand Declaration of Conformity - EMC	Complies with EMC provision of Radio communications Act per the following standard(s): AS/NZS 2064.1/2 Industrial, Scientific and Medical Equipment: 1992 [1, 2, 3]

1. **High-quality shielded cables must be used to ensure compliance to the above listed standards**
2. **Compliance demonstrated on a single card configuration**
3. **On the host PC used by the customer, all unused back panel slots must be covered with EMI blocking plates**