Advanced timing features on CompuScope digitizers

CompuScope digitizers are available with a variety of advanced timing features, which may be standard or optional, depending on the CompuScope model. Advanced timing features are generally used to provide improved synchronization between the acquired signals, CompuScope triggering and ADC clocking. Advanced timing features are described in detail below and include: External Clocking, Trigger Out, Clock Out and 10 MHz reference clocking.

CompuScope External Clocking

External Clocking functionality is a very powerful feature in a digitizer and is available on all CompuScope models. External Clocking functionality allows the user to synchronize the digitizer to an external clocking signal that may have been already synchronized to an external system. Within CompuScope digitizers, input external clocking signals are routed almost directly to CompuScope ADC chips so that each clock edge causes the ADC chips to produce exactly one sample. No re-clocking or Phase Lock Loop circuitry is used in CompuScope external clocking circuitry, since these methods may lead to extra or missing ADC clocks.

Below is a table of available External Clock options for the various CompuScope digitizer models.

	External Clock Input
Cobra CompuScope	Standard
CompuScope 82G	Optional
CompuScope 8500	Optional
CompuScope 12400	Standard
CompuScope 12100	Optional (X1 External Clocking available)
CompuScope 1220	Standard
CompuScope 14200	Standard
CompuScope 14105	Standard
CompuScope 14100	Standard
CompuScope 1610	Standard
CompuScope 1602	Optional
Octopus CompuScopes	Standard

A good example of a system requiring external clocking is an imaging system that produces a stream of analog voltages, which correspond to light intensities, together with an accompanying “pixel clock” signal, whose rising edge indicates when the light intensity signal must be sampled. Such a light intensity signal must be sampled using the pixel clock, since any other clock source will drift over time and become out of phase with the pixel clock. By connecting the pixel clock to the external clock input of a CompuScope card, perhaps through a conditioning amplifier, the user can sample the imaging signal with the pixel clock, as required.

The imaging system is a good example of the general case where the user has a reference clocking signal that is synchronous with the signal to be acquired. When using a clocking source, such as the CompuScopes internal sampling oscillator, that is asynchronous (unrelated) to the signal trigger, a one-point jitter always occurs from one acquisition to the next. This one-point jitter is a fundamental consequence of an asynchronous signal trigger and ADC clock. By using a synchronous clocking signal as an external clocking source for a CompuScope, however, this one-point jitter may be overcome and the user may achieve the best possible trigger stability that is limited only by the stability of the electrical components on the CompuScope hardware. This intrinsic jitter is typically ¼ of a data point or better.

In using CompuScope hardware, the user must provide an external clocking signal with the appropriate characteristics. First of all, all CompuScope models (except the CS3200 digital input card) have a minimum and maximum external clocking frequency that must be respected. The minimum value directly indicates that the external clocking signal may not be turned off during an acquisition, since this corresponds to a disallowed 0 Hz external clocking frequency. Secondly, the user must provide an external clocking signal with sufficient

electrical drive. Most CompuScope digitizers terminate the external clock input with a 50 Ohm load in order to inhibit high-frequency signal reflections. The user's clocking signal must, therefore, be capable of driving a 50 Ohm load for most CompuScope digitizers. The user must ensure that the external clocking signal has a duty cycle that is within specification. Finally, the user must ensure that the external clock signal amplitude is within the specified limits. A clocking signal with an amplitude that is too high or too low may lead to incorrect operation.

For convenience a table is given on the next page that lists the input characteristics of the external clock input for each CompuScope digitizer.

Most CompuScope digitizers sample the input signal upon each rising edge of the input external clocking signal. In this case, the sampling frequency is equal to the external clocking frequency.

Figure 1 and Figure 2 below illustrate sampling on the majority of CompuScope digitizers in Single or Dual channel mode. As discussed, a new ADC sample is taken upon every rising edge of the External Clocking signal. For simplicity, a square wave clocking signal is illustrated. For CompuScope digitizers that specify sinusoidal clock signal inputs, the rising edge is the zero-crossing point of the sine wave with a positive slope. Generally, the specified shape of the external clocking signal (square or sinusoidal) is not important. If a shape different than the specified one is used, then the specified external clocking signal levels must be appropriately translated.

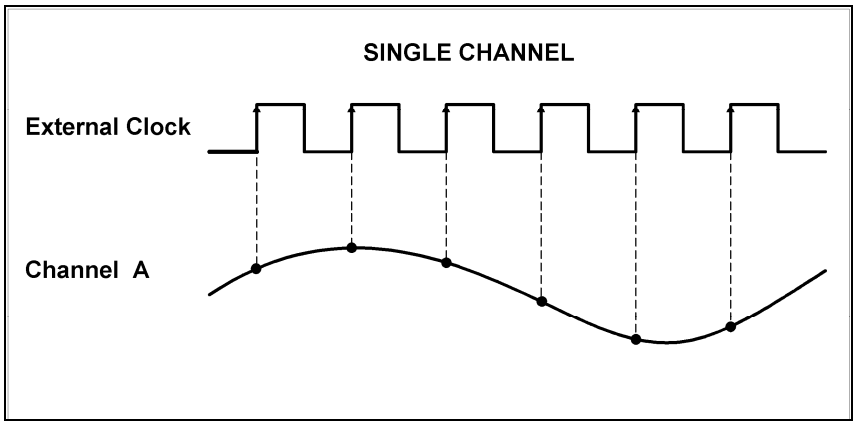

Figure 1: CompuScope External Clocking in Single Channel mode

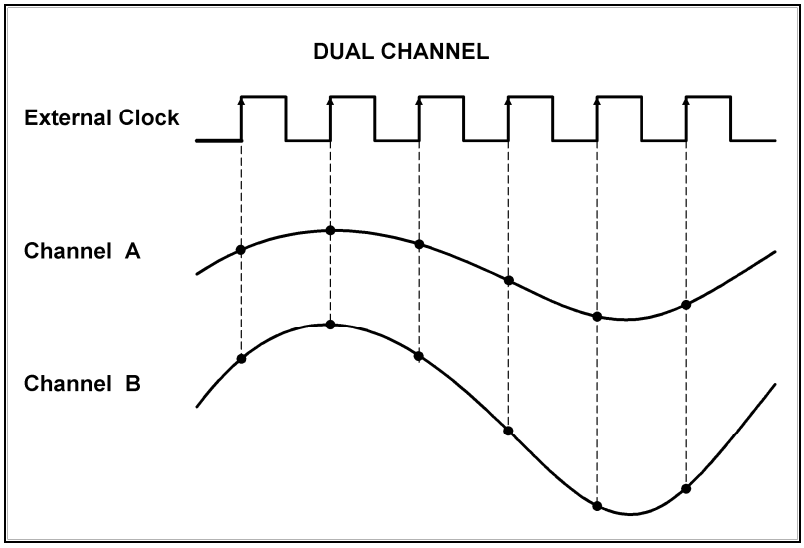

Figure 2: CompuScope External Clocking in Dual Channel mode

Some CompuScope digitizers sample at a frequency other than the frequency of the input external clocking signal. These exceptions are discussed below.

The first exception is the CS82G. In Dual Channel mode, the CS82G samples on every rising edge of the external clocking signal, as illustrated in Figure 2. In Single Channel mode, however, the CS82G will sample on both rising and falling edges of the external clocking signal, as illustrated in Figure 3. In this case, therefore, the sampling frequency is equal to twice the frequency of the external clocking signal. For instance, in order to obtain a sampling frequency of 2 GS/s in Single Channel mode on the CS82G, a 1 GHz external clocking frequency must be used.

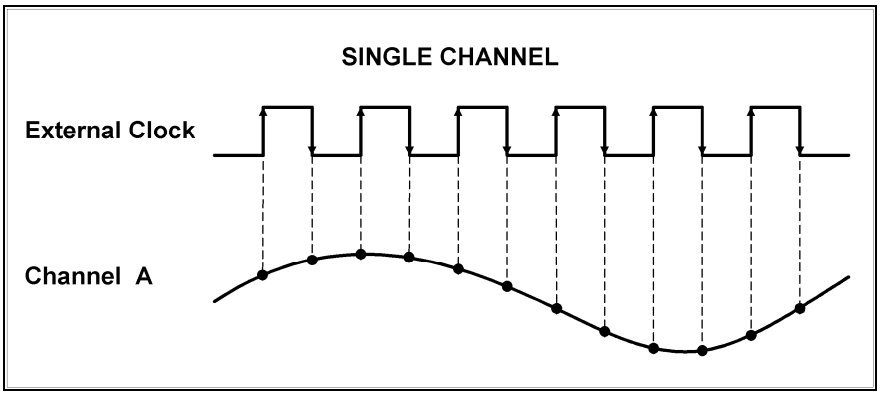

Figure 3: Single Channel Mode External Clocking on the CompuScope 82G

The other external clocking exceptions occur in Dual Channel mode only for CompuScope models, CS12100, CS1602 and CS1610. For these models in Dual Channel mode, sampling does not occur on every rising edge of the external clocking signal so that the sampling rate is less than the external clocking signal frequency. Figure 4 illustrates external clocking on the CS12100 and CS1610 in Dual Channel mode. As illustrated, ADC samples are acquired on every other rising edge of the external clocking signal so that the sampling frequency is one-half of the external clock signal frequency. For these models in Dual Channel mode, therefore, an external clocking frequency of 10 MHz will cause the CompuScopes to sample at 5 MS/s. For the CS1602, the sampling frequency to external clocking frequency ratio is 8. For instance, if a 20 MHz external clocking is used, the CS1602 will sample at its maximum rate of 2.5 MS/s.

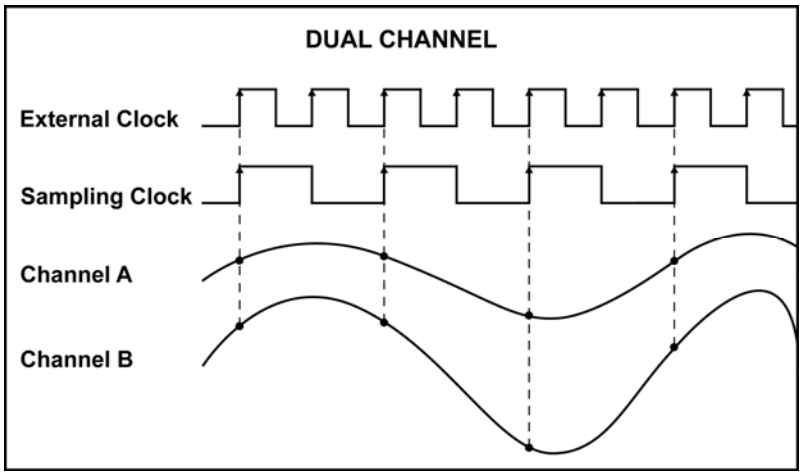

Figure 4: Dual Channel Mode External Clocking on the CS12100 and CS1610

A special external clocking option is available for the CS12100 called the *X1 External Clock upgrade*. This option allows the CS12100 to sample on every rising edge of the external clocking signal in Dual Channel mode, as illustrated in Figure 5. With this option, therefore, the sampling frequency is equal to the external

clocking frequency in Dual Channel mode. With the X1 External Clock upgrade, however, the CS12100 is unable to acquire in Single Channel acquisition mode – even with internal clocking.

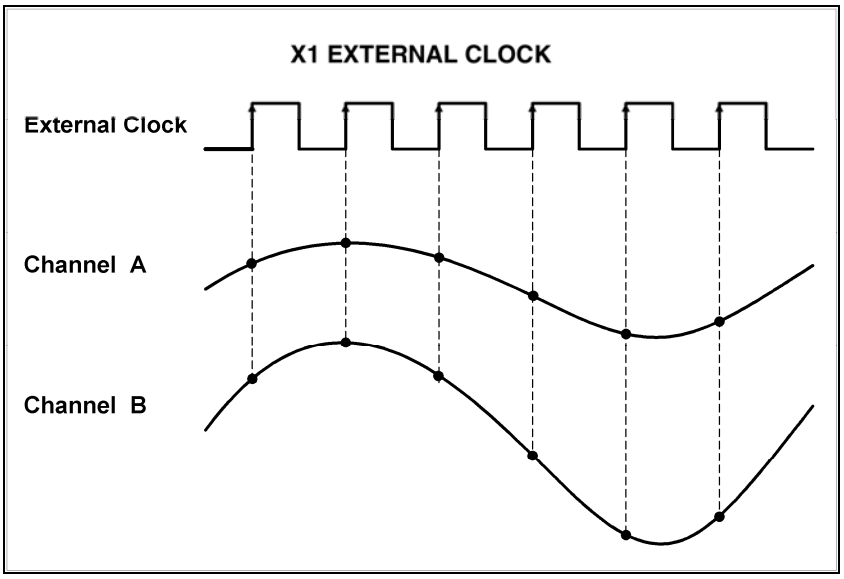

Figure 5: X1 External Clock upgrade for the CS12100 in Dual Channel mode

	Signal level	Termination Impedance	Sampling edge	Coupling	External Clock frequency range	Duty cycle
Octopus CompuScope	MIN. 1 V RMS MAX. 2 V RMS	50 Ω	Rising	AC	1 MHz to maximum product sample rate	50% ± 5%
Cobra CompuScope	Minimum 200 mV RMS Maximum 500 mV RMS	50 Ω	Dual: Rising Only Single: Rising < 1 GS/s; Rising and falling > 1 GS/s	AC	200 MHz to 1 GHz	50% ± 5%
CS82G	MIN. 225 mV RMS MAX. 500 mV RMS	50 Ω	Dual: Rising only Single: Rising & Falling	AC	10 MHz to 1 GHz	Single/Dual: 50% ± 5 %
CS8500	500 mV RMS sine wave	50 Ω	Rising	AC	200 MHz to 500 MHz	50% ±30%
CS12400	MIN. 1 V RMS MAX. 2 V RMS	50 Ω	Rising	AC	Single/Dual: 40 MHz to 420 MHz	50% ± 5%
CS12100	0 to +5 Volt TTL	50 Ω	Rising	DC	ExtClk: 10 MHz to 100 MHz X1 ExtClk: 5 MHz to 50 MHz	ExtClk: 50% ±30% X1 ExtClk: 50% ±5%
CS1220	TTL	50 Ω	Rising	DC	1 kHz to 20 MHz	50% ±5%, -0% at 20 MHz
CS14200	MIN. 1 V RMS MAX. 2 V RMS	50 Ω	Rising	AC	Single/Dual: 1 MHz to 200 MHz	50% ± 5%
CS14105	MIN. 1 V RMS MAX. 2 V RMS	50 Ω	Rising	AC	Single/Dual: 30 MHz to 105 MHz	50% ± 5%
CS14100	MIN. 1 V RMS MAX. 2 V RMS	50 Ω	Rising	AC	Single: 40 MHz to 100 MHz Dual: 20 MHz to 50 MHz	Single: 50% ± 30% Dual: 50% ± 5%
CS1610	TTL	50 Ω	Rising	DC	2 kHz to 20 MHz, maximum using 2x decimation filter	50% ±5%, -0% at 20 MHz
CS1602	TTL	50 Ω	Rising	DC	8 kHz to 20 MHz, maximum using 8x decimation filter	50% ±5%, -0% at 20 MHz

10 MHz Reference Clocking

Please note: this feature is not available on the CS82G, CS8500, CS12100, CS1220, CS14100, CS1610 or CS1602

When internally clocking, GaGe CompuScope ADCs use a clocking source that is derived from a highly stable crystal oscillator, whose accuracy is typically 100 parts-per-million or better. This sampling rate accuracy is more than sufficient for most digitizer applications. In some digitizer applications, notably communications applications, however, higher ADC clocking accuracy and stability are required. For these requirements, GaGe can provide 10 MHz reference clocking on the Cobra, CS14200, CS14105, CS12400, and the Octopus family of multi-channel digitizers.

10 MHz reference clocking allows users to synchronize CompuScope on-board crystals with a standard external 10 MHz reference source. Such sources are now available on low-cost IRIG devices, which receive high-accuracy 10 MHz signals derived from atomic clock sources on orbiting GPS satellites. 10 MHz IRIG devices may be accurate to of order 1 part-per-billion.

The CompuScope 10 MHz reference circuitry employs Voltage Controlled Crystal Oscillators (VCXOs) within Phase Lock Loop (PLL) circuitry. This circuitry ensures that the frequency of the VCXO is reset every 100 nanoseconds so that the relative accuracy and stability of the sampling rate is equal to that of the 10 MHz reference input.

For internal sampling, Octopus CompuScope models actually employ VCXO/PLL circuitry that is driven by an on-board 10 MHz reference standard that has an accuracy of order 1 part-per-million, which is achieved through temperature compensation. While this internal 10 MHz reference frequency is not as accurate as an IRIG 10 MHz source, it far exceeds the accuracy of a fixed crystal oscillator without temperature compensation.

Trigger Out

Please note: this feature is not available on the CS1220

A CompuScope Trigger Out connector provides an output TTL pulse whenever a trigger event occurs on a CompuScope system. Its main usage is as a source for the synchronous external triggering of other devices. Usage of the Trigger Out signal allows synchronous sampling without the need for synchronous external clock and trigger sources.

The primary use case involves using the CompuScope as the master trigger source by forcing a trigger event on the CompuScope from software. In this case, the CompuScope is forcibly triggered from software, which creates a synchronous output TTL pulse that externally triggers another device. Signals provided by this device are then captured on the CompuScope system.

Using Trigger Out triggering from a CompuScope system provides three advantages over externally triggering the CompuScope system. First, the Trigger Out pulse is synchronous with the CompuScope internal sampling clock. This means that the rising edge of the Trigger Out pulse has a fixed phase relationship with the CompuScope internal sampling clock. As a result, signals that are triggered by the Trigger Out pulse are also synchronous with the CompuScope internal sampling clock. Repetitive waveforms, therefore, do not suffer the usual one-point jitter that always arises due to asynchronous clocking and triggering.

The second advantage of using the Trigger Out signal as a trigger source is the impossibility of missing triggers because all triggers are generated by the CompuScope itself. By contrast, if the CompuScope is externally triggered from a separate device, the possibility of trigger loss exists if the CompuScope is unable to process the previous external trigger quickly enough. Since the CompuScope generates the Trigger Out pulses itself only when it is ready to do so, triggers cannot be missed. The final advantage of using Trigger Out is that the repetitive trigger frequency may be maximized. With a slow external trigger source, the CompuScope may have to wait around for the next external trigger pulse to occur. By using the Trigger Out source, however, the CompuScope may initiate the next trigger event as quickly as possible, as soon as it has finished processing the last trigger event.

On most CompuScope models, the Trigger Out pulse is qualified, which means that the pulse only occurs once for each waveform acquired by the CompuScope hardware. On the CS14200, 14105 and 12400, however The Trigger Out pulse is unqualified. This means, for instance, that if the trigger source is Channel 1 and if the signal connected to Channel 1 is a 1 MHz sine wave, the Trigger Out pulse will occur at a 1 MHz rate, and may

occur multiple times per waveform acquisition. An unqualified Trigger Out signal does not present a problem for the primary use case of forced triggering discussed above. In the case of internal or external triggering, however, the user must think carefully about how to manage the unqualified Trigger Out signal.

Clock Out

Please note: this feature is not available on the CS82G, CS8500, CS12100, CS1220, CS14100, CS1610 or CS1602

Some CompuScope digitizers provide a Clock Out signal that may be used as an external clocking signal for other devices, such as a GaGe CompuGen card. The frequency of the Clock Out signal is exactly equal to the ADC sampling rate, in all sampling modes. The only exceptions are the Cobra, CS12400 , and CS14200. When the Cobra is sampling above 1 GS/s, or the CS12400 is sampling above 200 MS/s, or the CS14200 is sampling above 100 MS/s, the Clock Out frequency is one half of the sampling rate. The Clock Out signal provides a convenient source of a common clock signal for multiple devices so that it is not necessary for the user to provide a separate external clocking signal.