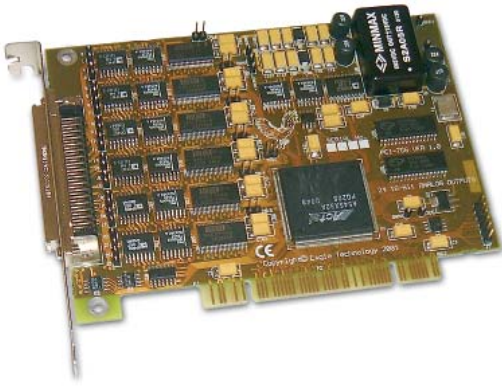


Extra Low Noise | High Accuracy



DESCRIPTION

The **PCI-766** is an advanced multi-channel analog output board with optimized 8, 16 or 24 channels with full 16-bit resolution.

Up to 24 channels of analog output can be streamed at a maximum speed of 100KHz. The PCI-766 has 2 different operation modes, FIFO and loop mode. FIFO is used to stream data from software to hardware. Loop mode continuously streams data saved in the board's hardware buffer.

Other features include 6 digital inputs which can be used as digital inputs or clock and trigger source.

FEATURES

- 8/16/24 Analog output channels ($\pm 10V$)
- Maximum update rate of 100kHz per channel
- On card 128K x16 FIFO for channel list configuration
- Channels programmable to operate under programmed I/O or channel list mode
- Under channel list mode number of channels configured between 4/8/12/16/20/24
- Channel list timing can be synchronized to an external clock or to an internal 16-bit programmable counter
- 6x Over-voltage protected digital inputs are provided (can be programmed as digital inputs or counter/timer functions)
- 2x 16-bit 82C54 compatible counter/timers
- Windows98/ME/2000/XP OS Support (NT on request)
- WaveView for Windows Data Acquisition & Logging Software
- Labview, Testpoint and VEE Pro Drivers
- Modules are 3.3V or +5V PCI slot compatible

SCSI DSub 68M

| | | | |
|-------------|----|----|-----------|
| AGND | 35 | 1 | AGND |
| AOCH0 | 36 | 2 | AREF0 |
| AOCH1 | 37 | 3 | AREF1 |
| AOCH2 | 38 | 4 | AREF2 |
| AOCH3 | 39 | 5 | AREF3 |
| AGND | 40 | 6 | AGND |
| AOCH4 | 41 | 7 | AREF4 |
| AOCH5 | 42 | 8 | AREF5 |
| AOCH6 | 43 | 9 | AREF6 |
| AOCH7 | 44 | 10 | AREF7 |
| AGND | 45 | 11 | AGND |
| AOCH8 | 46 | 12 | AREF8 |
| AOCH9 | 47 | 13 | AREF9 |
| AOCH10 | 48 | 14 | AREF10 |
| AOCH11 | 49 | 15 | AREF11 |
| AGND | 50 | 16 | AGND |
| AOCH12 | 51 | 17 | AREF12 |
| AOCH13 | 52 | 18 | AREF13 |
| AOCH14 | 53 | 19 | AREF14 |
| AOCH15 | 54 | 20 | AREF15 |
| AGND | 55 | 21 | AGND |
| AOCH16 | 56 | 22 | AREF16 |
| AOCH17 | 57 | 23 | AREF17 |
| AOCH18 | 58 | 24 | AREF18 |
| AOCH19 | 59 | 25 | AREF19 |
| AGND | 60 | 26 | AGND |
| AOCH20 | 61 | 27 | AREF20 |
| AOCH21 | 62 | 28 | AREF21 |
| AOCH22 | 63 | 29 | AREF22 |
| AOCH23 | 64 | 30 | AREF23 |
| DI5 | 65 | 31 | DI4 |
| DI3 | 66 | 32 | DI2 |
| DI1/EXT_CLK | 67 | 33 | DI0 |
| DGND | 68 | 34 | +5V_FUSED |

Specifications

ANALOG outputs

| | |
|--|--|
| Operating Modes | |
| Programmed I/O: | Host writes data directly to DAC channel |
| FIFO output using timer source: | Data is cycled out of FIFO using timer |
| FIFO output using external timer input (one of the digital input channels) | |

Conversion Characteristics

| | |
|--------------------------------|--|
| Resolution: | 16-bit |
| Full Scale Error (Calibrated): | .005% Full scale |
| Maximum update rate: | 100 kHz to 0.035% full scale; 50 kHz to 0.025% |
| FIFO Buffer Size: | 64K x 16 and Pattern Length (Programmable) |
| Data Transfer: | Triggered interrupts, DMA or programmed IO |
| Update Mode: | In channel list mode, channels are synchronously updated |

Voltage Output Characteristics

| | |
|-----------------------|--|
| Range: | $\pm 10 V$ |
| Output Settling Time: | 10 μ S to 0.03% Full scale |
| Accuracy: | ± 3 LSB (Including Gain and offset errors) |
| Noise: | ± 2 LSB |
| Output Coupling: | DC |
| Output Impedance: | 0.2 Ohm |
| Output Drive: | ± 5 mA |
| Power-on state: | 0V |

DIGITAL INPUTS

| | |
|---------------------------------------|--|
| No. of Digital Inputs: | 6 |
| Min input voltage (logic '1'): | +2.5 V (Relative to DGND) |
| Max input voltage (logic '0'): | +1.0 V (Relative to DGND) |
| Max Continuous Input Voltage: | ± 32 V (Relative to DGND) |
| Max Input Voltage Spike < 100 ms: | ± 80 V (Relative to DGND) |
| Max Timer Input Frequency: | 100 kHz (Used as a sync DAC clock) |
| Max Timer Input Frequency: | 8 MHz (Used as a counter/timer clock source) |
| Min Positive Pulse Width: | 120ns |
| Min Low time between positive pulses: | 120ns |

TIMERS

| | |
|--------------|---|
| Number: | 2x 82C54 compatible (16 bits wide) 1x programmable divider |
| Timer Clock: | 20 MHz internal or external input via the programmable I/O |

EXTERNAL

| | |
|-------------|------------------|
| Dimensions: | 143 mm x 98,5 mm |
|-------------|------------------|

Optional Accessories: PCI-703-16/16A

| | |
|--------------|--|
| ADPT-6868SCD | SCSI-II 68 (F) Centronics & SCSI-II 68 (F) DSub to 69way Screw Terminal Adaptor |
| SCSI-D68M/F | 68-way SCSI-II D-Sub(M) to (F) multi-core screened cable (1m length) |

Ordering Information

Supplied with EDR Enhanced Software Development Kit

| | |
|------------|---------------------------------------|
| PCI-766-8 | 8 Channel 16-bit Analog Output Board |
| PCI-766-16 | 16 Channel 16-bit Analog Output Board |
| PCI-766-24 | 24 Channel 16-bit Analog Output Board |

Optional Accessories Diagram

