

**User manual for**

**PC-81**

**Low Cost Analog Input Expander Card**

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# Preface

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This manual is written for users of the PC-81 analog input expander cards. It provides all information necessary to successfully program and operate this card. As the card is designed for use with almost any existing analog input card, detailed instructions for your particular system cannot be given.

This manual assumes :

- That you have a basic knowledge of electronic circuitry and measurement techniques.
- That you are familiar with the host PC and analog input card which you are using.
- That you are capable of writing your own programs.

The manual contains the following sections.

Chapter 1 - Introduction.

- Chapter 1 contains an overview of the PC-81 card, and its capabilities.

Chapter 2 - Architecture and Configuration.

- Chapter 2 discusses the basic operation and internal structure, as well as the configuration, of the PC-81 for various operating requirements.

Chapter 3 - Interconnection.

- Chapter 3 describes the connection of the PC-81 card to the host computer/analog input card and to user inputs.

Chapter 4 - Software.

- Chapter 4 discusses considerations for the software which is to control the PC-81.

Appendix A - Hardware Specifications.

- Appendix A provides complete electrical specifications for the PC-81.

Appendix B - Error Analysis.

- **Appendix B contains information which will allow you to calculate the effect of multiple PC-81's on the accuracy of your measurements.**

# CHAPTER 1

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## Introduction

The PC-81 is a analog input expander. The board has been designed to allow extra analog input channels to be added to virtually any analog input card. In order to operate, it requires the following :

- The existing analog input card must have at least two differential, or four single ended analog inputs.
- There must be at least four digital output lines available. Note that these digital output lines need not be a part of the analog input card, but can be from any other card (or, if desired, from a mechanical switch!). Users of PC/XT/AT machines can easily use a low cost PC-36 parallel interface card if their analog input cards do not have digital outputs available.
- A power supply must be available. This must have voltages of  $+ -12$  to  $+ -15$  V available. These power supply voltages may be obtained from the host analog input card.

### 1.1. Capabilities

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Each PC-81 provides the following capabilities :

- Input channels : 64 single ended, or 32 differential.
- Input voltage range : The input voltage must at all times be less than 3 Volts below the power supply voltages for accurate measurements. All inputs are protected against overvoltage.
- Decoding logic : Each PC-81 contains an eight bit DIP switch and eight select inputs. If the code on these inputs does not match that set on the DIP switch, then all four outputs of the PC-81 are electronically disconnected. This is used to allow many PC-81's to be connected in parallel.

## **1.2. Total number of channels.**

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The total number of PC-81's, and hence the total number of channels possible is dependant on several factors, principally the interconnection scheme. PC-81's can be interconnected to your host card in a multitude of fashions. There are however, two major techniques :

### **1.2.1. Parallel interconnection.**

This technique allows the maximum possible number of channels with the lowest possible number of PC-81's. For every four single ended or two differential inputs on the host card, you can have :

- 64 single ended or 32 differential inputs with 4 digital output lines and 1 PC-81.
- 1024 single ended or 512 differential inputs with 8 digital output lines and 16 PC-81's.
- 16384 single ended or 8192 differential inputs with 12 digital output lines and 256 PC-81's.

### **1.2.2. Sub-multiplexed interconnection.**

This technique requires a larger number of PC-81's for a given channel density, but has less effect on accuracy for large numbers of channels. For every four single ended or two differential inputs on the host card, you can have :

- 64 single ended or 32 differential inputs with 4 digital output lines and 1 PC-81.
- 1024 single ended or 512 differential inputs with 8 digital output lines and 17 PC-81's.
- 16384 single ended or 8192 differential inputs with 12 digital output lines and 273 PC-81's.

Note that with sufficient digital output lines, the sub-multiplexed technique can be extended far further than this, limited only by accuracy constraints. These constraints are fully described in appendix B.

# CHAPTER 2

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## Architecture and Configuration

### 2.1. Introduction.

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A block diagram of the PC-81 is shown in figure 2.1. The board consists of three basic sections, each of which will be discussed below. Figure 2.2 shows the component layout for the PC-81. The location of the DIP switch and three jumpers used to configure the PC-81 may be obtained from this, as well as from the component overlay on the board. The three sections of the PC-81 are as follows :

### 2.2. Multiplexers.

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This section consists of four 16 channel to 1 channel multiplexers. The inputs to the multiplexers are the 64 input channels, CH0 to CH63. For differential configurations, CH32 acts as the return for channel 0, channel 33 acts as the return for channel 1 etc.

The outputs of these four multiplexers are V0 to V3. In a differential configuration, V2 is the return for V0, and V3 the return for V1.

The input which the multiplexers select is controlled by four of the address input lines, A0 to A3.

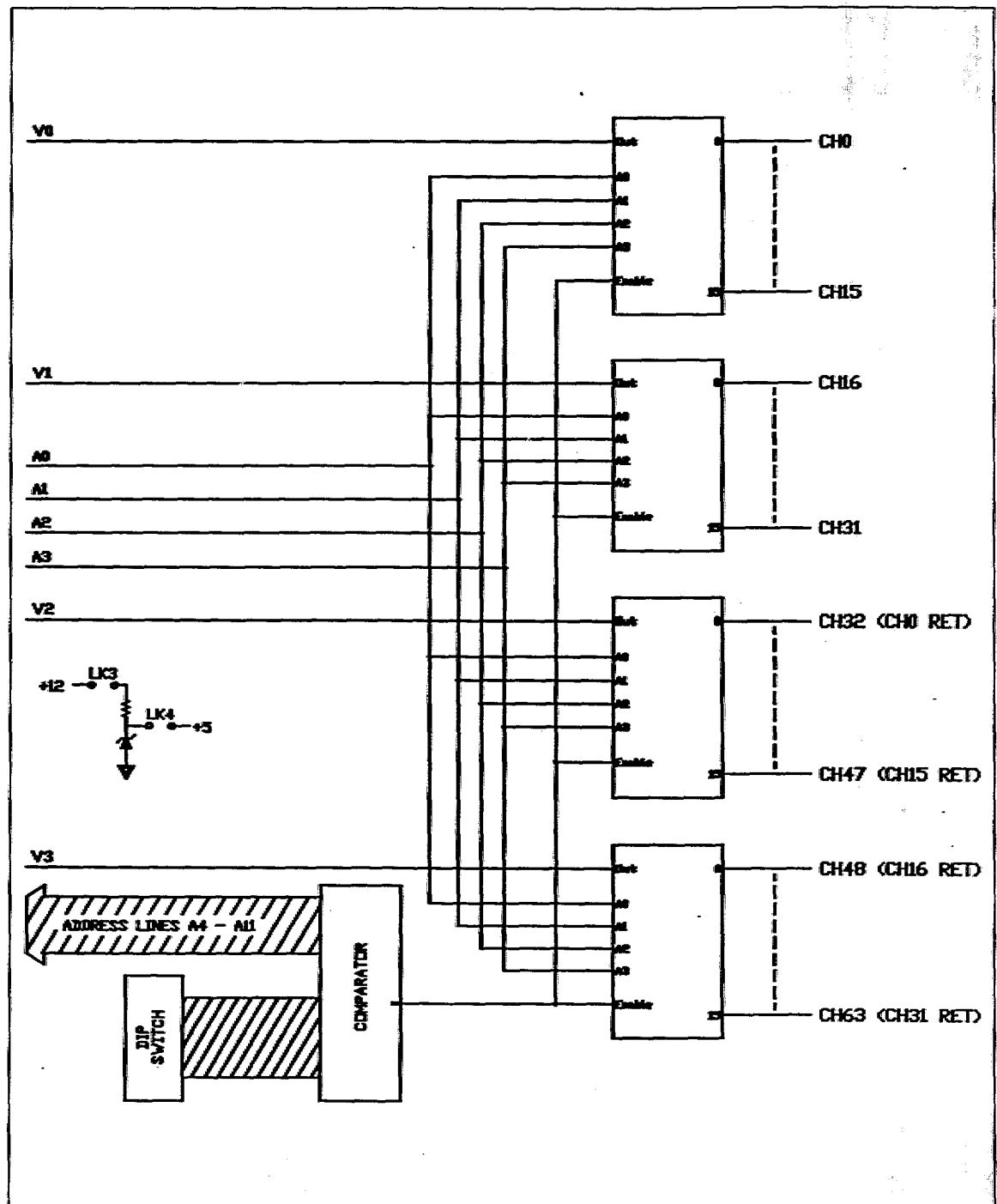
### 2.3. Address comparator.

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#### 2.3.1. Operation.

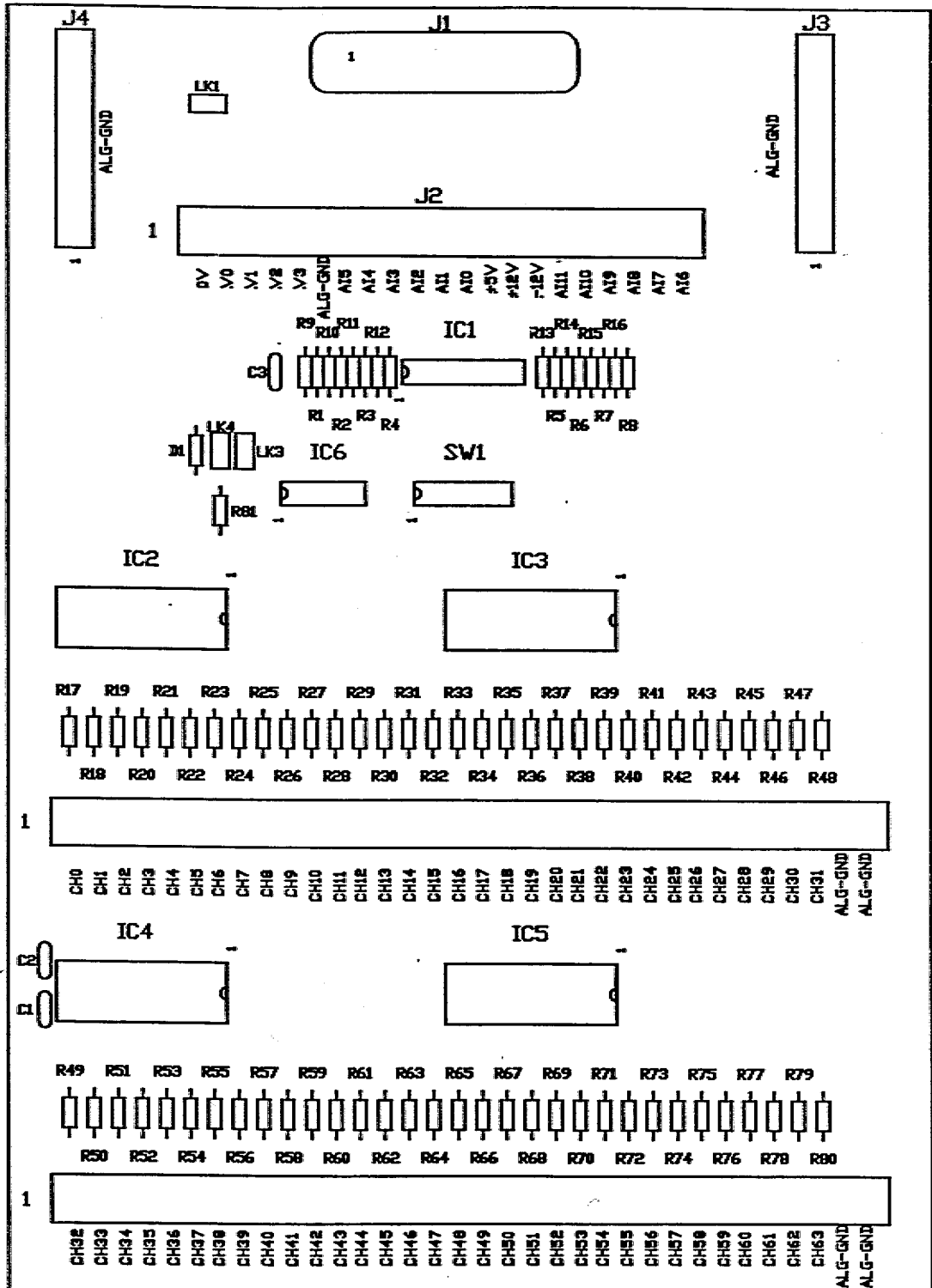
An address comparator is included in the PC-81, to allow the parallel connection of PC-81's. This address comparator compares the address inputs A4 to

Fig 2.1.  
PC-81  
block  
diagram.



A11 to the code set on the DIP switch. If the input code and the DIP switch setting are not identical, then the multiplexer outputs are disabled. Note that if the address inputs are left open, then these inputs default to a logical 0. All switches in the DIP switch must then be OFF for the PC-81 to operate.

Fig. 2.2.  
PC-81  
component  
layout.



### 2.3.2. Configuration

All configuration which is required is to set the DIP switch to the address corresponding to the address to which the PC-81 should respond. Note that in sub-multiplexed mode the addressing feature of the PC-81 is not used, and all DIP switches should be set to the OFF position.

## 2.4. Power supply.

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### 2.4.1. Configuration

Two aspects of power supply operation may be configured :

i. The PC-81 normally operates from +12, -12 and +5V power supplies. However, to allow for operation from host cards which do not supply +5V, the PC-81 has internal provision for the generation of a +5V signal from the +12V supply. Note however that this considerably increases the power consumption of the PC-81.

The internal power supply is enabled by inserting jumpers LK3 and LK4.

**NOTE that these jumper must NOT be installed if the host card supplies +5V power.**

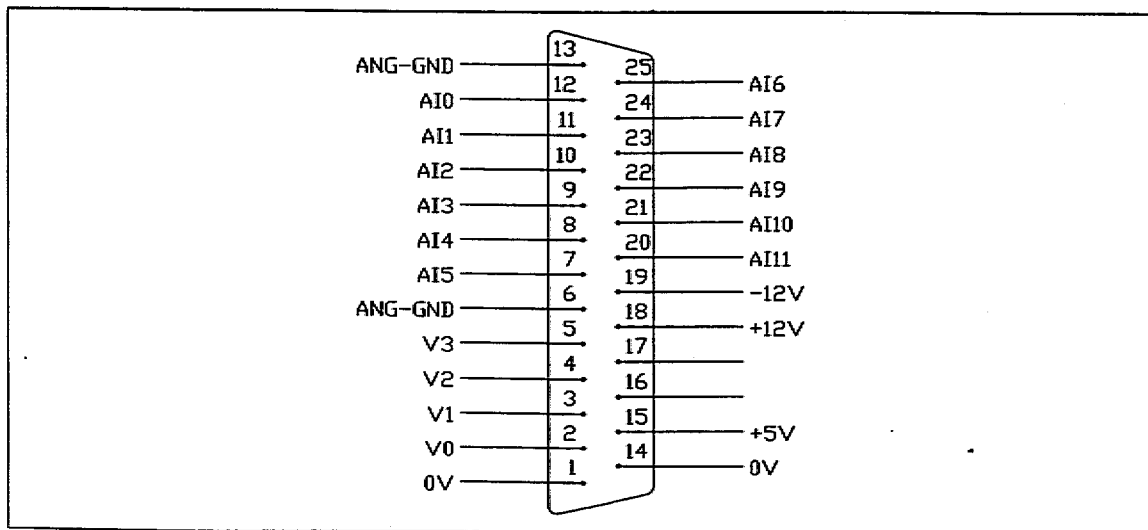
ii. Certain host A/D cards do not have a separate digital and analog ground. For these cards, jumper LK1 can be inserted. This connects the analog and digital ground on the PC-81 together. This jumper is normally not required, and should be inserted only when absolutely necessary, as its use results in an increase in noise levels.

# CHAPTER 3

## Interconnection

This chapter discusses the interconnection of the PC-81 to the host A/D card, as well as connections to the points to be measured. Also discussed are interconnection schemes for multiple PC-81's, and a specific example of connection the the PC-39 A/D card.

Fig. 3.1.  
J1 pin-out.



## 3.1. Connections to the host A/D card.

Connections from the host A/D card to the PC-81 are in several different groups. These signals appear both on J1, a 25 way D-type connector, and on J2, a screw terminal block. The pin-outs of J1 are shown in figure 3.1, and those of J2 in figure 2.1.

### 3.1.1. Analog signal lines. Two groups of signal lines exist :

i. Multiplexer outputs (V0 - V3). These are the outputs of the multiplexers in the PC-81, and must be connected to analog inputs of the host A/D card. Note that for differential applications, V2 is the return line for V0, and V3 the return line for V1.

**Note. Special considerations apply to the use of the PC-81 in conjunction with a PC-26 or PC-30. See appendix C.**

ii. Analog ground (ALG-GND). This line should be connected to the analog ground line of the host A/D card. Note that it should not be connected to the 0V line.

iii. Low order address select lines (AI0 - AI3). These four digital inputs to the PC-81 must be driven by digital output lines from the host computer. The code on these lines selects which of the 64 input channels appear on the 4 output lines V0 - V3.

iv. High order address select lines (AI4 - AI11). These eight digital inputs to the PC-81 can be driven by digital output lines from the host computer. The code on these lines selects, together with the code set on the PC-81's DIP switch, whether or not the output lines, V0 - V3, are enabled. Note that only systems which use multiple PC-81's in a parallel configuration need to make use of these lines, and then only as many as are needed to give each card in the system an unique address. For example, if two cards are to be used in parallel, then only one of the high order address lines needs to be connected. Unused lines may be left open, and will default to a logic 0.

v. Power supply lines. There are four power supply lines :

v.i +12V. This may range from +12 to +15V.

v.ii -12 V. This may range from -12 to -15V.

v.iii +5V. This may range from +4.5 to +5.5V. This supply is not required, but its use is recommended as it substantially reduces power consumption.

v.iv 0V. This is the power supply return and the digital ground.

### 3.1.2. Connections to the points to be measured.

Four connectors are used to connect to the analog points to be measured.

- J3 and J4 are screw terminal blocks which contain only analog ground lines.
- J5 contains input channels 0 to 31. The pin-out of this connector is shown in figure 2.2.

- J6 contains input channels 32 to 63. These channels are the return lines for channels 0 to 31 in differential configurations. The pin-out of this connector is shown in figure 2.2.

## 3.2. The use of multiple PC-81's.

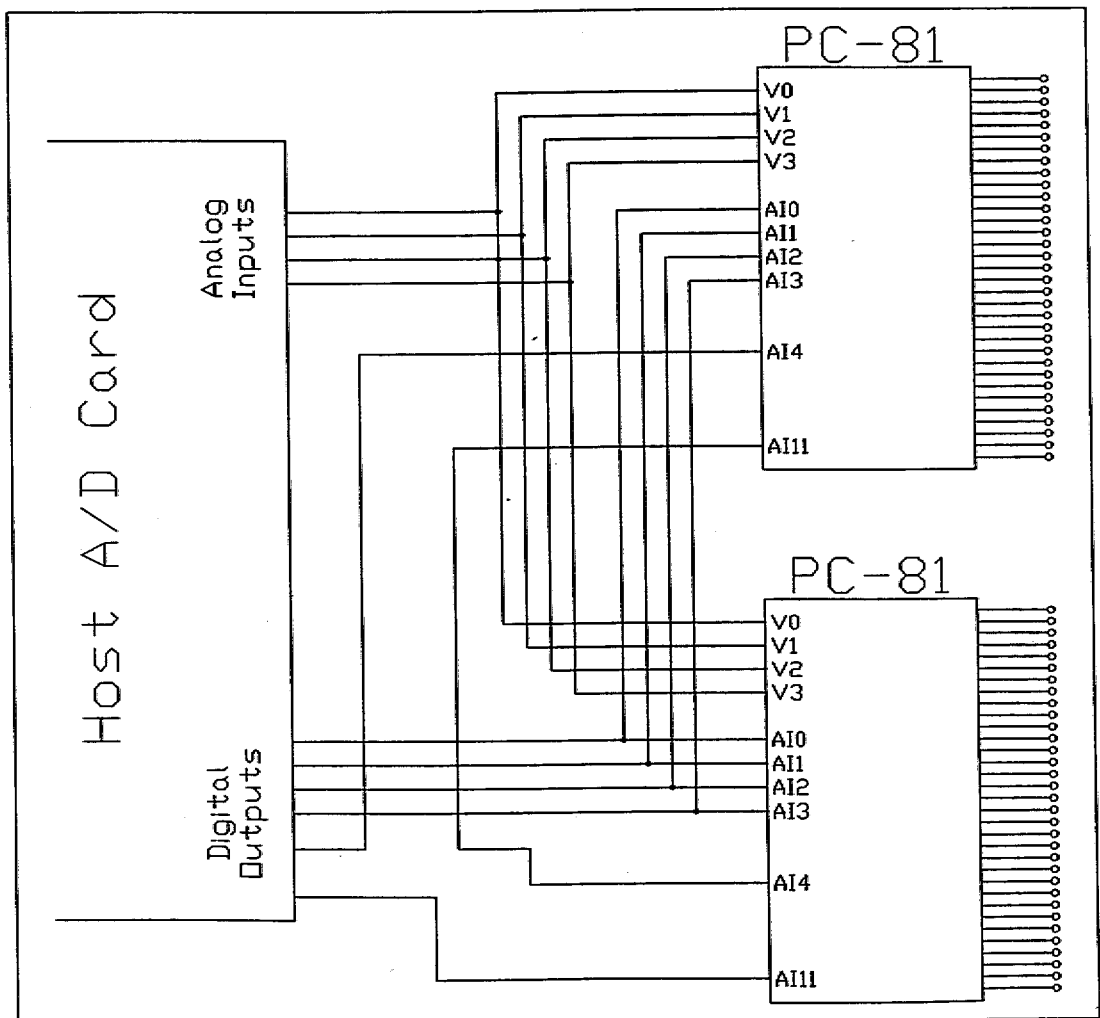
Two basic techniques exist to allow the use of multiple PC81's. These are the parallel and the sub-multiplexed modes.

### 3.2.1. Parallel interconnection.

This technique allows the maximum possible number of channels with the lowest possible number of PC-81's. For every four single ended or two differential inputs on the host card, you can have :

- 64 single ended or 32 differential inputs with 4 digital output lines and

Fig. 3.2.  
Parallel  
interconnection.



1 PC-81.

- 1024 single ended or 512 differential inputs with 8 digital output lines and 16 PC-81's.
- 16384 single ended or 8192 differential inputs with 12 digital output lines and 256 PC-81's.

A block diagram of parallel connection of PC-81's is shown in figure 3.2 for a host A/D card with four input channels.

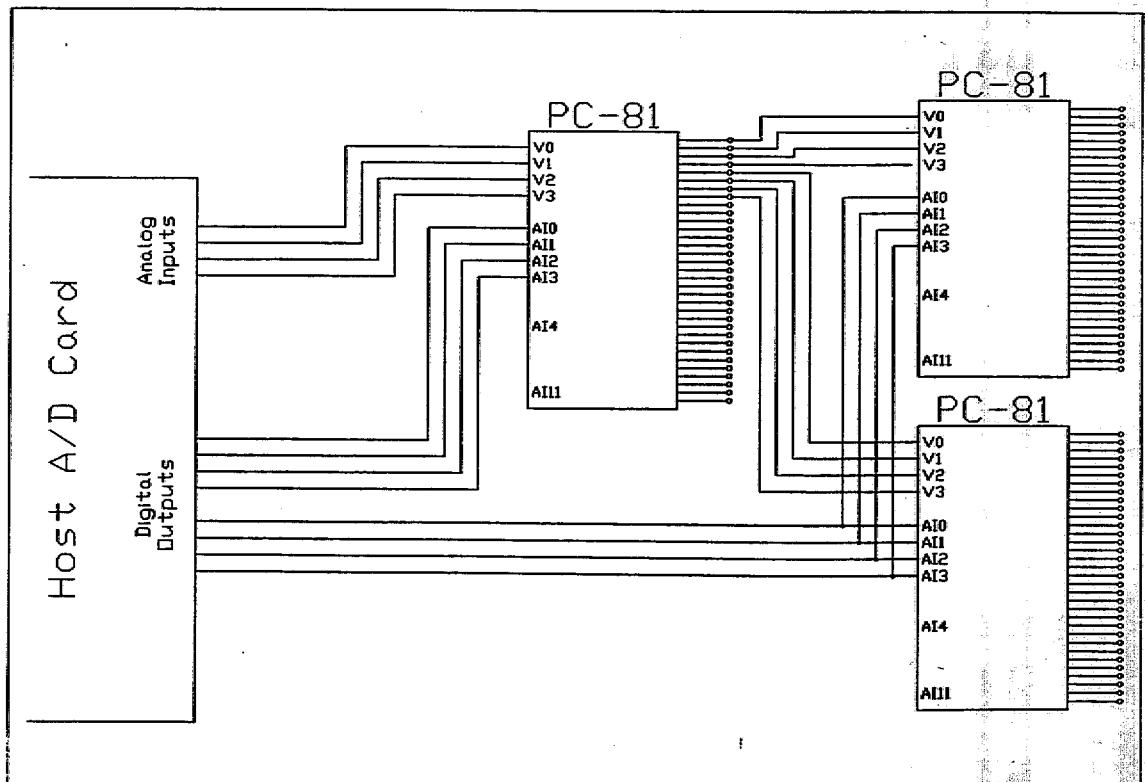
Parallel interconnection operates as follows. The address decoding logic on the PC-81's is used to allow up to 256 PC-81's to be connected in parallel. Each PC-81 has its own unique address, and is only enabled when the address on the high order address inputs matches this address. This address is set on the PC-81's DIP switch.

### 3.2.2. Sub-multiplexed interconnection.

This technique requires a larger number of PC-81's for a given channel density, but has less effect on accuracy for large numbers of channels. For every four single ended or two differential inputs on the host card, you can have :

- 64 single ended or 32 differential inputs with 4 digital output lines and 1 PC-81.
- 1024 single ended or 512 differential inputs with 8 digital output lines and 17 PC-81's.
- 16384 single ended or 8192 differential inputs with 12 digital output lines

Fig. 3.3.  
Sub-multiplexed  
interconnection.



and 273 PC-81's.

Note that with sufficient digital output lines, the sub-multiplexed technique can be extended far further than this, limited only by accuracy constraints. These constraints are fully described in appendix B.

Sub-multiplex operation occurs as follows. All PC-81's are enabled at all times. The input channel selected depends on the low order address inputs of each 'layer' of PC-81's. Figure 3.3. shows a two layer PC-81 system.

### 3.3. Connection to a PC-39.

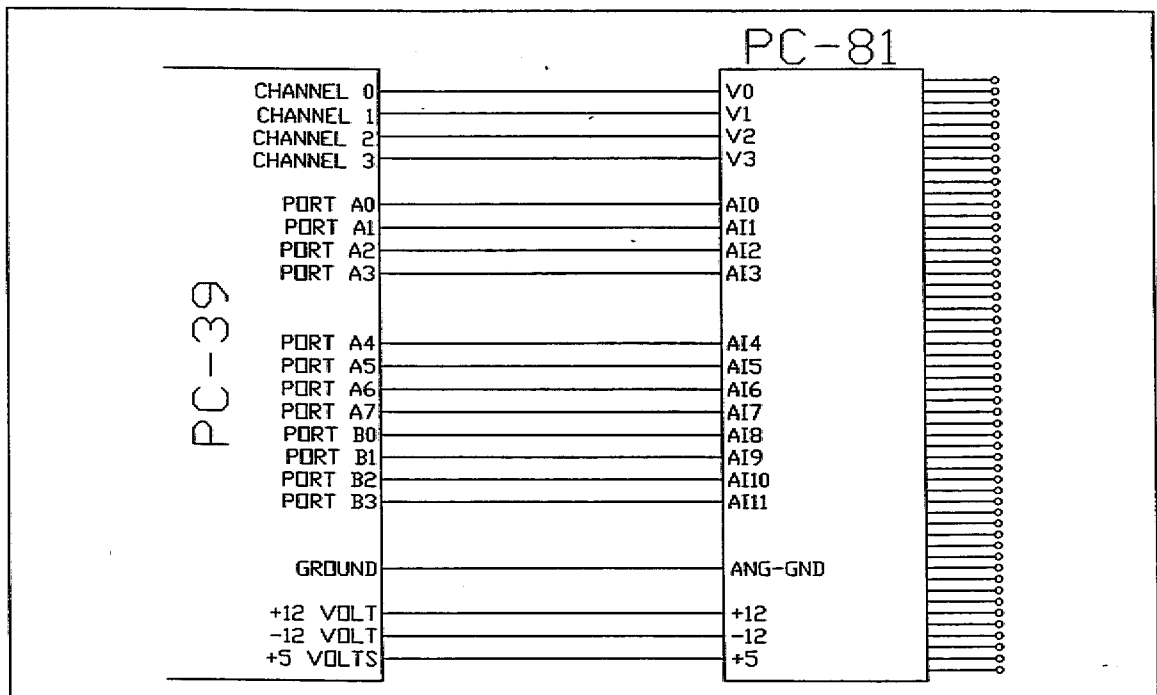
Figure 3.4. shows an actual example of how a PC-39 would be connected to a PC-81.

All of the PC-81's high order address lines are driven. This means that up to 256 additional PC-81's could be connected in parallel to the same four PC-39 analog inputs.

The PC-81 would be configured as follows :

- LK1 would be installed, as the PC-39 does not have a separate analog and digital ground.
- LK3 and LK4 would be removed, as the PC-39 supplies 5 V power.

Fig. 3.4.  
Connection  
to a PC-39.



# CHAPTER 4

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## Software

This chapter discusses the the software considerations necessary for A/D cards which use the PC-81.

### 4.1. Obtaining an A/D sample.

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The steps required to obtain an A/D sample are as follows.

- i. Set the A/D card input channel.
- ii. Set the PC-81 channel.
- iii. Wait for the PC-81 to settle.
- iv. Trigger the A/D converter in the A/D card.
- v. Wait for the A/D conversion to complete.
- vi. Read in the result.

A demonstration program, PC-81.PAS, supplied on the disk included with the PC-81, shows how this is done for a PC-39 A/D card. This program is written in Turbo Pascal, and displays 64 of a possible 256 input channels.

### 4.2. PC-81 settling time.

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As may be seen from the above, the major software consideration in using the PC-81 is the PC-81's settling time.

When using only an A/D card, the settling time of the card's internal multiplexer is included in the card's conversion time, and hence does not require any atten-

tion. If a PC-81 is used however, the settling time of the multiplexers on the PC-81 must be taken into account. This is normally done by a timing loop, although certain A/D cards have timers on board which could be used for this purpose. The use of a timing loop is shown in the demonstration program.

The actual settling time of the PC-81 is dependant on several factors.

- Cable length. The longer the cable between the PC-81 and the host A/D card, the longer the settling time.
- Source resistance. The effect of the cable is mainly to increase capacitance, which must be charged from the voltage to be measured. The higher the source impedance, the longer this will take.
- PC-81 configuration. When using multiple PC-81's, the way in which they are connected significantly effect the settling time. In general, the settling time of sub-multiplexed PC-81's is significantly lower than that of parallel PC-81's.

The following figures may be taken as general guidelines for application which use relatively short cables (less than 1m).

- For a single PC-81 approximately 5  $\mu$ S.
- For multiple PC-81's in sub-multiplexed mode add 5  $\mu$ S for each layer of PC-81's.
- For multiple PC-81's in parallel add 2  $\mu$ S for each PC-81.

# APPENDIX A

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## Hardware Specifications

Number of channels	64 Single ended, 32 differential.
Resistance, input to output	2 K Ohm channel on, 100 M Ohm channel off.
Input capacitance	20 pF max
Output capacitance	20 pF max
Leakage current, inputs	5 nA max (25 degrees celsius), 100 nA max (70 degrees celsius).
Leakage current, outputs	5 nA max (25 degrees celsius), 100 nA max (70 degrees celsius).
Settling time	1.5 $\mu$ S max (10 Ohm source impedance, 50 pF load)
Minimum host A/D input impedance	100 M
Digital inputs	TTL compatible, 100 $\mu$ A maximum leakage current.
Power supply current, +12V	4 mA max (internal power supply disabled), 10 mA max (internal power supply enabled).
Power supply current, -12V	4 mA max.
Power supply current, +5V	500 $\mu$ A max.
Power supply range, +12V	+11.5 to +15 V.
Power supply range, -12V	-11.5 to -15 V.
Power supply range, +5V	+4.5 to +5.5 V.

# APPENDIX B

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## Error Analysis.

Any extra components in the signal path of a data acquisition system will result in measurement errors. In the case of the PC-81, and multiplexers in general, it is the effect of leakage current which is by far the most significant. This is especially the case for large numbers of multiplexers.

### B.1. Multiplexer leakage current.

All multiplexers have some leakage current. For most multiplexers, including those used on the PC-81, this is strongly temperature dependant, typically doubling every 10 degrees celsius. For this reason leakage currents are specified both at 25 and 70 degrees celsius. For the PC-81, and almost all multiplexers used on A/D cards, maximum values for leakage are 5 nA and 100 nA respectively. The typical value of leakage current at 25 degrees celsius is 1 nA.

### B.2. Parallel operation.

For parallel operation, the error due to leakage can be calculated as follows:

$$V_{err} = (N_m + 2)(R_m + R_s)I_m$$

where

- $V_{err}$  is the error voltage due to leakage current,
- $N_m$  is the number of PC-81's,
- $R_m$  is the PC-81's on resistance,
- $R_s$  is the source resistance, and
- $I_m$  is the PC-81 leakage current.

Note that this calculation assumes that the A/D card contains a similar multiplexer to that in the PC-81. This is almost always the case.

### **B.3. Sub-multiplexed mode operation.**

For sub-multiplexed mode operation, the error due to leakage can be calculated as follows :

$$V_{err} = (NI(NI + 1)R_m/2 + NIR_s)I_m$$

where

- $V_{err}$  is the error voltage due to leakage current,
- $NI$  is the number of layers of multiplexers (including the multiplexer on the host A/D card),
- $R_m$  is the PC-81's on resistance,
- $R_s$  is the source resistance, and
- $I_m$  is the PC-81 leakage current.

Note that this calculation assumes that the A/D card contains a similar multiplexer to that in the PC-81, and that this calculation uses the number of layers of multiplexers, not the number of multiplexers. For example, in the diagram shown in figure 3.3,  $NI$  would be 3.

Note also that because the error in the case of sub-multiplexed mode operation is dependant on the number of layers, rather than the number of multiplexers, errors for sub-multiplexed mode operation are considerably lower if large numbers of channels are used.

# APPENDIX C

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## PC-26/30 Considerations.

For users of the PC-26 and PC-30 data acquisition cards, certain special considerations apply.

PC-26 and PC-30 cards have built in termination resistors, in order to prevent errors due to open inputs. These termination resistors must be removed to allow operation in conjunction with a PC-81.

The components in question are the 22K resistor arrays R9 and R10, and the discrete 22K resistors R6 and R7. We recommend removal by simply cutting the leads of these components on the component side of the board. Attempting to desolder the components is not recommended unless you have access to the following equipment:

- Professional PCB rework equipment
- Vapor or ultra-sonic board cleaning equipment, and the expertise to utilize this equipment.

