PC 66C

8/12 Channel D/A Card

User's Manual

For the IBM PC, PC/XT, PC/AT, PS/2 386, 486, Pentuim, ISA and EISA computers

First Edition

14 July 1996

14 July 1996 Printing

© Copyright 1996: Shafique Allie (E-mail: 100075,0441 or shafique@eagle.co.za)
Eagle Technology

Table of Contents

Table of Contents continued...

Introduction

The PC 66C 8 or 12 channel DAC board is a high accuracy Digital to Analog Board for the IBM PC/XT/AT, 486, Pentuim, ISA and EISA Computers. It provides 12 channels of D/A with remote sensing capability which compensates for voltage drops over long leads. DAC settling times are less than 2µs for a 10V output swing. Parallel triggering is also another feature of this board which makes it ideal for fast three phase waveform generation. Eight DACs can be preloaded with new output values and then updated in parallel by an eight bit control word. The other 4 DACs can also be updated in the same way by a 4 bit control word.

The PC 66C fits into one of the IBM 8 bit expansion slot.

Typical applications

- Three Phase Waveform Generation
- Process Control (eg: material transfer rates, fluid flow, motor speed, etc)
- Laboratory Automation
- Energy management
- Product testing

Key Features

- On-board wait state generation allows operation on high speed computers
- Provides 8 or 12 DACs with Remote Sense Inputs in bipolar mode
- Simulataneous Update feature for the first 8 DACs and the last 4 DACs.
- Optically Isolated External Trigger Interrupt available
- Ideal for three phase waveform generation
- DAC output voltage range variable by reference voltage from ±5V to ±10V
- Driver software libraries for C, Pascal, Qbasic Basic and Visual Basic is provided for easy programming. Windows drivers (DLL) including LabView, LabTech Notebook, DasyLab, TestPoint is also provided.

PC 66C Package

The PC 66C package consists of:

- PC 66C Interface Card
- PC 66C User's Manual
- EDR Developers Toolkit User Manual + 3½' diskettes
- A DB37 Male Connector
- One 3½' diskette containing the PC 66C demonstration software

If any of the items is missing, contact your dealer immediately specifying which components are missing.

Chapter 1: Installation

There are two aspects of the PC 66C that must be configured:

1.1) The Base Address

This address determines where the board is accessed. This can be set by a 8-way DIP switch found on the PC 66C Board. The address range are from 0 to 7ffh.

1.2) Wait State generation

Some computers have very high I/O bus cycles. In this case it is neccessary to slow down these cycles when the computer accesses the PC 66C Board. Additional wait states can be set by means of a jumper on the PC 66C Board.

1.1) Setting the base address

The PC 66C occupies a block of 32 consecutive I/O addresses. The base address setting controls where the block starts. This base address must be unique to the PC 66C only and no other card must occupy this address. If multiple PC 66C boards are installed in one computer then each board must have a different base address.

The base address can be assigned to any location from 0 to 7ffh in 32 byte boundaries. Table 1 shows the I/O addresses occupied by standard interface cards. Refer to the Base Address Setting Table in Appendix A for a list of the various base address settings that the PC 66C can occupy.

The base address setting can be set by adjusting the 8-way dip switch on the PC 66C. Each line on the DIP switch switch compares an address line in I/O space. Switch number 1 compares address line A12; switch number 2: address A11 while switch number 8 compares address line A5. Factory default setting is 300h.

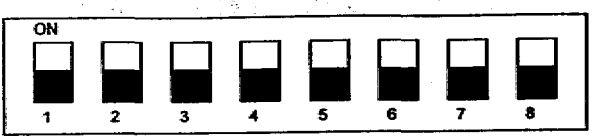
If one of the switches are OFF, then it contributes to the base address. An example is as follows:

```
Base Address  =   Switch 4 (Addr A9) + Switch 5 (addr A8)
              =   200 + 100
              =   300h
```

Table 1: Addresses for standard I/O devices

Address	Standard device
000-1FF	Internal system board
200-20F	Games port
210-217	Expansion unit
220-24F	Reserved
250-257	Not assigned
258-25F	Intel 'Above Board'
260-277	Not assigned
278-26F	Reserved
280-2EF	Not assigned
2F0-2F7	LPT2
2F8-2FF	COM2
300-31F	Prototype Board
320-32F	Hard Disk
330-377	Not assigned
378-37F	LPT1
380-38F	SDLC communications
390-39F	Not assigned
3A0-3AF	Binary comms
3B0-3BF	Mono Display Adaptor
3C0-3CF	Reserved
3D0-3DF	CGA
3E0-3E7	Reserved
3E3-3EF	Not assigned
3F0-3F7	Floppy disk
3F8-3FF	COM1
400-FFF	Not used see below

Table 1: Standard I/O Addresses



1000	800	400	200	100	80	40	20	Hex Weight when OFF
A12	A11	A10	A9	A8	A7	A6	A5	Corresponding Address line

Figure 1: Dip Switch Address Weight (in Hex)

Note that addresses from 400h-7FFh cannot normally be used because these addresses are not normally decoded by some cards and I/O devices in the 0h to 3FFh range.

The PC 66C D/A board however (and most other members of the PC-XX family) can use these addresses, if and only if the board at address 400h less than the address of the PC 66C also decodes the extra address.

For example, a PC 66C can be installed at address 300h and another one at address 700h (400h locations apart). However, it would not be advisable to install a PC 66C at address 7F8h. This is because communications port COM1 is installed at 3F8h and does not normally decode these extra addresses.

If your computer has boards not listed in Table 1 (such as LAN adaptors, back-up boards or other engineering boards), you should consult the User's Manuals for these boards for information on the address ranges used.

In most cases, base address of 300h is a good choice. Address 300h is also the factory default base address setting.

1.2) Wait State Generation on the PC 66C

Additional wait states can be inserted in the I/O bus cycle by changing the jumper setting on JP1 on the PC 66C. This jumper is marked 'Wait State Jumper' on the PC 66C board. Refer to figure 1.2 for the wait state jumper settings. Note that the factory default setting is zero wait states.

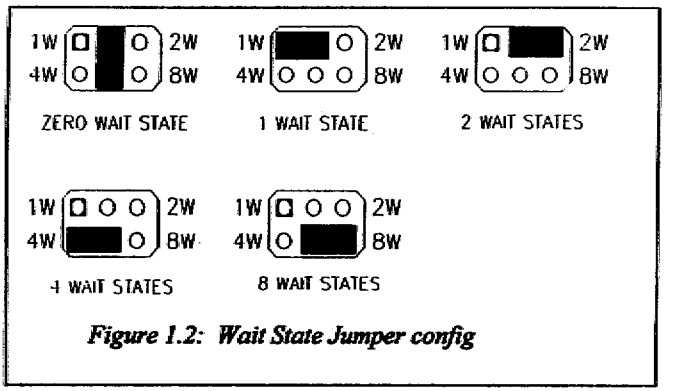


Figure 1.2: Wait State Jumper config

In most cases, only a very small number of computers require additional wait states. If the PC 66C seems to be giving incorrect results then try increasing the wait states until correct results are obtained. If the board still does not produce correct results even after the maximum number of wait states has been inserted then the PC 66C or the host computer are defective and should be serviced.

1.3) Interrupt Jumper Settings

If the external trigger option is used, then it is necessary to configure the interrupt jumper settings. Refer to figure 3 for the interrupt jumper settings.

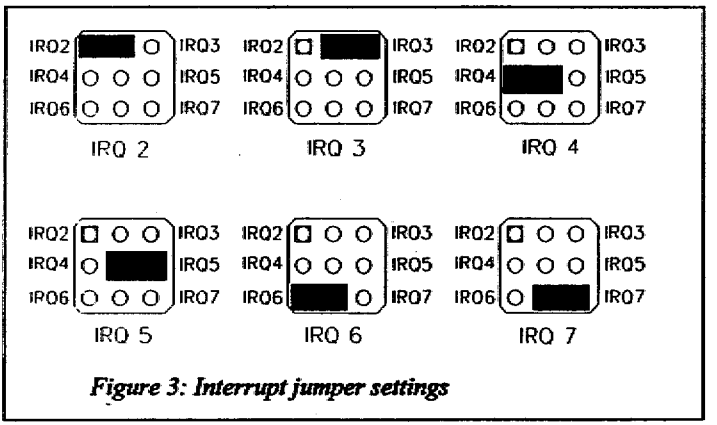


Figure 3: Interrupt jumper settings

In a standard PC, the interrupt levels are allocated as follows:

Level Level	Allocation
IRQ0	System timer
IRQ1	Keyboard
IRQ2/IRQ9	Display Adaptor
IRQ3	COM1 (if installed)
IRQ4	COM2 (if installed)
IRQ5	LPT2 (if installed)
IRQ6	Floppy disk controller
IRQ7	LPT1 (if installed)

Table 2: Standard Interrupt Settings

On PC ATs, IRQ2 is used by the system board itself and any interrupt requests on IRQ2 is transparently rerouted to IRQ9.

The default IRQ setting on the PC 66C is IRQ7. Note that unless the interrupt line is specifically enabled by software, the interrupt output from the PC 66C is tri-stated (ie: not connected). It is also tri-stated upon power-up.

1.4) Parallel Trigger Jumper Settings

Parallel Triggering (or simultaneous update) is used to ensure that the DACs output voltage changes at the same time. This ensures that there are no phase difference between the DACs. Jumper Settings are as follows (see figure 1.4):

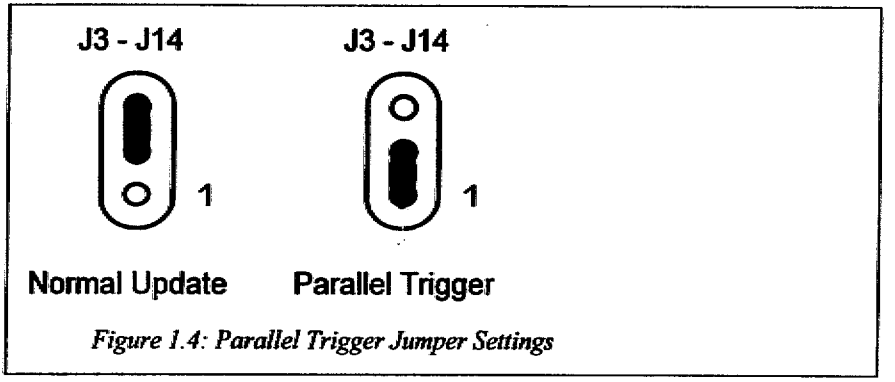


Figure 1.4: Parallel Trigger Jumper Settings

In normal mode, the DACs are updated as soon as the low order bits are written. This means that the MSB must be written first.

If parallel trigger is used, then either the MSB or LSB can be written first. The voltage at the DAC output will only change when a zero is written to the respective DAC bit n the parallel trigger register:

Base Address + 18h :	DAC0 thru DAC7
Base Address + 19h:	DAC8 thru DAC11 (lower four bits only)

Note that the parallel trigger jumper must be set in order for simulataneous update to function properly.

1.5) Connecting the PC 66C to the PC Backplane

Requirements:
- XT/286/386/486, ISA, EISA, Pentium Computer
- Phillips Screw Driver (or one to match screw on the computer cabinet and bracket)
- 8 bit or 16 bit bus slot

Procedure:

a) Switch off the computer and all attached devices
b) Unplug power cord from the computer and all attached devices.

> **☞ Warning**
>
> Failure to disconnect all power cables can result in harzardous conditions, as there may be dangerous voltage levels present in externally connected cables.

c) Remove the top cover from the PC. If you are not sure how to do this, consult the manual supplied with the system unit.

d) Choose any 8 or 16 bit expansion slot and remove the screw from the metal bracket fixed corresponding to the chosen slot.

e) Align the gold plated edge connector with the edge socket and the rear adaptor slot with the board bracket. Firmly press the board down into the socket on the computer's system board. Ensure that the board's edge connector is in the socket and has not slipped sideways past the socket.

f) Replace the screw on the bracket and tighten the screw to the back panel.

g) Replace the computer's cover. Plug in all cables and switch the computer power on. The PC 66C is now installed.

CHAPTER 2: Interconnections

The PC 66C 8/12 Channel DAC board plugs into any ISA expansion slot at the gold finger edge connectors J1/J2. The board communicates to the user circuit via connectors mounted on the bracket. This chapter describes these connectors

2.1) Connections to the IBM Bus

The PC 66C board may be plugged into any slot of the computer backplane with the exception of J8 slot of the IBM XTs. All data transfers to and from the host computer is channelled via this connector.

2.2) User Connector

The PC 66C interfaces to the external world via a 37 way D-type female connector. This connector acommodates the following signals:

- Eight Monopolar Voltage Outputs
- Twelve Bipolar Voltage Outputs
- Twelve Bipolar Sense Outputs
- Optically isolated external trigger point and the return line
- Analog Grounds (3 points)

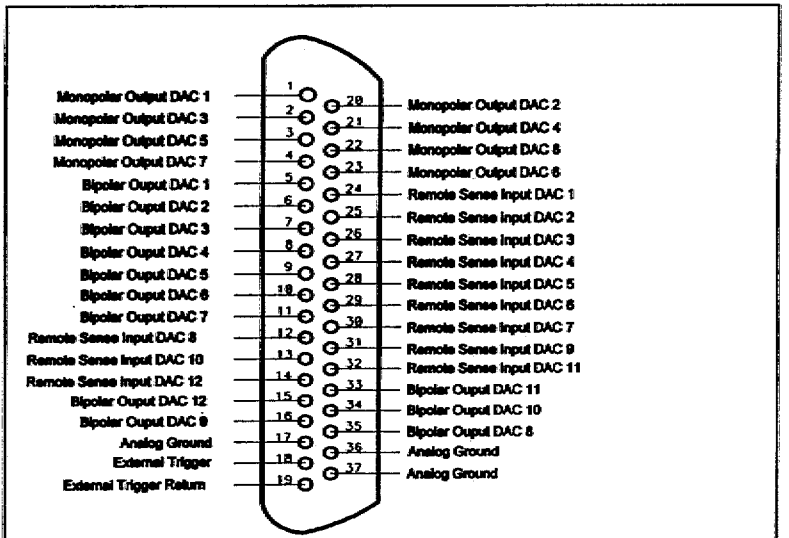


Figure 2.2: PC 66C Interface Connector (as seen from the rear of the PC)

Figure 2.2 graphically shows the connector together with their pin assignments. Note that the pin connections refer to the pin numbers of the connector when looking into the connector from the rear of the computer. Also note that the pin numbers are embossed on the connector itself.

Before making any connections to the PC 66C make sure that your PC is switched off. Ensure that all the output leads of the DAC connections are kept as short as possible or otherwise use the remote sense facility.

2.3) Cable precautionary measures

See figure 2.3 for applications which uses the remote sense facility.

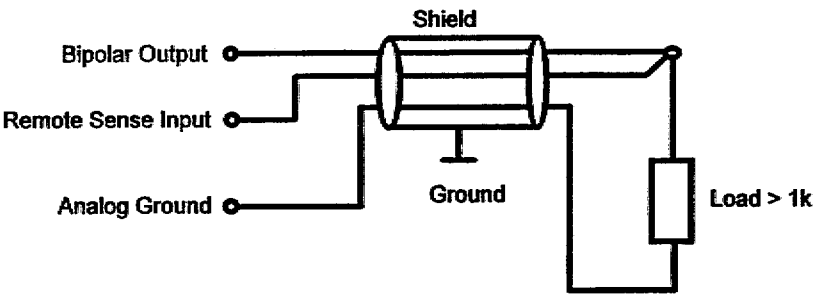


Figure 2.3: Remote Sense Interconnections

When generating waveforms of more than 50Hz with output leads longer than 3m you should use separate screened cables for each of the channels in order to avoid crosstalk. If the remote sense facility is not used then you must connect the remote sense iuputs of the respective channel to the respective DAC Voltage output pin on the DB37 connector. If you do not do this then the outputs will be pulled to about -10.6V.

> ☞ **Warning**
>
> If you do not intend using the remote sense facility of the DACs then you MUST connect these inputs to the appropiate DACs. Failure to do so will result in no DAC voltage change on the output after the digital data is written.

2.4) The Analog Ground Pins on the DB37 Connector

It is recommended that you use all the analog output pins to ensure that crosstalk between channels are minimized.

2.5) External Interrupt Trigger Line

This line can be used as an external interrupt trigger line to enable automatic shutdown/switch-on of the DACs. This line is optically isolated from the digital circuitry of the PC 66C. The output is connected to the interrupt line of the IBM bus via associated circuitry. Figure 2.5a illustrates the optically isolated connections:

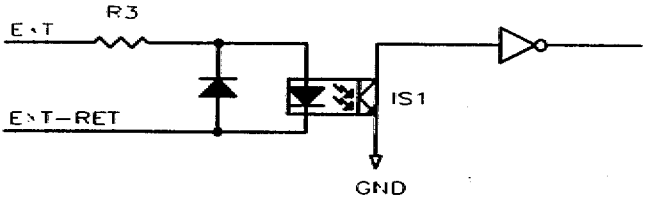


Figure 2.5a: Optically Isolated Trigger Line

Note that the External Trigger Return line can be connected to ground via jumper J16 if you wish. The default setting is enabled which hence connects the External Trigger Return to Digital Ground.

CHAPTER 3: Register Structure

3.0) Introduction

At the lowest level, the PC 66C can be programmed using I/O input and output instructions. This chapter contains the information on all the PC 66C registers. Although programming the board is not difficult, it is time consuming and requires detailed knowledge of the PC 66C as well as the operation of the host PC and its operating system. In order to simplify the process, a set of driver libraries is provided. The use of these libraries allow access to all the board's functions and is described in Chapter 5: Programming guide.

The PC 66C occupies 32 consecutive addresses in the computer's I/O space. The layout of these registers are shown in Table 4: PC 66C register structure. The offset of the registers are given as offset addresses from the base address of the board. This base address is set with the Dip Switch as detailed in Chapter 2: Installation.

Offset (Decimal)	Offset (Hex)	Read	Write
0	0	N/A	DAC 0 MSB
1	1	N/A	DAC 0 LSB
2	2	N/A	DAC 1 MSB
3	3	N/A	DAC 1 LSB
4	4	N/A	DAC 2 MSB
5	5	N/A	DAC 2 LSB
6	6	N/A	DAC 3 MSB
7	7	N/A	DAC 3 LSB
8	8	N/A	DAC 4 MSB
9	9	N/A	DAC 4 LSB
10	0A	N/A	DAC 5 MSB
11	0B	N/A	DAC 5 LSB
12	0C	N/A	DAC 6 MSB
13	0D	N/A	DAC 6 LSB
14	0E	N/A	DAC 7 MSB
15	0F	N/A	DAC 7 LSB
16	10	N/A	DAC 8 MSB
17	11	N/A	DAC 8 LSB
18	12	N/A	DAC 9 MSB
19	13	N/A	DAC 9 LSB
20	14	N/A	DAC 10 MSB
21	15	N/A	DAC 10 LSB
22	16	N/A	DAC 11 MSB
23	17	N/A	DAC 11 LSB
24	18	N/A	XFER 0
25	19	N/A	XFER 1
26	1A	STATUS	IEN

Table 3.0: PC 66C register structure

3.1) DAC 0...DAC11 - Write Register (offset 0 - LSB / offset 1 - MSB, write)

These registers are exactly the same for all the DACs. The input registers of the DACs are arranged to accept a left-justified data word from the PC with the most significant 8 bits coming first (MSB) and the lower (LSB) second. Left justification simply means that the binary point is assumed to be located to the left of the most signicant bit. Mapping is shown graphically below:

12 bit Dataword															
MSB								LSB							
DAC Number Base + 1								DAC Number Base + 0							
12	11	10	9	8	7	6	5	4	3	2	1	x	x	x	x
Write first								Write Second							

Figure 3.1a: DAC 12 bit Word format

Note: x - don't care

DAC 0 loading sequence is shown below.

LSB Register (write only, offset 0)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B3	B2	B1	B0	x	x	x	x

Bit 7 thru 4: These bits specify the least significant bits of the 12 bit DAC data (B3 thru B0). These bits are written as one byte at DAC Number Address + offset 0.

Bit 3 thru 0: These bits are undefined.

MSB Register (write only, offset 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B11	B10	B9	B8	B7	B6	B5	B4

Bit 7 thru 0: These bits specify the most significant bits of the 12 bit DAC data (B11 thru B4). These bits are written as one byte at DAC Number Address + offset 1.

The above data format is the same for all the DACs: DAC0 thru DAC 11. The table for the MSB and LSB register for each DAC are shown below:

DAC NO	MSB	LSB	DAC NO	MSB	LSB
0	BASE + 1	BASE + 0	6	BASE + 13	BASE + 12
1	BASE + 3	BASE + 2	7	BASE + 15	BASE + 14
2	BASE + 5	BASE + 4	8	BASE + 17	BASE + 16
3	BASE + 7	BASE + 6	9	BASE + 19	BASE + 18
4	BASE + 9	BASE + 8	10	BASE + 21	BASE + 20
5	BASE + 11	BASE + 10	11	BASE + 23	BASE + 22

Table 3.1b: DAC lsb and msb address locations

3.2) XFER0 - Parallel Trigger Status Register (offset 18h, write only)

This register is used to update the first eight DACs simultaneously.

XFER0 Register (write only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

Bit 0 to 7: These bits represents the simultaneous update bits for each DAC0 thru DAC7. With Bit 0 enabling DAC0, Bit 1 enabling DAC1, etc. Writing a zero for each bit automatically update the appropriate DACs.

For example, writing a 1111 1000b (or F8 hex) to this register automatically updates DAC0 , DAC1, DAC2 at the same time. Note that the Jumpers for parallel triggering must be set correctly before the parallel update is effective.

> ☞ **Note**
>
> *If the parallel trigger jumpers (J3-J14) on the PC 66C are not set correctly then the parallel update feature will not work correctly. To ensure that this feature is working, Jumpers J3 thru J14 must have (1-2) short.*

3.3) XFER1 - Parallel Trigger Status Register (offset 19h, write only)

This register is used to update the last four DACs simultaneously.

XFER1 Register (write only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
x	x	x	x	DAC11	DAC10	DAC9	DAC8

Bit 0 to 3: These bits represents the simultaneous update bits for DAC8 thru DAC11. With Bit 0 enabling DAC8, Bit 1 enabling DAC9, etc. Writing a zero for each bit automatically update the appropriate DACs.

For example, writing a 1111 1010b (or FA hex) to this register automatically updates DAC8 and DAC10 respectively. Note that the Jumpers for parallel triggering must be set correctly before the parallel update is effective. Note that the last four high order bits are not used hence either a 0 or a 1 can be written to these bits. For the sake of clarity, I suggest that 1s be written to these locations.

Bit 4 to 7: These bits are reserved and have no effect on the DAC update feature.

> **☞ Note**
>
> *If the parallel trigger jumpers (J3-J14) on the PC 66C are not set correctly then the parallel update feature will not work correctly. To ensure that this feature is working, Jumpers J3 thru J14 must have (1-2) short.*

3.4) IEN: - Interrupt Enable / Status register (offset 1A: read/write)

This register contains control/status bits for the external optically isolated trigger line, Interrupt Enable as well as the IRQ Clear line.

IEN Register (write mode)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	IRQCLR	IRQEN

IEN Register (read mode)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
x	x	x	x	IRQCLK	IRQSET	/IRQCLR	IRQEN

Bit 0: Controls the interrupt line. Setting this bit to 1 enables the interrupt line while setting the bit to 0 disables the line. Note that bit 0 is set to 0 upon power up. Reading back this bit provides the status of the interrupt enable line.

Bit 1: Clears the interrupt flip flop. Two writes will initiate clear this register bit. Write a 1 and then a 0 to this register. Reading back this line will appear inverted. For example, writing a zero to this line will yield a 1 when reading this bit back and v.v.

Bit 2: Reading back this line determines the status of the output of the IRQ register. This line can be read back irrespective of the status of the IRQEN bit.

Writing to this line is undefined.

Bit 3: Reading back this line determines the status of the opto isolator. For example if the External Trigger line voltage is less than 3V then the bit read back on this line after initiating a read cycle will be 0. If the External Trigger line voltage was greater than 3.1V and less than 24V then the bit read back on this line will be 1.

Writing to this line is undefined.

Bit 4 thru 7: Reserved for manufacturing tests. Write a 0 to these bits. Reading these bits are undefined.

Chapter 4: Programming Guide

4.0) Introduction

This chapter describes programming the PC 66C at its lowest level. In order to accomplish this, detailed knowledge of chapter 4 and the system hardware is required.

As an alternative to low level programming, driver software is provided with the PC 66C. This is described in Chapter 5.

The advantages of using the driver software are:

a) Detailed knowledge of the PC 66C is not required.
b) The Driver Libraries supports multiple boards. In other words, you can cascade boards in the same computer.
c) The Driver Library is callable from most high level languages.

Programmers who need to incorporate special routines into their application will need to read this chapter. Examples are application programs written in Clarion, Clipper, etc.

Once the PC 66C has been installed into the computer and external connections are made, the board is in an operational state. The PC 66C occupies 32 consecutive I/O addresses starting from the board's base address. The base address is set by the DIP Switch on the PC 66C. Programming the PC 66C is done by using the input/output instructions. Reading and writing to these addresses allows data to be moved to and from the PC 66C.

Reading and writing to these ports typically takes on the form of one of the following instructions:

Language	Port Read	Port Write
'C'	value = inp(addre);	outp(addre, value);
Pascal	value := port[addre];	port[addre] := value;

Assembly	mov al, value
	mov dx, addre
	in al, dx
		mov al, value
		mov dx, addre
		out dx, al

where: addre is the I/O location of the PC 66C registers
value is the byte read or written to the register

4.1) Initialization

It is preferred to initialize the PC 66C to a known state before performing certain tasks. Note that it is not necessary to perform this procedure because all registers are set to a known state upon power-up. The default powerup voltage on the DACs are -10V.

4.2) Loading sequence of the D/A

The input registers of DACs of the PC 66C are arranged to accept a left-justified data word from the PC with the most significant 8 bits coming first (msb) and the lower (lsb) second. Left justification simply means the binary point is assumed to the left of the most significant bit. Figure 4.2a below illustrates this:

12 bit Dataword															
MSB								LSB							
DAC Number Base + 1								DAC Number Base + 0							
12	11	10	9	8	7	6	5	4	3	2	1	x	x	x	x
Write first								Write Second							

Figure 4.2a: Left justified data format

Note: x - don't care

If the parallel trigger facility is not used, then the output of the DACS are updated as soon as the 4 least significant bits are written to the respective I/O addresses.

To write to the DAC under program control, proceed as follows:

a) Write the 8 msb's of the 12 bit data word into msb port of the DAC. For example, for DAC0 it would mean at Base Address + 1, for DAC6 it would mean at Base address + 13, etc. *See table 4.2a for DAC msb locations.*

b) Write the 4 lsb's of the 12 bit data word (left justified) into the lsb port of the DAC. For example, for DAC0 it would mean at Base Address + 0, for DAC6 it would mean at Base address + 12, etc. *See table 4.2a for DAC lsb locations.*

DAC NO	MSB	LSB	DAC NO	MSB	LSB
0	BASE + 1	BASE + 0	6	BASE + 13	BASE + 12
1	BASE + 3	BASE + 2	7	BASE + 15	BASE + 14
2	BASE + 5	BASE + 4	8	BASE + 17	BASE + 16
3	BASE + 7	BASE + 6	9	BASE + 19	BASE + 18
4	BASE + 9	BASE + 8	10	BASE + 21	BASE + 20
5	BASE + 11	BASE + 10	11	BASE + 23	BASE + 22

Table 4.2b: DAC msb and lsb address locations

Programming code in Pascal (assuming the base address of the PC 66C is 300h) is as follows:

```
MSB := HI( D SHL 4);
LSB := LO( D SHL 4);
PORT[$301] := MSB; {write hi byte to DAC0 MSB register}
PORT[$300] := LSB; {write lo byte to DAC0 LSB register}
```

Note: If the parallel trigger facility is not used then the msb must be written first. The DAC is automatically updated as soon as the LSB is written.

4.3) Setting the DACs

> ☞ **Warning**
>
> *The calibration procedure and formulae supplied allow the DACs to range from -Full Scale to +Full Scale. This is, however, different fromthe classical calibration procedure which only allows the DAC to reach Full Scale - 1 LSB.*

a) Monopolar Mode:

When using the monopolar outputs of the DACs, the output voltage is defined with a 12 bit data word in the following way:

Vout = -Vref * D / 4095

where Vref is the reference voltage which is used for all DACs.

To set the output Vout of the DAC channel, the necessary 12 bit data word D is calculated in Turbo Pascal in the following way:

D := ROUND((Vout/(-Vref)) * 4095);

Where Vref = -5.000V (Note for calculations Vref is exactly -5.000V)

The MSB and LSB values which have to be written to the DAC Registers (left justified data format, as described above) are calculated in Turbo Pascal as follows:

```
MSB := HI( D SHL 4);
LSB := LO( D SHL 4);
PORT[$301] := MSB; {write high byte to DAC0 MSB register }
PORT[$300] := LSB; {write low byte to DAC0 LSB register}
```

Note: If the parallel trigger facility is not used then the MSB must be written first. The DAC is automatically updated as soon as the LSB is written.

If parallel trigger is used, then either the MSB or LSB can be written first. The voltage at the DAC output will only change when a zero is written to the respective DAC bit n the parallel trigger register:

Base Address + 18h :	DAC0 thru DAC7
Base Address + 19h:	DAC8 thru DAC11

b) Bipolar Mode:

When using the bipolar outputs of the DACs, the output voltage is defined with a 12 bit data word in the following way:

Vout = -Vref * (D - 2048) / 2048

where Vref is the reference voltage which is used for all DACs.

To set the output Vout of the DAC channel, the necessary 12 bit data word D is calculated in Turbo Pascal in the following way:

D := ROUND((Vout * (2048/Vref)) + 2048);

Where Vref = -5.000V (Note for calculations Vref is exactly -5.000V)

The MSB and LSB values which have to be written to the DAC Registers (left justified data format, as described above) are calculated in Turbo Pascal as follows:

```
MSB := HI( D SHL 4 );
LSB := LO( D SHL 4 );
PORT[$301] := MSB; {write hi byte to DAC0 MSB register }
PORT[$300] := LSB; {write lo byte to DAC0 LSB register}
```

Note: If the parallel trigger facility is not used then the msb must be written first. The DAC is automatically updated as soon as the LSB is written.

If parallel trigger is used, then either the MSB or LSB can be written first. The voltage at the DAC output will only change when a zero is written to the respective DAC bit n the parallel trigger register:

Base Address + 18h :	DAC0 thru DAC7
Base Address + 19h:	DAC8 thru DAC11

4.4) External Triggering

This external trigger function is an additional feature present in the PC 66C only. This feature provides an auto reset DAC feature using interrupts. The input line is optically isolated from the digital circuitry. A voltage of 0 to 3V on this input line will give a logical low (0V) while a voltage of 3.1V - 24V will give a logical high (5V). If a +ve edge (low high) transition has occurred then the interrupt line (if enabled) will be pulled high. An interrupt service interrupt routine will then be service. This can be a simple program to switch the write to all the DAC in order to reset them to zero. It can also be used for any other purpose as well. A detailed example is explained in the EDR Software Developers Toolkit User Manual.

Procedure

a) Write a 1 to the IEN Register (Base + 20) in order to enable interrupts.
b) Write interrupt service routine (ISR).
c) Ensure that a Low - High transition occurs on the optically isolated input lines.
d) If so, then ISR will be serviced.
e) Write a 11b (or 3 hex) to the IRES register (offset + 20) and then a 01b (or 01 hex) in order to reset the interrupt flip flop.
f) Return to c)

Note that the status of the external trigger line or opto isolator can be determined by reading back the INTEN register and checking bit 2. If the bit is Low (0V) then the interrupt line is not active. If it is high (5V) then the interrupt line has been serviced.

4.5) Interrupt Handling

The external trigger line is connected to the interrupt line on the PC's I/O channel. This allow external hardware devices to request attention from the host computer. Note that the external trigger line is signal conditioned (optically isolated) thus a higher voltage can be fed into this line. This output of this isolator is TTL compatible and fed into the PC's interrupt system via associated circuitry.

Chapter 5: Driver Software

Full driver software is supplied with the PC 66C package. Full details are explained in the EDR Software developers kit User Manual. A summary of what these drivers consist of are explained below.

Both DOS and Windows Languages are supported: They are:

DOS Languages:

Borland C/C++ Version 3.1 or 4.0
Microsoft C/C++ Version 6.0 or 7.0
Borland Pascal / Turbo Pascal Version 6.0 or 7.0
Microsoft QuickBasic Version 4.5

Windows Languages:

Delphi V1.00
Borland C/C++ 3.1 or 4.0
Microsoft C/C++ 6.0 or 7.0
Borland Pascal / Turbo Pascal Version 6.0 or 7.0

5.1) Board Handles

All EDR functions used above require a board handle as the first parameter. The board handle defines which board is affected by the function call. Using this method has several advantages, For example, there is no need for a 'select board' function; working with parallel boards is much easier; different applications using the EDR at the same time will not conflict with each other.

Board handle are integers obtained by calling EDR_AllocBoardHandle (see 7.2 of EDR Developers Toolkit). Once allocated a board handle must be initialised to the PC 66C before it can be accessed. this is achieved by calling EDR_InitBoard or EDR_InitBoardType (see 7.5 of EDR manual) with the base address or EDR_loadConfiguration (see section 7.8 of EDR manual).

EDR_InitBoard will attempt to detect the PC66C at the base address specified.

5.2) Interrupt functions

Since an optically isolated external trigger line on the PC 66C is connected to a hardware interrupt, an ISR can be installed using the EDR driver functions to obtain external triggering in the background.

These functions are only callable from virtually an programming language. See the EDR Software Developers Kit Reference Manual.

5.3) Quick Function Reference

The PC 66C 8/12 channel D/A Board utilises the following functions calls contained in the EDR driver developers toolkit. They are:

Function Name	Description
EDR_AddToDAChanList	Adds a channel to the end of the channel list increasing its length by 1
EDR_BackgroundDAOutStatus	Function is not support by this version of EDR
EDR_BackGroundDAOutType	Function is not support by this version of EDR
EDR_DAOutBin	Generates a waveform on one or more D/A channels.
EDR_OutBinBackground	N/A
EDR_OutBinOneSample	Sets the voltage on the specified D/A channel using a binary voltage
EDR_DAOutBinReadback	Getsthe last voltage set on the specified D/A channel in binary form
EDR_OutBinToVoltage	Converts a single binary voltage for a DAC into microvolt value
EDR_DAOutUpdate	Updates the voltages on all D/A channels programmed for parallel (preload) update
EDR_DAOutVoltage	Sets the voltage on the specified D/A channel using a microvolt value
EDR_DAOutVoltageReadback	Gets the last voltage set on the specified D/A channel as a microvolt value
EDR_DAOutVoltageToBin	Converts a microvolt value for a specific DAC into a binary value for the DAC
EDR_DAOutVoltageToBinBlock	Converts microvolt waveforms into binary waveforms ready for EDR_DAOutBin.
EDR_GetDAChanListIndex	Gets an entry from the channel list
EDR_GetDAChanListLen	Gets the number of channels currently present in the channel list
EDR_GetDADisableAllInts	Gets that status of hte disable all ints flag
EDR_GetDAKeyAbort	Gets the status of the key abort flag
EDR_GetDATransferMode	Gets the current D/A transfer mode
EDR_SetDAChanListIndex	Changes the specified entry in the channel list
EDR_SetDAChanListLen	Sets the number of channels in the boards channel list
EDR_SetDADisableAllInts	Changes the disable all interrupt flag for waveform generation.

Function Name	Description
EDR_SetDAKeyAbort	Changes the key abort flag for waveform generation
EDR_SetDATransferMode	Changes the transfer mode used bythe waveform generation functions
EDR_StopBackgroundDAOut	This function is not supported by EDR
EDR_ValidDATransferMode	Checks the validity of the transfer mode given the current board setup
EDR_InstallISR	Installs an ISR for the specified hardware interrupt request
EDR_UninstallISR	Removes an interrupt service routine that was installed with EDR_InstallISR
EDR_InstallBoardISR	Installs an ISR for a particular type of interrupt installed on the PC 66C.
EDR_UninstallBoardISR	Removes an interrupt service routine that was installed with EDR_InstallBoardISR
EDR_MaskIRQ	Masks or unmasks a particular IRQ level
EDR_MaskBoardIRQ	Masks or unmasks a particular board interrupt
EDR_EnableInterrupt	Enables / disables a specified interrupt on hte PC 66C
EDR_ResetInterrupt	Sends an EOI command to one of the PCs interrupt controllers on completion of the interrupt
EDR_AllocBoardHandle	Allocates a new board handle to the PC 66C. If no board handles are available then a 0 is returned. This is particularly useful is multiple PC 66C are present in the same.computer.
EDR_FreeBoardHandle	Releases a board handle allocated to the PC 66C making it available to any other PC card
EDR_InitBoardType	Initialises a board and allocates a board handle to it
EDR_ConfigDialog	Diplays a dialog box that allows the user to manually configure the driver for the Board in the computer

Function Name	Description
EDR_SaveConfiguration	Function writes configuration information to a file for later loading with EDR_LoadConfiguration
EDR_LoadConfiguration	Loads details of the Cards configuration from the file created by EDR_SaveConfiguration
EDR_RestoreDefaults	Restores factory default configuration for a baord attached to a handle
EDR_IsBaseAddressInUse	Checks if any board initialised with EDR is using the specified I/O address
EDR_DetectBoard	Tries to determine the type of board present at a specified I/O address.
EDR_SetBoardType	Changes the board type attached to a board handle
EDR_SetIRQLevel	Set the IRQ level EDR will use for the interrupt ID specified.
EDR_SetIRQLevel	Set the IRQ level EDR will use for the interrupt ID specified.

Chapter 6: Testing and Calibrating the PC 66C

Before attempting to interface the PC 66C with your application, it is essential that you test the board first. This is done using the following Procedure:

6.1) Testing the PC 66C Board

Install the PC 66C using the procedure described in the Chapter 2: Installation. Proceed as follows:

- Switch the Computer on .
- On the DOS prompt, go to the C:\EDR\TPAS\DEMOS\ sub-directory
- Run the VOLTGEN.EXE test program with parameter 300 where 300 is the base address of the PC 66C.

If an error message 'Board not found' appears on your screen then the PC 66C was not installed at that address. Try a different base address as specified in Apendix A (eg: 700h) and re-run the test S/W. If the problem persists then try increasing the wait states on the PC 66C Board and re-run test software. The board should work.

If the PC 66C is found, a message will appear on the screen: 'PC 66C Board found'. The program will interactively allow you to set the voltage on a specific DAC.

6.2) Calibrating the PC 66C Board

6.2.1) Introduction

This procedure should be performed at six month intervals or whenever the input range jumpers are changed.

> ☞ **Note**
>
> Before attempting to calibrate the PC 66C Board, allow the host PC and the PC 66C to warm up for at least 10min before calibration

A/D calibration is performed by adjusting:

a) The Reference Voltage (for all DACs) [VR37]
b) The offset of the Op-amp [eg: For DAC0 it is VR5]
c) The Offset of the DAC [eg: For DAC0 it is VR1]
d) The Gain of the DACgain [eg: For DAC0 it is VR4]

These trimpots are easily located from the board layout as shown in Appendix B. Note that you can use the silkscreen text on the PC 66C as a reference.

a) Requirements

i) Calibration is done on all the channels. If the current sense inputs are not used then connect these pins to the relevant DAC.

ii) Calibration is performed with the board jumpered into its intended operating mode.

iii) All cables should be as short as possible.

b) Equipment required

i) Precision voltmeter with ±10V range and accurate to at least 1mV or better.

c) Procedure

1) Setting the reference Voltage

i) Connect a DVM on one terminal of L1 (inductor) on the PC 66C and analog ground.
ii) Adjust VR37 until the required reference voltage is reached (default is -5.050V). VR37 voltage range is between -4.5V to -10.5V.

> ☞ **Note**
>
> The reference voltage Vref must be set to a voltage 50mV lower than the desired maximum output voltage of the DACs. This is needed to allow a symmetrical calibration range of ±50mV in each DAC channel (with Pots VR1 and VR4). For example, if the maximum output voltage is to be 5.000V then set Vref to -5.050V. This is also the default setting of Vref.

2) Calibrating the DACs Outputs (Monopolar and Bipolar)

i) Run the PC66.EXE program found in the C:\EDR\C\DEMOS directory. Follow the on screen instructions carefully.

ii) The software will apply +5.000V (or +Vref-50mV) to the DACs (assuming Vref = 5.050V). Connect a DVM across pins 2 and 3 of U13 and adjust the offset trimpot VR5 until 0.00mV is shown.

iii) Next step is to adjust the Offset voltage of the DACs. The Software will set the DAC output voltage to +5.000V. Connect a DVM across the DAC channels and analog ground. Adjust VR4 until +5.000V is obtained.

iv) Next step is to adjust the Gain of the DACs. The Software will set the DAC output voltage to -5.000V. Connect a DVM across the DAC channels and analog ground. Adjust VR1 until -5.000V is obtained.

Repeat iii) and iv) until no further adjustment is required.

> ☞ **Note**
>
> Repeat steps ii) thru iv) for each DAC channel. Table for the exact Trimpots are given below

DAC No	Op-amp Offset	+Full Scale	-Full Scale
DAC 0	VR5	VR4	VR1
DAC 1	VR6	VR3	VR2
DAC 2	VR11	VR9	VR7
DAC 3	VR12	VR10	VR8
DAC 4	VR17	VR15	VR13
DAC 5	VR18	VR16	VR14
DAC 6	VR23	VR19	VR21
DAC 7	VR24	VR20	VR22
DAC 8	VR29	VR25	VR26
DAC 9	VR30	VR27	VR28
DAC 10	VR35	VR31	VR32
DAC 11	VR36	VR33	VR34

Table 6.2) DAC Pot Calibration Table

Chapter 7: Troubleshooting

Problem: 'Board not found' message appears on the screen when running test software.

Solution: Another I/O card might be using the same base address location as the PC 66C. Try a different base address other than the manufacturers default base address (eg: 700h) and re-run test software. If the problem persists then try increasing the wait states on the PC 66C. If the PC 66C still does not work even after the maximum number of wait states was chosen then try a different computer. If the test still fails then the PC 66C is faulty. Return the board to your distributor for repairs.

Problem: DAC output Voltage in bipolar mode is constant at 10.6V (or -10.6V) with no change in its output as soon as the DAC data is written.

Solution: Check if you are using the current sense facility. If not then you must connect the current sense input lines to the appropriate DAC. Run VOLTGEN.EXE found in the C:\EDR\PASCAL\DEMOS subdir and set the DAC output voltage to 1.000V. The reading on the output connector should be correct.

Problem: Parallel trigger facility does not work. DACs voltage changes as soon as the lower 4 LSBs are written.

Solution: Check if the parallel trigger jumpers (J3 to J14) are set correctly. To enable parallel trigger, you must short 1-2 on the appropriate DAC jumper. Rerun VOLTGEN.EXE found in the C:\EDR\PASCAL\DEMOS subdir and set the DAC output voltage to 1.000V. The output should not change until you have written a 0 to the correct bit in the parallel trigger register.

Problem: Interrupts does not occur when the Opto-Isolator receives a pulse from 0V to above the threshold of 3.1V. In other words a square pulse Posituve edged 0 to 5V does not yield an interrupt.

Solution: First read back Bit 2 [IRQSET] in the IEN Register [Base + 19] and check if the bit is high. If so then an interrupt has occurred. Check if you have enabled the Interrupt Bit (IRQEN) in the IEN Register by reading back bit 0 [IRQEN] in the IEN Register [Base + 19]. If not then the Interrupts will not occur because the tri-state buffer is disabled. Set this bit (Bit 0) to 1 in order to enable Interrupts. For reference, see Chapter 3, Section 3.4.

If you have enabled the IRQEN bit, then check whether the IRQ line that you used is not also used by another Card in your computer. If so, then

change the IRQ Jumper (JM1) to another IRQ line. Interrupts should occur after these changes are made.

☞ Warning

Any parts replaced on the PC 66C must be done by a qualified or trained technician. If you (the user) is not a trained technician then rather return the board to your distributor for repairs explaining in detail what the problem is.

If you cannot solve the problem then simply call your distributor for immediate help.

Chapter 8: Repair Service

The PC 66C is guaranteed for a period of 1 year. If the board is faulty within this period, we will gladly repair it free of charge provided that the maximum specifications was not exceeded. If any burn't tracks are seen on the PC 66C Board, warranty will be void. A repair charge will be levied in the user requires the board to be repaired.

Before sending the board to your distributor for repairs, ensure that you go through Chapter 7: TroubleShooting Hints thoroughly. If, after you have gone through this Chapter, the board still does not work, return it for repairs stating in detail what the problem is.

Our repair service centre will be available to repair our products even after the 1 year warranty. A small service fee will be levied which usually covers the cost of the components that are faulty.

Specifications

Computer Host Interface

Base Address:	Switchable from 0 to 1FE0h in 32 byte boundaries
Bus Type:	XT, AT, ISA or EISA
I/O Wait States:	0, 2, 4, or 8 Jumper selectable.
Number of Registers:	Thirty Two 8-bit
Interrupts:	Jumper selectable from IRQ 2 thru IRQ7

Analog Outputs

✱ *No. of Output Channels:*	12 Bipolar and 8 Monopolar
✱ *Resolution:*	12 bits, 1 in 4096
✱ *Total System Accuracy:*	± 1 LSB (depending on enviromental conditions)
✱ *Differential Nonlinearity:*	±1 LSB
✱ *Quantization Uncertainty:*	±½ LSB
✱ *Reference Voltage:*	Adjustable from 4.900V to 10.100V;
✱ *Output Ranges:*	Adjustable (depends on Reference Voltage) Default (Vref = 5.050V): ±5V, 0 to 5V
✱ *Gain Error:*	Adjustable to zero
✱ *Offset Error:*	±0.2LSB after calibration
✱ *Gain Drift:*	±30 ppm/°C
✱ *Acquisition Rate:*	130Khz max
✱ *DAC Settling Time:*	2µS
✱ *Output compliance:*	±5mA
✱ *Monotonicity*	0 to 50°C

Optical Trigger Input

✱ *Input voltage:*	0 to 3V	logical low
	3.1V to 24V	logical high
✱ *Max reverse voltage:*	400V peak	
✱ *Max input current:*	1A peak	
	30mA continuous	
✱ *Signal frequency response:*	10kHz	
✱ *Interrupt link:*	Jumper selectable from IRQ2 thru IRQ7	

I/O Connector

✱ *DAC Outputs; Trigger Input:*	DB37 female connector

Enviromental

✱ *Operating temperature:*	0°C to 55°C
✱ *Storage temperature:*	-55°C to 150°C
✱ *Relative humidity:*	5% to 90% non-condensing
✱ *PC Board size:*	200mm x 103mm

Power Supply Requirements

✱ *+5V Supply: :*	600mA typ
✱ *+12V Supply:*	100mA typ
✱ *-12V Supply:*	100mA typ

Appendix A

Base Address Switch Settings

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
00	ON	ON	ON	ON	ON	ON	ON	ON	00
20	ON	ON	ON	ON	ON	ON	ON	OFF	20
40	ON	ON	ON	ON	ON	ON	OFF	ON	40
60	ON	ON	ON	ON	ON	ON	OFF	OFF	60
80	ON	ON	ON	ON	ON	OFF	ON	ON	80
A0	ON	ON	ON	ON	ON	OFF	ON	OFF	A0
C0	ON	ON	ON	ON	ON	OFF	OFF	ON	C0
E0	ON	ON	ON	ON	ON	OFF	OFF	OFF	E0
100	ON	ON	ON	ON	OFF	ON	ON	ON	100
120	ON	ON	ON	ON	OFF	ON	ON	OFF	120
140	ON	ON	ON	ON	OFF	ON	OFF	ON	140
160	ON	ON	ON	ON	OFF	ON	OFF	OFF	160
180	ON	ON	ON	ON	OFF	OFF	ON	ON	180
1A0	ON	ON	ON	ON	OFF	OFF	ON	OFF	1A0
1C0	ON	ON	ON	ON	OFF	OFF	OFF	ON	1C0
1E0	ON	ON	ON	ON	OFF	OFF	OFF	OFF	1E0
200	ON	ON	ON	OFF	ON	ON	ON	ON	200
220	ON	ON	ON	OFF	ON	ON	ON	OFF	220
240	ON	ON	ON	OFF	ON	ON	OFF	ON	240
260	ON	ON	ON	OFF	ON	ON	OFF	OFF	260
280	ON	ON	ON	OFF	ON	OFF	ON	ON	280
2A0	ON	ON	ON	OFF	ON	OFF	ON	OFF	2A0
2C0	ON	ON	ON	OFF	ON	OFF	OFF	ON	2C0
2E0	ON	ON	ON	OFF	ON	OFF	OFF	OFF	2E0
300	ON	ON	ON	OFF	OFF	ON	ON	ON	300
320	ON	ON	ON	OFF	OFF	ON	ON	OFF	320
340	ON	ON	ON	OFF	OFF	ON	OFF	ON	340
360	ON	ON	ON	OFF	OFF	ON	OFF	OFF	360
380	ON	ON	ON	OFF	OFF	OFF	ON	ON	380
3A0	ON	ON	ON	OFF	OFF	OFF	ON	OFF	3A0
3C0	ON	ON	ON	OFF	OFF	OFF	OFF	ON	3C0
3E0	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	3E0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
400	ON	ON	OFF	ON	ON	ON	ON	ON	400
420	ON	ON	OFF	ON	ON	ON	ON	OFF	420
440	ON	ON	OFF	ON	ON	ON	OFF	ON	440
460	ON	ON	OFF	ON	ON	ON	OFF	OFF	460
480	ON	ON	OFF	ON	ON	OFF	ON	ON	480
4A0	ON	ON	OFF	ON	ON	OFF	ON	OFF	4A0
4C0	ON	ON	OFF	ON	ON	OFF	OFF	ON	4C0
4E0	ON	ON	OFF	ON	ON	OFF	OFF	OFF	4E0
500	ON	ON	OFF	ON	OFF	ON	ON	ON	500
520	ON	ON	OFF	ON	OFF	ON	ON	OFF	520
540	ON	ON	OFF	ON	OFF	ON	OFF	ON	540
560	ON	ON	OFF	ON	OFF	ON	OFF	OFF	560
580	ON	ON	OFF	ON	OFF	OFF	ON	ON	580
5A0	ON	ON	OFF	ON	OFF	OFF	ON	OFF	5A0
5C0	ON	ON	OFF	ON	OFF	OFF	OFF	ON	5C0
5E0	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	5E0
600	ON	ON	OFF	OFF	ON	ON	ON	ON	600
620	ON	ON	OFF	OFF	ON	ON	ON	OFF	620
640	ON	ON	OFF	OFF	ON	ON	OFF	ON	640
660	ON	ON	OFF	OFF	ON	ON	OFF	OFF	660
680	ON	ON	OFF	OFF	ON	OFF	ON	ON	680
6A0	ON	ON	OFF	OFF	ON	OFF	ON	OFF	6A0
6C0	ON	ON	OFF	OFF	ON	OFF	OFF	ON	6C0
6E0	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	6E0
700	ON	ON	OFF	OFF	OFF	ON	ON	ON	700
720	ON	ON	OFF	OFF	OFF	ON	ON	OFF	720
740	ON	ON	OFF	OFF	OFF	ON	OFF	ON	740
760	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	760
780	ON	ON	OFF	OFF	OFF	OFF	ON	ON	780
7A0	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	7A0
7C0	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	7C0
7E0	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	7E0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
800	ON	OFF	ON	ON	ON	ON	ON	ON	800
820	ON	OFF	ON	ON	ON	ON	ON	OFF	820
840	ON	OFF	ON	ON	ON	ON	OFF	ON	840
860	ON	OFF	ON	ON	ON	ON	OFF	OFF	860
880	ON	OFF	ON	ON	ON	OFF	ON	ON	880
8A0	ON	OFF	ON	ON	ON	OFF	ON	OFF	8A0
8C0	ON	OFF	ON	ON	ON	OFF	OFF	ON	8C0
8E0	ON	OFF	ON	ON	ON	OFF	OFF	OFF	8E0
900	ON	OFF	ON	ON	OFF	ON	ON	ON	900
920	ON	OFF	ON	ON	OFF	ON	ON	OFF	920
940	ON	OFF	ON	ON	OFF	ON	OFF	ON	940
960	ON	OFF	ON	ON	OFF	ON	OFF	OFF	960
980	ON	OFF	ON	ON	OFF	OFF	ON	ON	980
9A0	ON	OFF	ON	ON	OFF	OFF	ON	OFF	9A0
9C0	ON	OFF	ON	ON	OFF	OFF	OFF	ON	9C0
9E0	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	9E0
A00	ON	OFF	ON	OFF	ON	ON	ON	ON	A00
A20	ON	OFF	ON	OFF	ON	ON	ON	OFF	A20
A40	ON	OFF	ON	OFF	ON	ON	OFF	ON	A40
A60	ON	OFF	ON	OFF	ON	ON	OFF	OFF	A60
A80	ON	OFF	ON	OFF	ON	OFF	ON	ON	A80
AA0	ON	OFF	ON	OFF	ON	OFF	ON	OFF	AA0
AC0	ON	OFF	ON	OFF	ON	OFF	OFF	ON	AC0
AE0	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	AE0
B00	ON	OFF	ON	OFF	OFF	ON	ON	ON	B00
B20	ON	OFF	ON	OFF	OFF	ON	ON	OFF	B20
B40	ON	OFF	ON	OFF	OFF	ON	OFF	ON	B40
B60	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	B60
B80	ON	OFF	ON	OFF	OFF	OFF	ON	ON	B80
BA0	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	BA0
BC0	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	BC0
BE0	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	BE0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
C00	ON	OFF	OFF	ON	ON	ON	ON	ON	C00
C20	ON	OFF	OFF	ON	ON	ON	ON	OFF	C20
C40	ON	OFF	OFF	ON	ON	ON	OFF	ON	C40
C60	ON	OFF	OFF	ON	ON	ON	OFF	OFF	C60
C80	ON	OFF	OFF	ON	ON	OFF	ON	ON	C80
CA0	ON	OFF	OFF	ON	ON	OFF	ON	OFF	CA0
CC0	ON	OFF	OFF	ON	ON	OFF	OFF	ON	CC0
CE0	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	CE0
D00	ON	OFF	OFF	ON	OFF	ON	ON	ON	D00
D20	ON	OFF	OFF	ON	OFF	ON	ON	OFF	D20
D40	ON	OFF	OFF	ON	OFF	ON	OFF	ON	D40
D60	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	D60
D80	ON	OFF	OFF	ON	OFF	OFF	ON	ON	D80
DA0	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	DA0
DC0	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	DC0
DE0	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	DE0
E00	ON	OFF	OFF	OFF	ON	ON	ON	ON	E00
E20	ON	OFF	OFF	OFF	ON	ON	ON	OFF	E20
E40	ON	OFF	OFF	OFF	ON	ON	OFF	ON	E40
E60	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	E60
E80	ON	OFF	OFF	OFF	ON	OFF	ON	ON	E80
EA0	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	EA0
EC0	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	EC0
EE0	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	EE0
F00	ON	OFF	OFF	OFF	OFF	ON	ON	ON	F00
F20	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	F20
F40	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	F40
F60	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	F60
F80	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	F80
FA0	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	FA0
FC0	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	FC0
FE0	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	FE0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
1000	OFF	ON	ON	ON	ON	ON	ON	ON	1000
1020	OFF	ON	ON	ON	ON	ON	ON	OFF	1020
1040	OFF	ON	ON	ON	ON	ON	OFF	ON	1040
1060	OFF	ON	ON	ON	ON	ON	OFF	OFF	1060
1080	OFF	ON	ON	ON	ON	OFF	ON	ON	1080
10A0	OFF	ON	ON	ON	ON	OFF	ON	OFF	10A0
10C0	OFF	ON	ON	ON	ON	OFF	OFF	ON	10C0
10E0	OFF	ON	ON	ON	ON	OFF	OFF	OFF	10E0
1100	OFF	ON	ON	ON	OFF	ON	ON	ON	1100
1120	OFF	ON	ON	ON	OFF	ON	ON	OFF	1120
1140	OFF	ON	ON	ON	OFF	ON	OFF	ON	1140
1160	OFF	ON	ON	ON	OFF	ON	OFF	OFF	1160
1180	OFF	ON	ON	ON	OFF	OFF	ON	ON	1180
11A0	OFF	ON	ON	ON	OFF	OFF	ON	OFF	11A0
11C0	OFF	ON	ON	ON	OFF	OFF	OFF	ON	11C0
11E0	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	11E0
1200	OFF	ON	ON	OFF	ON	ON	ON	ON	1200
1220	OFF	ON	ON	OFF	ON	ON	ON	OFF	1220
1240	OFF	ON	ON	OFF	ON	ON	OFF	ON	1240
1260	OFF	ON	ON	OFF	ON	ON	OFF	OFF	1260
1280	OFF	ON	ON	OFF	ON	OFF	ON	ON	1280
12A0	OFF	ON	ON	OFF	ON	OFF	ON	OFF	12A0
12C0	OFF	ON	ON	OFF	ON	OFF	OFF	ON	12C0
12E0	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	12E0
1300	OFF	ON	ON	OFF	OFF	ON	ON	ON	1300
1320	OFF	ON	ON	OFF	OFF	ON	ON	OFF	1320
1340	OFF	ON	ON	OFF	OFF	ON	OFF	ON	1340
1360	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	1360
1380	OFF	ON	ON	OFF	OFF	OFF	ON	ON	1380
13A0	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	13A0
13C0	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	13C0
13E0	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	13E0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
1400	OFF	ON	OFF	ON	ON	ON	ON	ON	1400
1420	OFF	ON	OFF	ON	ON	ON	ON	OFF	1420
1440	OFF	ON	OFF	ON	ON	ON	OFF	ON	1440
1460	OFF	ON	OFF	ON	ON	ON	OFF	OFF	1460
1480	OFF	ON	OFF	ON	ON	OFF	ON	ON	1480
14A0	OFF	ON	OFF	ON	ON	OFF	ON	OFF	14A0
14C0	OFF	ON	OFF	ON	ON	OFF	OFF	ON	14C0
14E0	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	14E0
1500	OFF	ON	OFF	ON	OFF	ON	ON	ON	1500
1520	OFF	ON	OFF	ON	OFF	ON	ON	OFF	1520
1540	OFF	ON	OFF	ON	OFF	ON	OFF	ON	1540
1560	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	1560
1580	OFF	ON	OFF	ON	OFF	OFF	ON	ON	1580
15A0	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	15A0
15C0	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	15C0
15E0	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	15E0
1600	OFF	ON	OFF	OFF	ON	ON	ON	ON	1600
1620	OFF	ON	OFF	OFF	ON	ON	ON	OFF	1620
1640	OFF	ON	OFF	OFF	ON	ON	OFF	ON	1640
1660	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	1660
1680	OFF	ON	OFF	OFF	ON	OFF	ON	ON	1680
16A0	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	16A0
16C0	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	16C0
16E0	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	16E0
1700	OFF	ON	OFF	OFF	OFF	ON	ON	ON	1700
1720	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	1720
1740	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	1740
1760	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	1760
1780	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	1780
17A0	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	17A0
17C0	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	17C0
17E0	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	17E0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Addres
1800	OFF	OFF	ON	ON	ON	ON	ON	ON	1800
1820	OFF	OFF	ON	ON	ON	ON	ON	OFF	1820
1840	OFF	OFF	ON	ON	ON	ON	OFF	ON	1840
1860	OFF	OFF	ON	ON	ON	ON	OFF	OFF	1860
1880	OFF	OFF	ON	ON	ON	OFF	ON	ON	1880
18A0	OFF	OFF	ON	ON	ON	OFF	ON	OFF	18A0
18C0	OFF	OFF	ON	ON	ON	OFF	OFF	ON	18C0
18E0	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	18E0
1900	OFF	OFF	ON	ON	OFF	ON	ON	ON	1900
1920	OFF	OFF	ON	ON	OFF	ON	ON	OFF	1920
1940	OFF	OFF	ON	ON	OFF	ON	OFF	ON	1940
1960	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	1960
1980	OFF	OFF	ON	ON	OFF	OFF	ON	ON	1980
19A0	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	19A0
19C0	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	19C0
19E0	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	19E0
1A00	OFF	OFF	ON	OFF	ON	ON	ON	ON	1A00
1A20	OFF	OFF	ON	OFF	ON	ON	ON	OFF	1A20
1A40	OFF	OFF	ON	OFF	ON	ON	OFF	ON	1A40
1A60	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	1A60
1A80	OFF	OFF	ON	OFF	ON	OFF	ON	ON	1A80
1AA0	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	1AA0
1AC0	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	1AC0
1AE0	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	1AE0
1B00	OFF	OFF	ON	OFF	OFF	ON	ON	ON	1B00
1B20	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	1B20
1B40	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	1B40
1B60	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	1B60
1B80	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	1B80
1BA0	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	1BA0
1BC0	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	1BC0
1BE0	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	1BE0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
1C00	OFF	OFF	OFF	ON	ON	ON	ON	ON	1C00
1C20	OFF	OFF	OFF	ON	ON	ON	ON	OFF	1C20
1C40	OFF	OFF	OFF	ON	ON	ON	OFF	ON	1C40
1C60	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	1C60
1C80	OFF	OFF	OFF	ON	ON	OFF	ON	ON	1C80
1CA0	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	1CA0
1CC0	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	1CC0
1CE0	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	1CE0
1D00	OFF	OFF	OFF	ON	OFF	ON	ON	ON	1D00
1D20	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	1D20
1D40	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	1D40
1D60	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	1D60
1D80	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	1D80
1DA0	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	1DA0
1DC0	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	1DC0
1DE0	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	1DE0
1E00	OFF	OFF	OFF	OFF	ON	ON	ON	ON	1E00
1E20	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	1E20
1E40	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	1E40
1E60	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	1E60
1E80	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	1E80
1EA0	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	1EA0
1EC0	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	1EC0
1EE0	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	1EE0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
1F00	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	1F00
1F20	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	1F20
1F40	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	1F40
1F60	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	1F60
1F80	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	1F80
1FA0	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	1FA0
1FC0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	1FC0
1FE0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	1FE0

Appendix B

EAGLE TECHNOLOGY
TITLE: PC 66C 8/12 CHANNEL D/A BOARD
TOP SILK

DATE: 31/7/96
FILENAME: RB66C9FM.PCB

DESIGNER: S. ALLIE