PC 36C

Enhanced 24 Channel Digital I/O Card

User's Manual

For the IBM PC/XT/AT, PS/2 386, 486, Pentiums, ISA and EISA computers

First Edition

December 1996

2 December 1996 Printing

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Introduction

The PC 36C is an enhanced parallel digital I/O interface board for the IBM PC/XT/AT, 486, Pentuim, ISA and EISA Computers. It provides 24 Digital I/O lines built around the industry standard 8255 type Programmable Peripheral Interface (PPI) adapter ICs.

The PC 36C fits into one of the IBM PC/AT 8 bit expansion slot.

Typical applications

- Industrial control
- Process Control
- Laboratory Automation
- Energy management
- Product testing

Key Features

- On-board wait state generation allows operation on high speed computers
- Provides 24 digital I/O channels configured in blocks of three 8 bits
- All 8255 PPI modes are supported for example:
  a) Simple inputs and outputs
  b) Strobed inputs and outputs with handshaking
  c) Bidirectional input/output with handshaking
- Interrupt level for each PPI selectable from IRQ2 thru IRQ15
- Wide base address selection range so that multiple boards can be paralleled
- Latched External Trigger Interrupt Line available to directly toggle the interrupt system
- EDR Driver software libraries for C, Pascal, Qbasic Basic and Visual Basic is provided for easy programming.
- EDR Driver software libraries (DLL) for Windows V3.11 or Win95 are included
- Third Party Software like LabView for Windows, LabTech Notebook, DasyLab and TestPoint are also provided.

PC 36C Package

The PC 36C package consists of:

- PC 36C Interface Card
- PC 36C User's Manual
- EDR Developers Toolkit User Manual + 5¼ or 3½' diskette
- One 5¼' OR 3½' diskette containing the PC 36C drivers and demonstration software

If any of the items is missing, contact your dealer immediately specifying which components are missing.

Chapter 1: Installation

There are two aspects of the PC 36C that must be configured:

1.1) Setting the base address

This address determines where the board is accessed. This can be set by a 8-way DIP switch found on the PC 36C Board. The address range are from 0 to 1fffh.

The PC 36C occupies a block of 64 consecutive I/O addresses. The base address setting controls where the block starts. This base address must be unique to the PC 36C only and no other card must occupy this address. If multiple PC 36C boards are installed in one computer then each board must have a different base address.

The base address can be assigned to any location from 0 to 1fffh in 64 byte boundaries. Table 1 shows the I/O addresses occupied by standard interface cards. Refer to the Base Address Setting Table in Appendix A for a list of the various base address settings that the PC 36C can occupy.

The base address setting can be set by adjusting the 8-way dip switch on the PC 36C. Each line on the DIP switch switch compares an address line in I/O space. Switch number 1 compares address line A13; switch number 2: address A12 while switch number 8 compares address line A6. Factory default setting is 300h

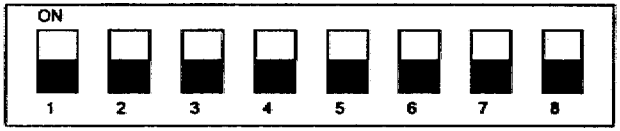
If one of the switches are OFF, then it contributes to the base address. An example is as follows:

```
Base Address   =    Switch 2 (Addr A9) + Switch 3 (addr A8)
               =    200 + 100
               =    300h
```

Table 1: Addresses for standard I/O devices

Address	Standard device
000-1FF	Internal system board
200-20F	Games port
210-217	Expansion unit
220-24F	Reserved
250-257	Not assigned
258-25F	Intel 'Above Board'
260-277	Not assigned
278-26F	Reserved
280-2EF	Not assigned
2F0-2F7	LPT2
2F8-2FF	COM2
300-31F	Prototype Board
320-32F	Hard Disk
330-377	Not assigned
378-37F	LPT1
380-38F	SDLC communications
390-39F	Not assigned
3A0-3AF	Binary comms
3B0-3BF	Mono Display Adaptor
3C0-3CF	Reserved
3D0-3DF	CGA
3E0-3E7	Reserved
3E3-3EF	Not assigned
3F0-3F7	Floppy disk
3F8-3FF	COM1
400-FFF	Not used see below

Table 1: Standard I/O Addresses



400	200	100	80	40	20	10	8	Hex Weight when OFF
A10	A9	A8	A7	A6	A5	A4	A3	Corresponding Address line

Figure 1: Dip Switch Address Weight (in Hex)

Note that addresses from 400h-7FFh cannot normally be used because these addresses are not normally decoded by some cards and I/O devices in the 0h to 3FFh range.

The PC 36C (and most other members of the PC-XX family) can use these address, if and only if the board at address 400h less than the address of the PC 36C also decodes the extra address.

For example, a PC 36C can be installed at address 300h and another one at address 700h (400h locations apart). However, it would not be advisable to install a PC 36C at address 7F8h. This is because communications port COM1 is installed at 3F8h and does not normally decode these extra addresses.

If your computer has boards not listed in Table 1 (such as LAN adaptors, back-up boards or other engineering boards), you should consult the User's Manual for these boards for information on the address ranges used.

In most cases, base address of 300h is a good choice. Address 300h is also the factory default base address setting.

1.2) Wait State Generation on the PC 36C

Some computers have very high I/O bus cycles. In this case it is neccessary to slow down these cycles when the computer accesses the PC 36C Board. Additional wait states can be set by means of a jumper on the PC 36C Board.

Additional wait states can be inserted in the I/O bus cycle by changing the jumper setting on JP1 on the PC 36C. This jumper is marked 'Wait State Jumper' on the PC 36C board. Refer to figure 1.2 for the wait state jumper settings. Note that the factory default setting is zero wait states.

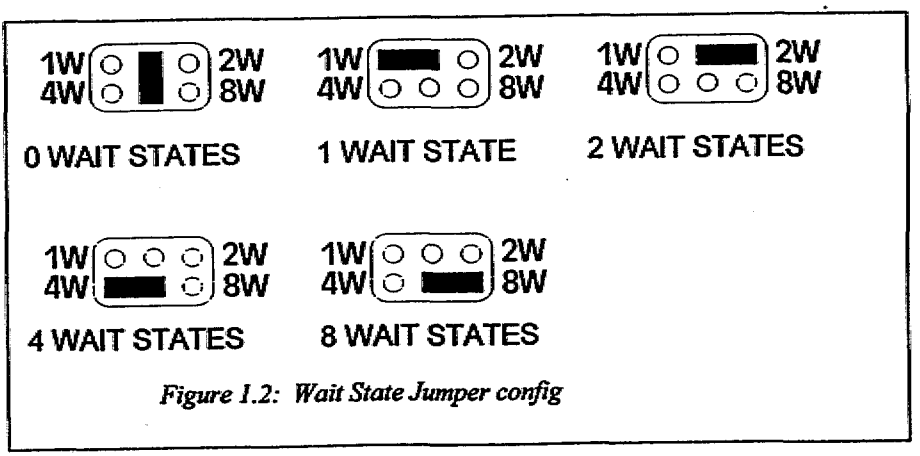


Figure 1.2: Wait State Jumper config

In most cases, only a very small number of computers require additional wait states. If the PC 36C seems to be giving incorrect results then try increasing the wait states until correct results are obtained. If the board still does not produce correct results even after the maximum number of wait states has been inserted then the PC 36C or the host computer are defective and should be serviced.

1.3) Port C0 and C3 Interrupt Jumper Settings (JP3 and JP4)

Jumpers on board the card selects an IRQ line for Port C0 and C3 of each 8255 PPI. This is normally applicable if the 8255 PPI is in mode 1 (strobed I/O) or Mode 2 (bidirectional data bus). You can use Port C0 and C3 in mode 0 as well. In this case Port C should be configured as inputs and the IRQ lines will be toggled externally (non-latched).

Two subsystems on the 8255 PPI are used to generate interrupts to the host computer. They are:

PIN FUNCTION	8255 PPI NO	DESCRIPTION
0INTRA	0 PORT C0	Port C0 of 1st 8255 PPI
0INTRB	0 PORT C3	Port C3 of 1st 8255 PPI

Table 1.3: Port Lines used to generate interrupts

The above interrupts are generated if the PPI is set to Mode 1. Full details on the function and use of the interrupts are given later in the manual.

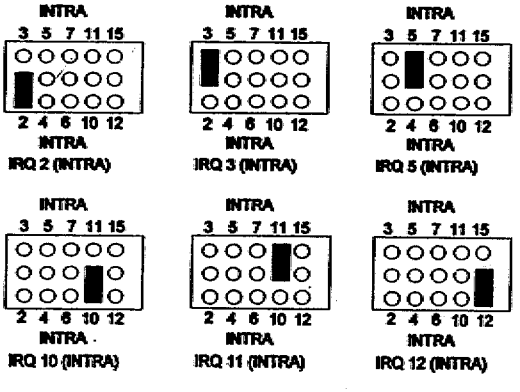


Figure 1.3a: Port C0 and C3 Interrupt jumper settings

Figure 1.3a shows the interrupt jumper settings [JP3] for INTRA of the PPI (ie: Port C0). Jumpers can also be placed on INTRB of the PPI (ie: Port C3) header [JP2] in order to link INTRB of the PPI (ie: Port C3) to the interrupt system.

In a standard PC, the interrupt levels are allocated as follows:

Level Level	Allocation
IRQ0	System timer
IRQ1	Keyboard
IRQ2/IRQ9	Display Adaptor
IRQ3	COM1 (if installed)
IRQ4	COM2 (if installed)
IRQ5	LPT2 (if installed)
IRQ6	Floppy disk controller
IRQ7	LPT1 (if installed)
IRQ10	Not used
IRQ11	Not used
IRQ12	Used by PS/2 Mouse (if installed)
IRQ13	Coprocessor
IRQ14	Primary IDE Harddisk (if installed)
IRQ15	Secondary IDE Harddisk (if installed)

Table 1.3b: Standard interrupt settings

On PC ATs, IRQ2 is used by the system board itself and any interrupt requests on IRQ is transparently rerouted to IRQ9.

The default IRQ setting on the PC 36C is IRQ5. Note that unless the interrupt line is specifically enabled by software, the interrupt output from the PC 36C is tri-stated (ie: not connected). It is also tri-stated upon power-up.

1.4) External Interrupt Jumper Settings (JP2)

If the external trigger interrupt option is used, then it is necessary to configure the interrupt jumper settings. Refer to figure 1.3b for the some examples of setting the interrupt jumper. Adhere to the Interrupt numbers placed on the silkscreen of the PC36C.

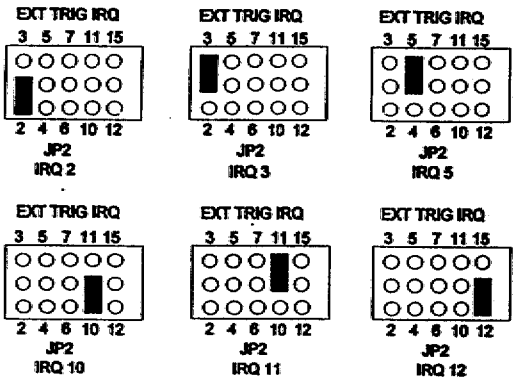


Figure 1.4a: External Interrupt jumper settings

1.5) Differential/Single-ended External Interrupt Jumper Setting

The optically isolated input line can be connected differentially or single ended. Figure 1.5 illustrates this graphically:

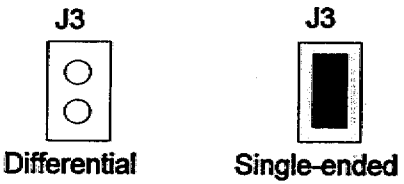


Figure 1.5a: Optically Isolated Input Diff/Single-ended Jumper Setting

Jumper J3 when enabled simply shorts the External Trigger Line Return to GND on the PC 36C Board.

1.6) Connecting the PC 36C to the PC Backplane

Requirements:
- XT/286/386/486, ISA, EISA, Pentium Computer
- Phillips Screw Driver (or one to match screw on the computer cabinet and bracket)
- 8 bit or 16 bit bus slot

Procedure:

a) Switch off the computer and all attached devices

b) Unplug power cord from the computer and all attached devices.

> ☞ **Warning**
>
> Failure to disconnect all power cables can result in harzardous conditions, as there may be dangerous voltage levels present in externally connected cables.

c) Remove the top cover from the PC. If you are not sure how to do this, consult the manual supplied with the system unit.

d) Choose any 8 or 16 bit expansion slot and remove the screw from the metal bracket fixed corresponding to the chosen slot.

e) Align the gold plated edge connector with the edge socket and the rear adaptor slot with the board bracket. Firmly press the board down into the socket on the computer's system board. Ensure that the board's edge connector is in the socket and has not slipped sideways past the socket.

f) Replace the screw on the bracket and tighten the screw to the back panel.

g) Replace the computer's cover. Plug in all cables and switch the computer power on. The PC 36C is now installed.

> ☞ **Note (IBM XT installation)**
>
> If you are installing the PC 36C in an XT then the interrupts 9 thru 15 will not be available for use.

CHAPTER 2: Interconnections

2.0) Introduction

The PC 36C 24 digital I/O board plugs into any ISA expansion slot at the gold finger edge connectors J1/J2 and J3/J4. The board communicates to the user circuit via IDE connectors mounted on the PC board. This chapter describes these connectors.

2.1) Connections to the IBM Bus

The PC 36C board may be plugged into any slot of the computer backplane with the exception of J8 slot of the IBM XTs. All data transfers to and from the host computer is channelled via this connectors.

2.2) PC36C User Connector

The PC 36C interfaces to the external world via a D-Type 37 way male connector.

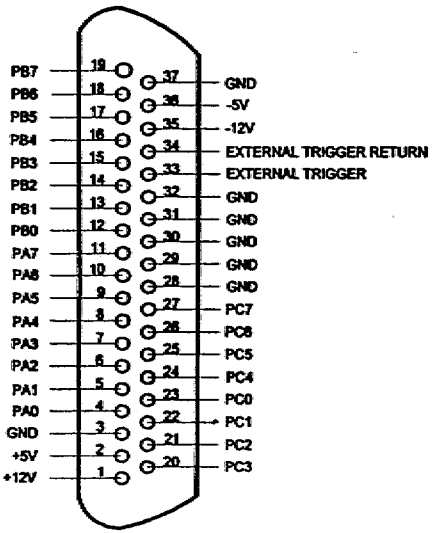


Figure 2.2: PC 36C Interface Connector (as seen from the rear of the PC)

Figure 4 graphically shows the connector together with their pin assignments. Note that the pin connections refer to the pin numbers of the connector when looking into the connector from the rear of the computer. Also note that the pin numbers are embossed on the connector itself.

2.3) Making Connections

The digital I/O lines on the PC 36C are directly compatible with most forms of TTL and CMOS logic operating from +5V supplies. Detailed specifications on the digital I/O lines are found in Appendix A: Specifications.

The ±5V, ±12V power lines are available on the connector. Precautionary measures should be taken when using these supplies.

> **☞ Warning**
>
> DO NOT exceed 5.1V or fall below 0V on the I/O ports of the PC36C. Permanent damage will result if these thresholds are exceeded.
>
> The maximum permissible current draw on the I/O connector for the ±5V and ±12V supplies are 100mA. Exceeding this can cause irreparable damage to the PC 36C and your computer.

2.4) 8255 PPI Port C Analysis

Some of Port C take on different meanings when the 8255 PPI is programmed to operate in strobed I/O or bidirectional bus mode. They are summarised below in table 2.4a.

Port C Line	Simple I/O Mode 0	Strobed Input Mode 1	Strobed Output Mode 1	Birectional Bus: Mode 2
C7	I/O	I/O	$/OBF_A$	$/OBF_A$
C6	I/O	I/O	$/ACK_A$	$/ACK_A$
C5	I/O	IBF_A	I/O	IBF_A
C4	I/O	$/STB_A$	I/O	$/STB_A$
C3	I/O	$INTR_A$	$INTR_A$	$INTR_A$
C2	I/O	$/STB_B$	$/ACK_B$	I/O
C1	I/O	IBF_B	$/OBF_B$	I/O
C0	I/O	$INTR_B$	$INTR_B$	I/O

Table 2.4a: Port C Line Usage

The symbol '/' indicates that a signal is active low.

When an 8255 PPI is used in on of the handshaking modes, the /STB and IBF lines are used to synchronise input data transfers. The /OBF and /ACK lines are used to synchronise the output data transfers. The signals in the table have the following functions:

Name	Type	Description
/STB	External Input	Strobe Input: A low on this handshaking line loads the data from the peripheral bus into the input latch.
IBF	External Output	Input Buffer Full: A high on this line indicates that the external data has been loaded into the input latch. This is an input acknowledge signal.
/ACK	External Input	Acknowledge: The external device asserts this line low to indicate that the data written to the port by the program has been accepted
/OBF	External Output	Output Buffer Full: The 8255 PPI asserts this line low to indicate to the external device that the program has written data to the selected port. This line can be used to strobe the data into the external device.
INTR	Internal Output	Interrupt Request: This signal becomes active high when the 8255 PPI is requesting service from the host computer. For input operations, it indicates that there is data in the corresponding port to be read by the program. For output operations, it indicates that the external devices has accepted the data and thus the program can write another byte to the 8255 PPI. An interrupt line must be selected with the interrupt jumpers and the appropriate interrupt enable bits must be set , both in the 8255 PPI and the interrupt enable register in order to allow this signal to reach the host computer.
/RD	Internal Input	Read Signal: This signal is generated by the control lines of the host computer. It is activated when the program executes an Input instruction from any of the PC 36C registers.
/WR	Internal Input	Write Signal: This signal is generated by the control lines of the host computer. It is activated when the program executes an Output instruction from any of the PC 36C registers.

Figure 2.4b: Port C Handshaking Lines

2.5) Power supply connections

The ±12V and ±5V power with digital ground are available on the DB37 Male Connector.

> **☞ Warning**
>
> The maximum permissible current draw on the ±5V and the ±12V lines on the I/O connector is 100mA. Exceeding this can cause irreparable damage to the PC 36C.

2.6) External Interrupt Trigger Line

This line can be used as an external interrupt trigger line to enable automatic shutdown/switch-on of the I/O lines. This line is optically isolated from the digital circuitry of the PC 36C. The output is connected to the interrupt line of the IBM bus via associated circuitry. Figure 2.6a illustrates the optically isolated connections:

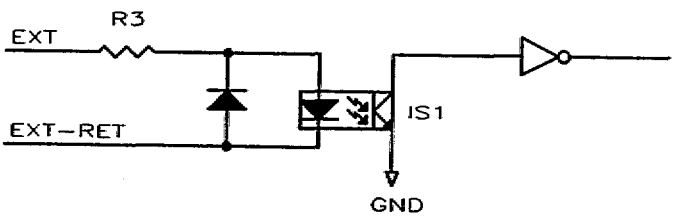


Figure 2.6a: Optically Isolated Trigger Line

Note that the External Trigger Return line can be connected to ground via jumper J3 if you wish. The default setting is enabled which hence connects the External Trigger Return to Digital Ground.

The signal should be fed into the DB37 connector on pins 33 (External Trigger Line) and 34 (External Trigger Return). A logical low pulse into the opto-isolator is defined from 0 to 2.9V. A logical high is defined from 3V to a max of 24V. Hence pulses from 0 to 24V will trigger the opto-isolator in generating a TTL pulse to enable the interrupt line.

CHAPTER 3: Register Structure

3.0) Introduction

At the lowest level, the PC 36C can be programmed using I/O input and output instructions. This chapter contains the information on all the PC 36C registers. Although programming the board is not difficult, it is time consuming and requires detailed knowledge of the PC 36C as well as the operation of the host PC and its operating system. In order to simplify the process, a set of driver libraries is provided. The use of these libraries allow access to all the board's functions and is described in Chapter 5: Programming guide.

The PC 36C occupies 8 consecutive addresses in the computer's I/O space. The layout of these registers are shown in Table 4: PC 36C register structure. The offset of the registeirs are given as offset addresses from the base address of the board. This base address is set with the Dip Switch as detailed in Chapter 2: Installation.

Offset	Read	Write
0	PPI 0: Port A (DIO0A)	PPI 0: Port A (DIO0A)
1	PPI 0: Port B (DIO0B)	PPI 0: Port B (DIO0B)
2	PPI 0: Port C (DIO0C)	PPI 0: Port C (DIO0C)
3	PPI 0: Control Register (DIO0CTL)	
4	Status Register (STATUS)	Interrupt Enable Register (IEN)
5		Interrupt Reset Register (IRES)

Table 4: PC 36C register structure

3.1) DIOA - Port A Register of first PPI (offset 0, read/write)

This register is port A of the first PPI. It can be operated in one of three modes. The operating mode is set by writing to the DIO0CTRL register, as described below.

DIOA Register (read/write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A7	0A6	0A5	0A4	0A3	0A2	0A1	0A0

Bit 0 thru 7: The bits 0A7 (MSB) down to 0A0 (LSB) reflect the status of Port A I/O lines. Depending on the programmed I/O mode of the port, the lines may be inputs, outputs or bidirectional.

3.2) DIOB - Port B Register of first PPI (offset 1, read/write)

This register is port B of the first PPI. It can be operated in one of three modes. The operating mode is set by writing to the DIO0CTRL register, as described below.

DIOB Register (read/write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B7	0B6	0B5	0B4	0B3	0B2	0B1	0B0

Bit 0 thru 7: The bits 0B7 (MSB) down to 0B0 (LSB) reflect the status of Port B I/O lines. Depending on the programmed I/O mode of the port, the lines may be inputs, outputs or bidirectional.

3.3) DIOC - Port C Register of first PPI (offset 2, read/write)

This register is port C of the first PPI. It can be operated in one of three modes. The operating mode is set by writing to the DIO0CTRL register, as described below.

DIOC Register (read/write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0C7	0C6	0C5	0C4	0C3	0C2	0C1	0C0

Bit 0 thru 7: The bits 0C7 (MSB) down to 0C0 (LSB) reflect the status of Port C I/O lines. Depending on the programmed I/O mode of the port, the lines may be inputs, outputs or bidirectional.

3.4) DIO0CTRL - Control register of the first PPI (offset 3, write only)

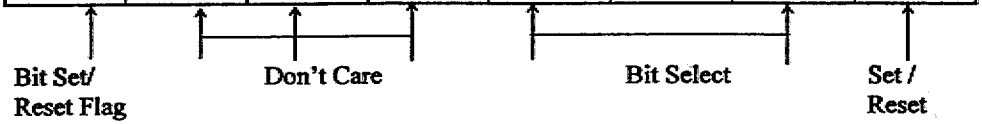
This register is used to control the operating modes of the first PPI or set and reset individual bits in port C of the PPI. The layout of the register is shown below. Note that the function and bit names of the register depend on the setting of bit 7.

DIO0CTL Register (write only) - Configuration Mode

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	MAS_1	MSA_0	PA	PCU	MSB_0	PB	PCL
Mode Set Flag	Group A Mode Selection		Port A I/O Direction	Port C Upper I/O direction	Group B Mode Selection	Port B I/O dir	Port C Lower I/O dir

DIO0CTL Register (write only) - Bit Set/Reset Mode

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	x	x	x	BS2	BS1	BS0	S/R



Bit 0 thru 7: Function Select: Setting this bit to 1 set the register in Configuration Mode. Writing a 0 to this bit configures this register in Set/Reset Mode.

The functions of the remaining bits are described below depending on the setting of bit 7:

3.4a) Configuration Mode

Bits 6-5: Group A mode select: These two bits set the mode of the Group A Ports. These are Port A and the upper four lines of port C. The bit combination are as follows:

MSA_1	MSA_0	Group A I/O Mode
0	0	Mode 0, simple I/O
0	1	Mode 1, Strobed I/O
1	x	Mode 2, Bidirectional bus

Bit 4: Port A I/O Direction: If this bit is set, then Port A functions as an input. If it is 0, then Port A is configured as an output.

Bit 3: Port C Upper I/O Direction: If this bit is set, then the upper four lines of Port C function as inputs. If the bit is 0, then the lines become outputs.

Bit 2: Group B Mode Select: This bit sets the mode of the group B ports. These are Port B and the lower four lines of Port C. The bit combinations are as follows:

MSB_0	Group B I/O Mode
0	Mode 0, Simple I/O
1	Mode 1, Strobed I/O

Bit 1: Port B I/O Direction: If this bit is set, then Port B functions as an input. If it is 0, then Port B is configured as an output.

Bit 0: Port C Lower I/O Direction: If this bit is set, then the lower four lines of Port C functions as inputs. If the bit is 0, then the lines become outputs.

> ☞ **Note**
>
> *Group B can only be used for simple or strobed I/O*

3.4b) Bit Set/Reset Mode

Bits 6-5: These bits have not effect in this function.

Bits 3-1: Bit Select: These bits select the bit in port C which is to be modified. A code of 000 selects Port C line 0 to set or reset. 001 selects line 1 and so on up to 111 which selects line 7.

Bit 0: Set/Reset: This bit specifies the state into which the selected Port C line will be placed. Writing a 1 will make the line go high and a 0 makes it go low. This operation has no effect on the other lines of Port C.

3.5) IEN0 - Interrupt / Status register 0 (offset 3: read/write)

This register contains control/status bits for enabling the interrupts from the 8255 PPIs (PPI0 thru PPI3) to the PC Bus. On power up or reset, all these bits are in a reset state. Hence all the Port lines are disabled from the PC bus.

IEN / STATUS Register (Write mode)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	EP1	EP0	0	IRQEN

IEN / STATUS Register (Read mode)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RES	RES	RES	TRIG	EP1	EP0	RES	IRQEN

Bit 0: Enable Interrupt from Optically Isolated Input line: Setting this bit to 1 enables the interrupt output from the External Trigger Line onto the PC bus. Writing a zero to this bit disables the Interrupt from the PC I/O channel.

Reading back these bits determines the status of the External Trigger Interrupt Enable Line.

Bit 1: Reserved for manufacturing tests. Write 0 to this bit in order to maintain future compatibility. Reading this bit is undefined.

Bit 2-3: Enable Interrupt from PPI0: Setting this bit to 1 enables the interrupt outputs (Port C0 and C3) from the second PPI on to the PC bus. With the PPI in mode 1 or mode 2, this electrically connects the $INTR_A$ and $INTR_B$ line to the selected interrupt lines of the host computer. Writing a zero to this bit disables the two Interrupts from the PC I/O channel. Bit 2 controls the interrupt line for Port C line 0 and Bit 3 controls the interrupt line for Port C Line 3.

Reading back these bits determines the status of the PPI interrupt enable lines (ie: Port C0 corresponds to Bit 0 and Port C3 corresponds to Bit 1).

☞ Additional External Interrupts

Note that the Port C0 and Port C3 lines are enabled onto the selected PC I/O Bus IRQ line bythe bit regardless of the mode setting of the 8255 PPI. This means that if Port C0 and C3 lines are not being used for digital I/O, they can be used as additional unlatched external interrupt inputs.

Bit 4: This bit reflects the status of the external trigger line. If this bit is set to a 0 then it means that the user input on the opto-isolator side is set low (between 0 to 3V). If the bit is set to 1 then the input to the opto-isolator is between 3.1 to 24V. Writing to this bit is undefined.

Bit 5-7: Reserved for manufacturing tests. Write 0 to these bits in order to maintain future compatibility. Reading these bits are undefined.

3.6) IRES - Interrupt Reset Register (offset 5: write only)

This register is used to clear the latched external interrupt.

IRES Register (Write mode)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
x	x	x	x	x	x	x	1

Bit 0: Writing a 0 to this bit clears the external interrupt latch thus resetting the external interupt line. Writing a 1 to this bit is undefined.

Bit 1-7: These bits have no effect on the function of the register. Zeros should be written to these bits for future compatibility.

Chapter 4: Programming Guide

4.0) Introduction

This chapter describes programming the PC 36C at its lowest level. In order to accomplish this, detailed knowledge of chapter 4 and the system hardware is required.

As an alternative to low level programming, driver software is provided with the PC 36C. This is described in Chapter 5.

The advantages of using the driver software are:

a) Detailed knowledge of the PC 36C is not required.
b) The Driver Libraries supports multiple boards. In other words, you can cascade boards in the same computer.
c) The Driver Library is callable from most high level languages.

Programmers who need to incorporate special routines into their application will need to read this chapter. Examples are application programs written in Clarion, Clipper, etc.

Once the PC 36C has been installed into the computer and external connections are made, the board is in an operational state. The PC 36C occupies 64 consecutive I/O addresses starting from the board's base address. The base address is set by the DIP Switch on the PC 36C. Programming the PC 36C is done by using the input/output instructions. Reading and writing to these addresses allows data to be moved to and from the PC 36C.

Reading and writing to these ports typically takes on the form of one of the following instructions:

Language	Port Read	Port Write
'C'	value = inp(addre);	outp(addre, value);
Pascal	value := port[addre];	port[addre] := value;

Assembly	mov al, value
	mov dx, addre
	in al, dx
		mov al, value
		mov dx, addre
		out dx, al

where: addre is the I/O location of the PC 36C registers
value is the byte read or written to the register

4.1) Programming the 8255 PPI

The 8255 PPI is a general purpose peripheral interface having 24 programmable I/O lines. The 24 lines are divided into three separate 8-bit ports (ie: Port A, Port B and Port C). The ports may be programmed either as two groups of 12 lines (group A and Group B) or as three individual 8 bit ports. The ports/groups may be operated in three modes: simple I/O, strobed I/O and bidirectional I/O. the 8255 PPI also has a single bit Set/Reset feature for port C.

Before any I/O can be done, the mode and direction of the ports/groups of the 8255 PPI must be set. This is done simply by writing on byte of configuration information to the control register (8255 PPI Base + 3). The 8255 PPI then operates in a specific mode until it is reset or new configuration information is written to the control register. The format of the register is shown below:

DIO0CTL Register (write only) - Configuration Mode

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	MAS_1	MSA_0	PA	PCU	MSB_0	PB	PCL
Mode Set Flag	Group A Mode Selection		Port A I/O Direction	Port C Upper I/O direction	Group B Mode Selection	Port B I/O dir	Port C Lower I/O dir

Bit 7 of the DIO0CTL Register must be set when programming the configuration of the 8255 PPIs. The mode is set for each of two groups of the 8255 PPI and the direction is set for individual ports. Note that the direction of Port C is independently programmable in two 4 line nibbles.

4.2) Mode 0: Simple I/O

This mode is used for simple input and output operatons for each of the ports. No handshaking is required and no interrupts are generated. Data is simply read from or written to a selected port.

The following characterise Mode 0:

- Two 8 bit ports (port A and Port B) and two 4-bit nibbles (upper and lower nibble of port C).
- Any port can be configured for input or output
- Outputs are latched, inputs are not latched.
- Data transfer by polled I/O.

Mode 0 Programming

To use the 8255 in mode 0:

i) Write a single byte to the control register to set the 8255 PPI into mode 0 with the three ports configured for the desired data direction.
ii) Read or write from the I/O port corresponding to an 8255 PPI port (Port A, B or C) as many times as necessary to obtain or transfer the required amount of data.

4.3) Mode 1: Strobed I/O

In this mode data transfers are controlled by handshaking signals and hardware interrupts. Some of the port C lines are used for these control signals. Hence they take on a different functions and names. Refer to Chapter 3: Register Structure for an in depth analysis of the bit functions.

The following characterise Mode 1:

* Two groups, Group A and B. Each group consists of an 8 bit data port and three control lines.
* Certain Port C lines take on special functions.
* The data ports can be either input or output ports.
* Both inputs and outputs are latched.
* One 20 bit simple I/O Port
* Data transfer by interrupts or polled I/O.

With both groups configured in mode 1, a single 8255 PPI can be read or write data 16 bits wide.

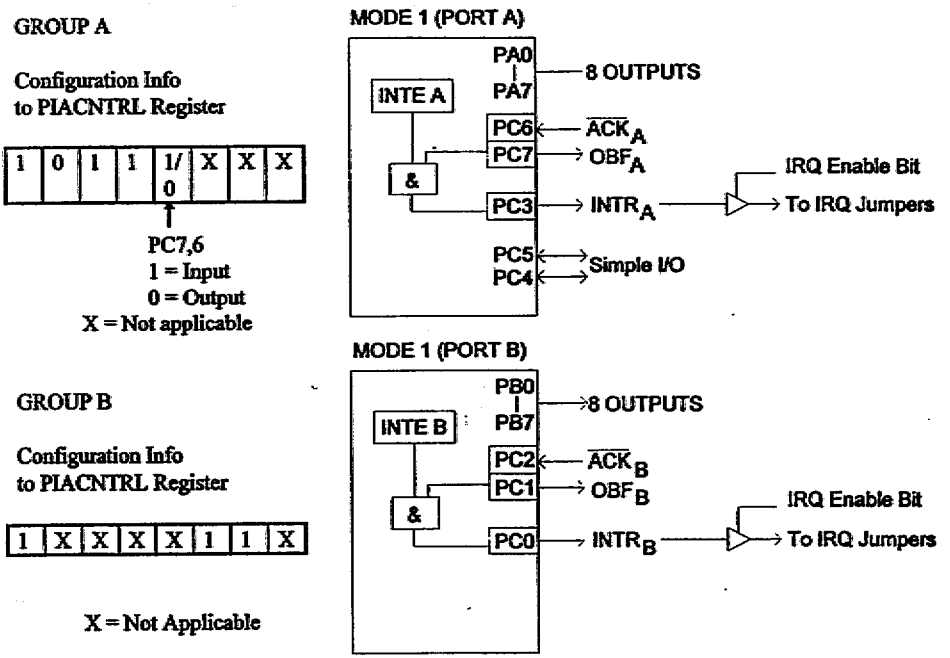


Figure 4.3: Mode 1 Input of an 8255

Mode 1 Programming

To use the 8255 PPI in mode 1 input with interrupts:

a) Write a byte to control register to configure the 8255 PPI for mode 1 and the appropriate group for data input.

b) With the bit set/reset operation, write a 1 to the Interrupt Enable Flip-Flop (INTE) of the desired port of the appropriate 8255 PPI.

c) Write a byte to the IEN0 register to enable interrupts from the appropriate 8255 PPI to the host computer.

d) The external device pulses the Strobe (/STB) input line on the digital I/O Connector low. The trailing edge of this loads the data into the input port.

e) The Input Buffer Full (IBF) output line goes high on the digital I/O connector to indicate that the data has been loaded into the input latch.

f) When the external device pulls the /STB line high, the Interrupt Request line (INTR) goes high. This indicates tothe host computer that there is data to be read from the 8255 PPI.

g) The computer reads the data using an interrupt service routine (ISR) and by doing so, automatically resets the INTR signal.

h) The external device can now pulse the /STB low again to make the PC 36C read another byte of data and hence repeat the cycle.

Whenever a group of the 8255 PPI is in mode 1 input, the status of the handshaking lines and interrupt signals can be obtained by reading Port C. The byte read contains the following information:

Port C Mode 1 Input Status Information

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C7	C6	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$

The 8255 PPI may alternatively be used in mode 1 and the data read by polled transfer.

The method is as follows:

a) Write a byte to control register to configure the 8255 PPI for mode 1 and the appropriate group for data input.

b) The program continually monitors the IBF line by reading Port C.

c) The external device pulses the Strobe (/STB) input line on the digital I/O Connector low. The trailing edge of this loads the data into the input port.

d) The Input Buffer Full (IBF) output line goes high on the digital I/O connector to indicate that the data has been loaded into the input latch.

e) This also causes the corresponding IBF bit in port C to be set and the program can thus read the data.

f) The external device can now pulse the /STB low again to make the PC 36C read another byte of data and hence repeat the cycle.

The program could also enable the INTR line with the INTE flip-flop and then monitor INTR instead of the IBF line. In this case, interrupts to the host computer are not enabled in the IEN0 register.

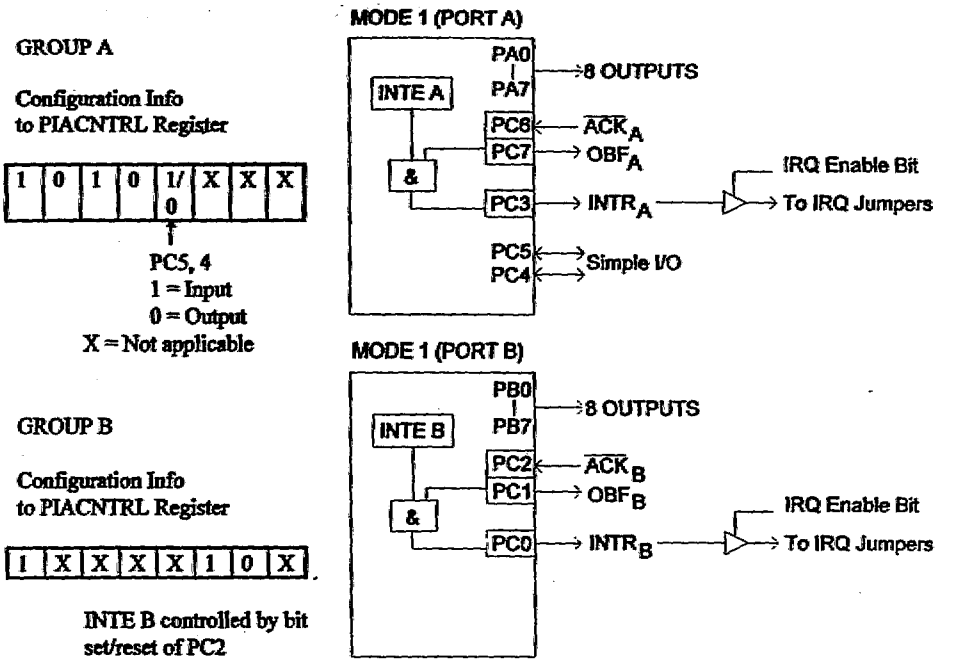


Figure 4.3b: Mode 1 Output of an 8255

To use the 8255 PPI in mode 1 output with interrupts:

a) Write a byte to control register to configure the 8255 PPI for mode 1 and the appropriate group for data output.

b) With the bit set/reset operation, write a 1 to the Interrupt Enable Flip-Flop (INTE) of the desired port of the appropriate 8255 PPI.

c) The 8255 PPI Interrupt Request Output (INTR) then goes high.

d) Write a byte to the IEN0 register to enable interrupts from the appropriate 8255 PPI to th host computer.

e) The host computer detects the INTR line is active. From an Interrupt Service Routine (ISR), it writes a byte to the output port. This automatically resets the INTR line.

f) The Output Buffer Full (/OBF) line to the digital I/O connector goes low to indicate that there is data to be read by the external device from the 8255 PPI.

) The external device pulses the Acknowledge (/ACK) input low and then high again to indicate that it has read the data.

) This makes the INTR line go high again and the cycle may be repeated until all the required data has been written.

Vhenever a group of the 8255 PPI is in mode 1 output, the status of the handshaking lines nd interrupt signals can be obtained by reading Port C. The byte read contains the ollowing information:

Port C Mode 1 Output Status Information

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$/OBF_A$	$INTE_A$	C5	C4	$INTR_A$	$INTE_B$	$/OBF_B$	$INTR_B$

'he 8255 PPI may alternatively be used in mode 1 and the data written by polled transfer.

'his is done as follows:

) Write a byte to control register to configure the 8255 PPI for mode 1 and the appropriate group for data output.

) The program continually monitors the /OBF line by reading Port C, waiting for it to go high. A high indicates that the last data written to the port has been read by the external device.

) Then the program can write new data to the port.

) The /OBF line to the digital I/O connector goes low to indicate that there is data to be read by the external device from the 8255 PPI.

) The external device pulls the /ACK input low to read the data.

) This makes the /OBF line go high again and the cycle may be repeated until all the required data has been written.

The program could also enable the INTR line with the INTE flip-flop and then monitor INTR instead of the /OBF line. In this case, interrupts to the host computer are not enabled in the IEN (Interrupt Enable Register).

4.4) Mode 2: Strobed Bidirectional Bus I/O

This mode provides a means for communicating with an external device using an 8-bit bus for both transmitting and receiving data. Both input and output handshaking signals similiar to mode 1 are provided to maintain proper bus flow descipline. Hardware interrupts signal the host computer that the port needs attention.

The following characterise Mode 2:

- Only group A operates in mode 2.
- One 8-bit bidirectional port, functions as both input and output.
- Five of the port C lines take on special functions.
- Both inputs and outputs are latched.
- One 3-bit simple I/O port available on each PPI
- Data transfer by interrupts or polled I/O.

With the 8255 PPI of the PC 36C configured in mode 2, the board provides the function of a full 8 bit wide bidirectional data bus.

GROUP A

Configuration Info
to PIACNTRL Register

1	1	X	X	X	0/1	1/0	1/0

Group B Mode
0 = Mode 0
1 = Mode 1

Port B
0 = Output
1 = Input

Port C2-C0
0 = Output
1 = Input

X = Not Applicable

INTE 1 controlled by
bit set/reset of PC6

INTE 2 controlled by
bit set/reset of PC4

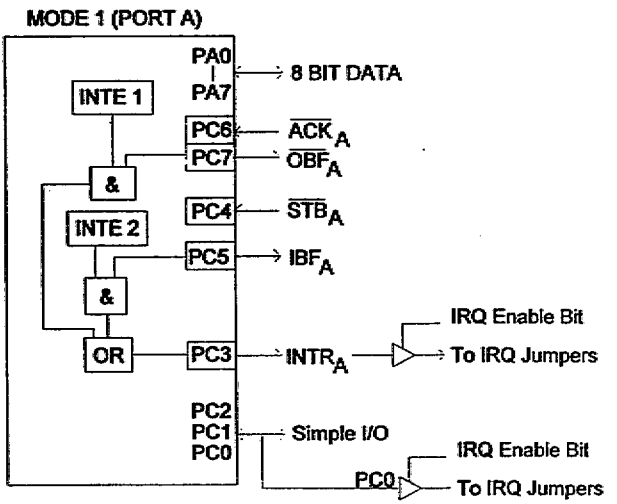


Figure 4.4: Mode 2 of an 8255

4.4.1) Mode 2 Programming

To use the 8255 PPI in mode 2 with hardware interrupt transfer:

a) Write a byte to the control register to configure the 8255 PPI for mode 2 operation.

b) Select an interrupt level with the interrupt jumpers and enable 8255 interrupt(s) in the PC 36C Interrupt Enable Register IEN.

c) With the bit set/reset operation, write a 1 to the Interrupt Enable number 1 flip-flop ($INTE_1$) to enable output transfer interrupts. Write a 1 to the Interrupt Enable number 2 flip-flop ($INTE_2$) to enable input transfer interrupts. Both input and output interrupts may be enabled at the same time.

d) With both interrupt flip-flop enabled, the interrupt request line to the host computer is activated if the external device has a strobed data into the 8255 input latch or if the external device has read the PC 36C output data from the output latch.

e) The host computer detects the INTR line is active. The Interrupt Service Routine (ISR) which services this interrupt determines whether it was an input or output interrupt by checking bit 5 (IBF_A) of the mode 2 status information from port C. In the IBF line is high (bit 5 is set) then it is an input interrupt, otherwise it is an output interrupt.

f) In either case, the ISR simply reads the data from or writes to the 8255 PPI and then issues an end of interrupt command (EOI) to the interrupt controller.

g) This generates the appropriate handshake signals from the 8255 PPI to the digital I/O connector.

h) The cycle continues when the next interrupt is generated.

Whenever the 8255 PPI is in mode 2, the status of the handshaking lines and the interrupt signals can be obtained by reading port C. The byte read contains the following information:

Table 4.4.1a) Port C Mode 2 Status Information

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$/OBF_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	C2	C1	C0

The 8255 PPI may alternatively be used in mode 2 with the data read and written by polled I/O transfer. This is done as follows:

a) Write a byte to the control register to configure the 8255 PPI for mode 2 operation.

b) The program continually monitors both the IBFA and /OBFA line by reading port C.

c) If port C bit corresponding to IBFA is set, this indicates that the external device has written data into the input latch. The program must therefore read the data from port A.

d) If the port C bit corresponding to /OBFA is set, this indicates that the external device has read the data written by the program to port A. It must therefore write more data to Port A.

e) This process can be repeated until the required amount of data has been read and written.

Interrupt to the host computer must not be enabled in the Interrupt Enable register IENC when data is transferred by polled I/O.

5) Single Bit Set/Reset

Any of the eight bits of port C can be set or reset using a single output instruction to the DIOCTRL register. When Port C is being used as status/control for port A or B, any of these bits can be set or reset just as if they were data outputs. The format of hte byte to write to the DIOCTRL register to set or reset a port C bit is repeated below.

DIO0CTL Register (write only) - Bit Set/Reset Mode

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	x	x	x	BS_2	BS_1	BS_0	S/R

0=Bit Set/Reset

Don't Care

Bit Select:
000 = PC0
to 111 = PC7

Set / Reset
0 = Reset
1 = Set

6) Mixed Mode Programming

An 8255 PPI is not constrained to operate in one mode only. For example, Port A may operate in mode 2 and port B may then operate in either mode 1 or mode 0. For nay combination, some or all of the Port C lines are used for control or status. The remaining port C lines may be used in mode 0 either as inputs or outputs.

A read operation of port C returns all the port C lines except the /ACK and /STB lines. In their place will appear the status of the Interrupt Enable flip-flops ($INTE_X$). This is illustrated in figures 6 to 8 above and the status information bytes which follow the figures.

A write operation to port C will affect lines programmed as mode 0 outputs. To write to any port C output programmed as a mode 1 output or to change an interrupt enable flip-flop, the Bit Set/Reset operation must be used.

Using the Bit Set/Reset command, any port C line programmed as an output (including INTR, IBF and /OBF) can be written or an interrupt enable flag set or reset. Lines programmed as inputs (including /ACK and /STB) are not affected by this command. Writing to these lines will affect the interrupt enable flags.

Chapter 5: Driver Software

Full driver software is supplied with the PC 36C package. Full details are explained in the EDR Software developers kit User Manual. A summary of what these drivers consist of are explained below.

Both DOS and Windows Languages are supported: They are:

DOS Languages:

Borland C/C++ Version 3.1 or 4.0
Microsoft C/C++ Version 6.0 or 7.0
Borland Pascal / Turbo Pascal Version 6.0 or 7.0
Microsoft QuickBasic Version 4.5

Windows Languages:

Delphi V1.00 / V2.00
Borland C/C++ 3.1 or 4.0
Microsoft C/C++ 6.0 or 7.0
Borland Pascal / Turbo Pascal Version 6.0 or 7.0
Visual Basic V1.00 thru V4.00

5.1) Board Handles

All EDR functions used above require a board handle as the first parameter. The board handle defines which board is affected by the function call. Using this method has several advantages, For example, there is no need for a 'select board' function; working with parallel boards is much easier; different applications using the EDR at the same time will not conflict with each other.

Board handle are integers obtained by calling EDR_AllocBoardHandle (see 7.2 of EDR Developers Toolkit). Once allocated a board handle must be initialised to the PC 36C before it can be accessed. this is achieved by calling EDR_InitBoard or EDR_InitBoardType (see 7.5 of EDR manual) with the base address or EDR_loadConfiguration (see section 7.8 of EDR manual).

EDR_InitBoard will attempt to detect the PC 36C at the base address specified.

2) Interrupt functions

Port C0 and C3 of the 8255 PPI are connected to the IRQ line via a tri-state buffer. An ISR can be installed using the EDR driver functions to service theses lines when pulses toggles the C0 and C3. Note that these lines are not latched in Mode 0. Hence the pulses must be long enough for the PC's Interrupt system to detect it.

The External Trigger Line is also connected to the IRQ line via a tri-state buffer. . An ISR can be installed using the EDR driver functions to service theses lines when pulses toggles the external trigger line + External Trigger Line Return. Note that this line is latched. The latch should be cleared in the ISR.

These functions are callable from virtually an programming language. See the EDR Software Developers Kit User Manual.

5.3) Quick Function Reference

The PC 36C Enhanced 8 port 8255 PPI Board utilises the following functions calls contained in the EDR driver developers toolkit. They are:

Function Name	Description
EDR_DIOConfigurePort	Configures a digital port for a particular mode and direction. EDR only directly supports mode 0 (EDR_DIO_SIMPLE) with the driver functions. Other modes can be be used but you will need to write your own support code.
EDR_DIOGetPortConfig	Gets the current configuration of the port A, B or C in any of the 8255 PPIs.
EDR_DIOLineInput	Gets the status of a single line (bit) in a digital input port. If the port is an output port then the last value written to the line (bit) is returned.
EDR_DIOLineOutput	Changes a single line (bit) in a digital output port.
EDR_DIOPortOutput	Writes a byte of data to the PC 36C I/O port
EDR_DIOPortInput	Reads a byte of data from the PC 36C I/O Port. If the port is an output port then the last value written to the port is returned.
EDR_HasDOReadback	Indicates if a particular board type's digital output ports can be read back or not. If the board supports readback from DO ports then doing EDR_DIOPortInput or EDR_DIOLineInput on an output port will read the last value written to the port from a board register. If the readback is not supported the EDR returns its software copy of the last value written using EDR_DIOPortOutput or EDR_DIOLineOutput.
EDR_EnableInterrupt	Enables or disables the specified interrupt on the PC 36C. Note that this just programs the board registers (ie: writing to IEN0 and IEN1 Registers) so that it will/will not generate the interrupt. If the interrupt from the is masked then interrupts from the board will be blocked. Disabling interrupts or enabling interrupts when they are already enabled may generate extra interrupts. Make sure that your ISR are prepared to handle these rogue interrupts.
EDR_InstallISR	Installs an ISR for the specified hardware interrupt request

Function Name	Description
EDR_UninstallISR	Removes an interrupt service routine that was installed with EDR_InstallISR
EDR_InstallBoardISR	Installs an ISR for a particular type of interrupt installed on the PC 36C.
EDR_UninstallBoardISR	Removes an interrupt service routine that was installed with EDR_InstallBoardISR
EDR_MaskIRQ	Masks or unmasks a particular IRQ level
EDR_MaskBoardIRQ	Masks or unmasks a particular board interrupt
EDR_ResetInterrupt	Resets an interrupt latch on the PC 36C and sends an EOI command to one of the PCs interrupt controllers on completion of the interrupt
EDR_AllocBoardHandle	Allocates a new board handle to the PC 36C. If no board handles are available then a 0 is returned. This is particularly useful is multiple PC 36C are present in the same.computer.
EDR_FreeBoardHandle	Releases a board handle allocated to the PC 36C making it available to any other PC card
EDR_InitBoardType	Initialises a board and allocates a board handle to it
EDR_ConfigDialog	Diplays a dialog box that allows the user to manually configure the driver for the Board in the computer
EDR_SaveConfiguration	Function writes configuration information to a file for later loading with EDR_LoadConfiguration
EDR_LoadConfiguration	Loads details of the Cards configuration from the file created by EDR_SaveConfiguration
EDR_RestoreDefaults	Restores factory default configuration for a baord attached to a handle
EDR_IsBaseAddressInUse	Checks if any board initialised with EDR is using the specified I/O address
EDR_DetectBoard	Tries to determine the type of board present at a specified I/O address.
EDR_SetBoardType	Changes the board type attached to a board handle
EDR_SetIRQLevel	Set the IRQ level EDR will use for the interrupt ID specified.
EDR_NumDIOPorts	Gets the number of DIO ports a board has.
EDR_ValidDIOPortConfig	Checks the configuration of a digital port.
EDR_ValidInterruptID	Checks to see if the board supports the ID specified
EDR_ValidIRQLevel	Checks an IRQ level

Chapter 6: Testing the PC 36C

Before attempting to interface the PC 36C with your application, it is essential that you test the board first. This is done using the following procedure:

6.1) Testing the PC 36C Board

Install the PC 36C using the procedure described in the Chapter 2: Installation. Proceed as follows:

* Switch the Computer on
* On the DOS prompt, go to the C:\EDR\TPAS\DEMOS\ sub-directory
* Run the DIOLOOP.EXE test program with parameter 300 where 300 is the base address of the PC 36C.

If an error message 'Board not found' appears on your screen then the PC 36C was not installed at that address. Try a different base address as specified in Apendix A (eg: 700h) and re-run the test S/W. If the problem persists then try increasing the wait states on the PC 36C Board and re-run test software. The board should work.

If the PC 36C is found, a message will appear on the screen: 'PC 36C Board found'. The program will walk a bit through port A and display all other ports (programmed as inputs) in Hex. You may feed any TTL signal input to the above ports.

.2) Connecting Normally Open devices to the 8255 PPIs

When connecting switches, etc, to the Port lines (classed as inputs) of the PPIs, it is important to ensure that the inputs are set to a defined state at all times. Figure 6.2 gives an example.

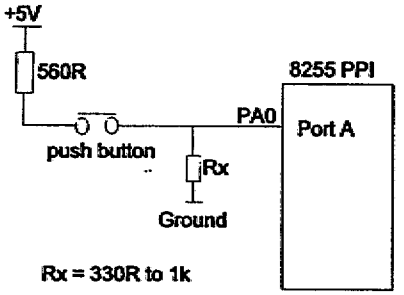


Figure 6.2: Connecting Normally Open deviecs to the PPI

Figure 6.2 gives an example of how to connect a push button to one of the lines of the 8255 PPI. We assume that when the Push button is closed, the Port line will go high (logic 1 = +5V). When the push button is not closed, the port line should be low. However, many Users does not connect the 'pull-down' resistor to the port line. If this is not done, the port line will be in a floating state and can hence yield either a high or a low.

Thus you must ensure that the port line is always connected which is done via a resistor network.

Chapter 7: Troubleshooting

Problem: 'Board not found' message appears on the screen when running test software.

Solution: Another I/O card might be using the same base address location as the PC 36C. Try a different base address other than the manufacturer's default base address (eg: 700h) and re-run test software DIOLOOP.EXE or WALKBIT.EXE found in sub directory C:\EDR\TPAS\DEMOS\. If the problem persists then try increasing the wait states on the PC 36C. If the PC 36C still does not work even after the maximum number of wait states was chosen then try a different computer with a different motherboard. If the test still fails then the PC 36C is faulty. Return the board to your distributor for repairs.

Problem: Data written to Port A, B or C (configured as Mode 0 outputs) does not set the output ports correctly.

Solution: Check the ports using the walkbit test program called WALKBIT.EXE found in EDR\TPAS\DEMOS subdirectory. Monitor the port lines of each 8255 PPI and check if the problem persists. If so, the the PPI might be faulty, replace the PPI in question with another NEC D8255AC-2 or an Intel I8255-2. You could also send the PC 36C back to your distributor for repairs.

Problem: I connected a push button to one of the port lines. When it is closed it is set to +5V (yield a logical 1) and the program reads a logical 1. However when it is open random numbers are read by the program on port A.

Solution: When the push button is not connected, it seems that the port line is floating (not connected). You must connect a 'pulldown' resistor (experiment from 330R to 1k) to the port line in order to ensure that it is in a defined state. Also note that if a port is configured as an input then all unused lines MUST be grounded. See Section 6.2 for more details.

Problem: Interrupts does not occur when the Opto-Isolator receives a pulse from 0V to above the threshold of 3.1V. In other words a square pulse Posituve edged 0 to 5V does not yield an interrupt.

Solution: First read back Bit 4 [TRIG] in the IEN Register [Base + 4] and check if the bit is high. If so then an interrupt has occurred. Check if you have enabled the Interrupt Bit (IRQEN) in the IEN Register by reading back bit 0 [IRQEN] in the IEN Register [Base + 4]. If not then the Interrupts will not occur because the tri-state buffer is disabled. Set this bit (Bit 0)

to 1 in order to enable Interrupts. For reference, see Chapter 3, Section 3.4.

If you have enabled the IRQEN bit, then check whether the IRQ line that you used is not also used by another Card in your computer. If so, then change the IRQ Jumper (JP4) to another IRQ line. Interrupts should occur after these changes are made.

> ☞ **Warning**
>
> Any parts replaced on the PC 36C must be done by a qualified or trained technician. If you (the user) is not a trained technician then rather return the board to your distributor for repairs explaining in detail what the problem is.

If you cannot solve the problem then simply call your distributor for immediate help.

Chapter 8: Repair Service

The PC 36C is guaranteed for a period of 1 year. If the board is faulty within this period, we will gladly repair it free of charge provided that the maximum specifications was not exceeded. If any burn't tracks are seen on the PC 36C Board, warranty will be void. A repair charge will be levied in the user requires the board to be repaired.

Before sending the board to your distributor for repairs, ensure that you go through Chapter 7: TroubleShooting Hints thoroughly. If, after you have gone through this Chapter, the board still does not work, return it for repairs stating in detail what the problem is.

Our repair service centre will be available to repair our products even after the 1 year warranty. A small service fee will be levied which usually covers the cost of the components that are faulty.

Specifications

Computer Host Interface

Base Address:	Switchable from 0 to 7FFh on 8 byte boundaries
Bus Type:	XT, AT, ISA or EISA
I/O Wait States:	0, 2, 4, or 8 Jumper selectable.
Number of Registers:	Eight 8-bit Registers
Word size:	8 bits
Word transfer Rate:	10Mhz max (depends on computer and program)
Interrupts:	Jumper selectable from IRQ2, 3, 4, 7, 10, 11, 12, 15

Digital Inputs/Outputs

✱ *Number of lines:*	24 I/O lines in three 8-bit digital ports
✱ *Compatibilty:*	TTL
✱ *Input Voltage:*	Logic Low: 0.5V to 0.8V Logic High: 2V to 5V
✱ *Output Voltage:*	Logic 0: 0.45V max Logic 1: 2.4V min
✱ *Output Current:*	Low State: 1.7mA max High State: -200µA min
✱ *Max Darlington drive current*	-4.0mA from ports types B and C only
✱ *Maximum Power per 8255*	1W max from all three ports per PPI

Absolute Maximum TTL Inputs

✱ *Absolute Max Input voltage:*	6.5V*
✱ *Absolute Min Input voltage:*	-0.5V*

☞ Warning

Stresses greater than listed above may cause permanent damage to the PC 36C. This stress rating only applies to the PC 36C at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. We do not recommend exposure to absolute maximum ratings.

I/O Connector

✱ *Digital I/O Connector:*	*37 D-type Male*
✱ *Max ±5V, ±12V supply current at I/O connector:*	*100mA from +5V typ. This also depends on the host computer power supply rating*

Optically Isolated External Trigger Input

✱ *Input voltage:*	0 to 3V	logical low
	3.1V to 24V	logical high
✱ *Max reverse voltage:*	400V peak	
✱ *Max input current:*	1A peak 30mA continuous	
✱ *Signal frequency response:*	10kHz	
✱ *Interrupt link:*	Jumper selectable from IRQ2, 3, 4, 7, 10, 11, 12, 15	

Enviromental

✱ *Operating temperature:*	0°C to 55°C
✱ *Storage temperature:*	-55°C to 150°C
✱ *Relative humidity:*	5% to 90% non-condensing
✱ *PC Board size:*	124mm x 85mm (including edge connector)

Power Supply Requirements

✱ *+5V Supply: :*	100mA typ (excludes +5V power for User Interfacing)

Appendix A

Base Address Switch Settings

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
00	ON	ON	ON	ON	ON	ON	ON	ON	00
08	ON	ON	ON	ON	ON	ON	ON	OFF	08
10	ON	ON	ON	ON	ON	ON	OFF	ON	10
18	ON	ON	ON	ON	ON	ON	OFF	OFF	18
20	ON	ON	ON	ON	ON	OFF	ON	ON	20
28	ON	ON	ON	ON	ON	OFF	ON	OFF	28
30	ON	ON	ON	ON	ON	OFF	OFF	ON	30
38	ON	ON	ON	ON	ON	OFF	OFF	OFF	38
40	ON	ON	ON	ON	OFF	ON	ON	ON	40
48	ON	ON	ON	ON	OFF	ON	ON	OFF	48
50	ON	ON	ON	ON	OFF	ON	OFF	ON	50
58	ON	ON	ON	ON	OFF	ON	OFF	OFF	58
60	ON	ON	ON	ON	OFF	OFF	ON	ON	60
68	ON	ON	ON	ON	OFF	OFF	ON	OFF	68
70	ON	ON	ON	ON	OFF	OFF	OFF	ON	70
78	ON	ON	ON	ON	OFF	OFF	OFF	OFF	78
80	ON	ON	ON	OFF	ON	ON	ON	ON	80
88	ON	ON	ON	OFF	ON	ON	ON	OFF	88
90	ON	ON	ON	OFF	ON	ON	OFF	ON	90
98	ON	ON	ON	OFF	ON	ON	OFF	OFF	98
A0	ON	ON	ON	OFF	ON	OFF	ON	ON	A0
A8	ON	ON	ON	OFF	ON	OFF	ON	OFF	A8
B0	ON	ON	ON	OFF	ON	OFF	OFF	ON	B0
B8	ON	ON	ON	OFF	ON	OFF	OFF	OFF	B8
C0	ON	ON	ON	OFF	OFF	ON	ON	ON	C0
C8	ON	ON	ON	OFF	OFF	ON	ON	OFF	C8
D0	ON	ON	ON	OFF	OFF	ON	OFF	ON	D0
D8	ON	ON	ON	OFF	OFF	ON	OFF	OFF	D8
E0	ON	ON	ON	OFF	OFF	OFF	ON	ON	E0
E8	ON	ON	ON	OFF	OFF	OFF	ON	OFF	E8
F0	ON	ON	ON	OFF	OFF	OFF	OFF	ON	F0
F8	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	F8

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
100	ON	ON	OFF	ON	ON	ON	ON	ON	100
108	ON	ON	OFF	ON	ON	ON	ON	OFF	108
110	ON	ON	OFF	ON	ON	ON	OFF	ON	110
118	ON	ON	OFF	ON	ON	ON	OFF	OFF	118
120	ON	ON	OFF	ON	ON	OFF	ON	ON	120
128	ON	ON	OFF	ON	ON	OFF	ON	OFF	128
130	ON	ON	OFF	ON	ON	OFF	OFF	ON	130
138	ON	ON	OFF	ON	ON	OFF	OFF	OFF	138
140	ON	ON	OFF	ON	OFF	ON	ON	ON	140
148	ON	ON	OFF	ON	OFF	ON	ON	OFF	148
150	ON	ON	OFF	ON	OFF	ON	OFF	ON	150
158	ON	ON	OFF	ON	OFF	ON	OFF	OFF	158
160	ON	ON	OFF	ON	OFF	OFF	ON	ON	160
168	ON	ON	OFF	ON	OFF	OFF	ON	OFF	168
170	ON	ON	OFF	ON	OFF	OFF	OFF	ON	170
178	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	178
180	ON	ON	OFF	OFF	ON	ON	ON	ON	180
188	ON	ON	OFF	OFF	ON	ON	ON	OFF	188
190	ON	ON	OFF	OFF	ON	ON	OFF	ON	190
198	ON	ON	OFF	OFF	ON	ON	OFF	OFF	198
1A0	ON	ON	OFF	OFF	ON	OFF	ON	ON	1A0
1A8	ON	ON	OFF	OFF	ON	OFF	ON	OFF	1A8
1B0	ON	ON	OFF	OFF	ON	OFF	OFF	ON	1B0
1B8	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	1B8
1C0	ON	ON	OFF	OFF	OFF	ON	ON	ON	1C0
1C8	ON	ON	OFF	OFF	OFF	ON	ON	OFF	1C8
1D0	ON	ON	OFF	OFF	OFF	ON	OFF	ON	1D0
1D8	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	1D8
1E0	ON	ON	OFF	OFF	OFF	OFF	ON	ON	1E0
1E8	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	1E8
1F0	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	1F0
1F8	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	1F8

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
200	ON	OFF	ON	ON	ON	ON	ON	ON	200
208	ON	OFF	ON	ON	ON	ON	ON	OFF	208
210	ON	OFF	ON	ON	ON	ON	OFF	ON	210
218	ON	OFF	ON	ON	ON	ON	OFF	OFF	218
220	ON	OFF	ON	ON	ON	OFF	ON	ON	220
228	ON	OFF	ON	ON	ON	OFF	ON	OFF	228
230	ON	OFF	ON	ON	ON	OFF	OFF	ON	230
238	ON	OFF	ON	ON	ON	OFF	OFF	OFF	238
240	ON	OFF	ON	ON	OFF	ON	ON	ON	240
248	ON	OFF	ON	ON	OFF	ON	ON	OFF	248
250	ON	OFF	ON	ON	OFF	ON	OFF	ON	250
258	ON	OFF	ON	ON	OFF	ON	OFF	OFF	258
260	ON	OFF	ON	ON	OFF	OFF	ON	ON	260
268	ON	OFF	ON	ON	OFF	OFF	ON	OFF	268
270	ON	OFF	ON	ON	OFF	OFF	OFF	ON	270
278	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	278
280	ON	OFF	ON	OFF	ON	ON	ON	ON	280
288	ON	OFF	ON	OFF	ON	ON	ON	OFF	288
290	ON	OFF	ON	OFF	ON	ON	OFF	ON	290
298	ON	OFF	ON	OFF	ON	ON	OFF	OFF	298
2A0	ON	OFF	ON	OFF	ON	OFF	ON	ON	2A0
2A8	ON	OFF	ON	OFF	ON	OFF	ON	OFF	2A8
2B0	ON	OFF	ON	OFF	ON	OFF	OFF	ON	2B0
2B8	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	2B8
2C0	ON	OFF	ON	OFF	OFF	ON	ON	ON	2C0
2C8	ON	OFF	ON	OFF	OFF	ON	ON	OFF	2C8
2D0	ON	OFF	ON	OFF	OFF	ON	OFF	ON	2D0
2D8	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	2D8
2E0	ON	OFF	ON	OFF	OFF	OFF	ON	ON	2E0
2E8	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	2E8
2F0	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	2F0
2F8	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	2F8

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
300	ON	OFF	OFF	ON	ON	ON	ON	ON	300
308	ON	OFF	OFF	ON	ON	ON	ON	OFF	308
310	ON	OFF	OFF	ON	ON	ON	OFF	ON	310
318	ON	OFF	OFF	ON	ON	ON	OFF	OFF	318
320	ON	OFF	OFF	ON	ON	OFF	ON	ON	320
328	ON	OFF	OFF	ON	ON	OFF	ON	OFF	328
330	ON	OFF	OFF	ON	ON	OFF	OFF	ON	330
338	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	338
340	ON	OFF	OFF	ON	OFF	ON	ON	ON	340
348	ON	OFF	OFF	ON	OFF	ON	ON	OFF	348
350	ON	OFF	OFF	ON	OFF	ON	OFF	ON	350
358	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	358
360	ON	OFF	OFF	ON	OFF	OFF	ON	ON	360
368	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	368
370	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	370
378	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	378
380	ON	OFF	OFF	OFF	ON	ON	ON	ON	380
388	ON	OFF	OFF	OFF	ON	ON	ON	OFF	388
390	ON	OFF	OFF	OFF	ON	ON	OFF	ON	390
398	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	398
3A0	ON	OFF	OFF	OFF	ON	OFF	ON	ON	3A0
3A8	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	3A8
3B0	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	3B0
3B8	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	3B8
3C0	ON	OFF	OFF	OFF	OFF	ON	ON	ON	3C0
3C8	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	3C8
3D0	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	3D0
3D8	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	3D8
3E0	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	3E0
3E8	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	3E8
3F0	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	3F0
3F8	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3F8

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
400	OFF	ON	ON	ON	ON	ON	ON	ON	400
408	OFF	ON	ON	ON	ON	ON	ON	OFF	408
410	OFF	ON	ON	ON	ON	ON	OFF	ON	410
418	OFF	ON	ON	ON	ON	ON	OFF	OFF	418
420	OFF	ON	ON	ON	ON	OFF	ON	ON	420
428	OFF	ON	ON	ON	ON	OFF	ON	OFF	428
430	OFF	ON	ON	ON	ON	OFF	OFF	ON	430
438	OFF	ON	ON	ON	ON	OFF	OFF	OFF	438
440	OFF	ON	ON	ON	OFF	ON	ON	ON	440
448	OFF	ON	ON	ON	OFF	ON	ON	OFF	448
450	OFF	ON	ON	ON	OFF	ON	OFF	ON	450
458	OFF	ON	ON	ON	OFF	ON	OFF	OFF	458
460	OFF	ON	ON	ON	OFF	OFF	ON	ON	460
468	OFF	ON	ON	ON	OFF	OFF	ON	OFF	468
470	OFF	ON	ON	ON	OFF	OFF	OFF	ON	470
478	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	478
480	OFF	ON	ON	OFF	ON	ON	ON	ON	480
488	OFF	ON	ON	OFF	ON	ON	ON	OFF	488
490	OFF	ON	ON	OFF	ON	ON	OFF	ON	490
498	OFF	ON	ON	OFF	ON	ON	OFF	OFF	498
4A0	OFF	ON	ON	OFF	ON	OFF	ON	ON	4A0
4A8	OFF	ON	ON	OFF	ON	OFF	ON	OFF	4A8
4B0	OFF	ON	ON	OFF	ON	OFF	OFF	ON	4B0
4B8	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	4B8
4C0	OFF	ON	ON	OFF	OFF	ON	ON	ON	4C0
4C8	OFF	ON	ON	OFF	OFF	ON	ON	OFF	4C8
4D0	OFF	ON	ON	OFF	OFF	ON	OFF	ON	4D0
4D8	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	4D8
4E0	OFF	ON	ON	OFF	OFF	OFF	ON	ON	4E0
4E8	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	4E8
4F0	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	4F0
4F8	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	4F8

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
500	OFF	ON	OFF	ON	ON	ON	ON	ON	500
508	OFF	ON	OFF	ON	ON	ON	ON	OFF	508
510	OFF	ON	OFF	ON	ON	ON	OFF	ON	510
518	OFF	ON	OFF	ON	ON	ON	OFF	OFF	518
520	OFF	ON	OFF	ON	ON	OFF	ON	ON	520
528	OFF	ON	OFF	ON	ON	OFF	ON	OFF	528
530	OFF	ON	OFF	ON	ON	OFF	OFF	ON	530
538	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	538
540	OFF	ON	OFF	ON	OFF	ON	ON	ON	540
548	OFF	ON	OFF	ON	OFF	ON	ON	OFF	548
550	OFF	ON	OFF	ON	OFF	ON	OFF	ON	550
558	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	558
560	OFF	ON	OFF	ON	OFF	OFF	ON	ON	560
568	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	568
570	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	570
578	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	578
580	OFF	ON	OFF	OFF	ON	ON	ON	ON	580
588	OFF	ON	OFF	OFF	ON	ON	ON	OFF	588
590	OFF	ON	OFF	OFF	ON	ON	OFF	ON	590
598	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	598
5A0	OFF	ON	OFF	OFF	ON	OFF	ON	ON	5A0
5A8	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	5A8
5B0	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	5B0
5B8	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	5B8
5C0	OFF	ON	OFF	OFF	OFF	ON	ON	ON	5C0
5C8	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	5C8
5D0	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	5D0
5D8	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	5D8
5E0	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	5E0
5E8	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	5E8
5F0	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	5F0
5F8	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	5F8

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
600	OFF	OFF	ON	ON	ON	ON	ON	ON	600
608	OFF	OFF	ON	ON	ON	ON	ON	OFF	608
610	OFF	OFF	ON	ON	ON	ON	OFF	ON	610
618	OFF	OFF	ON	ON	ON	ON	OFF	OFF	618
620	OFF	OFF	ON	ON	ON	OFF	ON	ON	620
628	OFF	OFF	ON	ON	ON	OFF	ON	OFF	628
630	OFF	OFF	ON	ON	ON	OFF	OFF	ON	630
638	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	638
640	OFF	OFF	ON	ON	OFF	ON	ON	ON	640
648	OFF	OFF	ON	ON	OFF	ON	ON	OFF	648
650	OFF	OFF	ON	ON	OFF	ON	OFF	ON	650
658	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	658
660	OFF	OFF	ON	ON	OFF	OFF	ON	ON	660
668	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	668
670	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	670
678	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	678
680	OFF	OFF	ON	OFF	ON	ON	ON	ON	680
688	OFF	OFF	ON	OFF	ON	ON	ON	OFF	688
690	OFF	OFF	ON	OFF	ON	ON	OFF	ON	690
698	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	698
6A0	OFF	OFF	ON	OFF	ON	OFF	ON	ON	6A0
6A8	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	6A8
6B0	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	6B0
6B8	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	6B8
6C0	OFF	OFF	ON	OFF	OFF	ON	ON	ON	6C0
6C8	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	6C8
6D0	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	6D0
6D8	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	6D8
6E0	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	6E0
6E8	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	6E8
6F0	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	6F0
6F8	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	6F8

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
700	OFF	OFF	OFF	ON	ON	ON	ON	ON	700
708	OFF	OFF	OFF	ON	ON	ON	ON	OFF	708
710	OFF	OFF	OFF	ON	ON	ON	OFF	ON	710
718	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	718
720	OFF	OFF	OFF	ON	ON	OFF	ON	ON	720
728	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	728
730	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	730
738	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	738
740	OFF	OFF	OFF	ON	OFF	ON	ON	ON	740
748	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	748
750	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	750
758	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	758
760	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	760
768	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	768
770	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	770
778	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	778
780	OFF	OFF	OFF	OFF	ON	ON	ON	ON	780
788	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	788
790	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	790
798	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	798
7A0	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	7A0
7A8	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	7A8
7B0	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	7B0
7B8	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	7B8
7C0	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	7C0
7C8	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	7C8
7D0	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	7D0
7D8	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	7D8
7E0	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	7E0
7E8	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	7E8
7F0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	7F0
7F8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	7F8

Appendix B

EAGLE TECHNOLOGY TITLE: PC 36C I/O BOARD TOP SILK	DOC NO: PC36C REV 1A FILEMANE: 36CB.PCB DATE: 6/7/96