PC-36
single 8255 I/O card

PC-37
solid state relay
adaptor unit

PC-38
electromechanical
relay adaptor unit

User manual

PC-36/A 8255 RELAY DRIVER CARD
PC-37 SOLID STATE RELAY ADAPTOR UNIT
& PC-38 ELECTROMECHANICAL RELAY ADAPTOR UNIT

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Introduction

The PC-36 8255 relay driver card is a programmable parallel interface for the IBM-PC/XT and compatible machines. Although it has been specifically designed to drive the PC-37 solid state relay adaptor unit, it is also ideally suited for driving other solid state relays, or small electromechanical relays. The software disc supplied as standard gives examples of testing, setting, and resetting the ports.

The 24 I/O lines of the PC-36 are arranged in three 8-bit ports (A,B and C). They can be programmed in two groups of twelve, and used in three main modes of operation:

Mode 0: Each of the two groups may be programmed in three sets of four lines of input or output.

Mode 1: Each of the two groups is programmed to have eight lines of input or output, and three of the remaining lines in each group are used for interrupt control signals and handshaking.

Mode 2: This is a bi-directional mode, using eight lines for a bi-directional bus, and five for handshaking. The fifth line is borrowed from the other group.

The 24 I/O lines, +5V, +12V, and ground lines are available at the 37-pin D-connector at the rear of the PC-36.

The PC-36A differs from the PC-36 by having 256 possible addresses, and occupying eight byte locations instead of four. The four registers are duplicated: for example, if the base address 778H is chosen, the four registers will appear at locations 778-77B and 77C-77F, and may be accessed at either location. Full switching details will be found at the rear of this manual.

To run the sample applications software, boot your PC and, using the demonstration diskette, type "autoexec.bat <return>".

The PC-37 solid state relay adaptor unit is designed to be driven by the PC-36. It is supplied with either 8 or 16 Opto-22 P240 D4 relays fitted. These can each switch a continuous AC load of 240V at 4A. Switching is performed at the AC voltage zero crossover, to prevent surge currents and electromagnetic interference.

Ports A and B of the PC-36 only are used to drive the PC-37, but Port C's 8 lines are available at the PC-37 terminal block, together with +5V, +12V and ground. The terminal block is labelled with all input and output lines. The Darlington transistor arrays, IC1 to 1C3, are specially designed for relay driving applications, and are fully TTL and CMOS compatible.

The PC-38 electro-mechanical relay adaptor card is driven by the PC-36 in the same way as is the PC-37. This card is designed to switch up to 32 AC or DC loads under software control of an IBM-PC/XT or compatible machine. Each contact of the 16 DPDT relays can switch two resistive loads of 24V/3A DC or 100V/3A AC. Inductive loads can also be switched if the user takes precautions against contact arcing, which can result in the contacts sticking.

All the relay contacts (6 per relay) are available on a screw panel on the PC-38. The 8 Port C I/O lines of the PC-36 are also available on a screw terminal on the PC-38. They can be used for digital I/O. The Darlington transistor arrays used on the PC-38 are the same as those on the PC-37.

Opto-22 model P240 D4 solid state relay

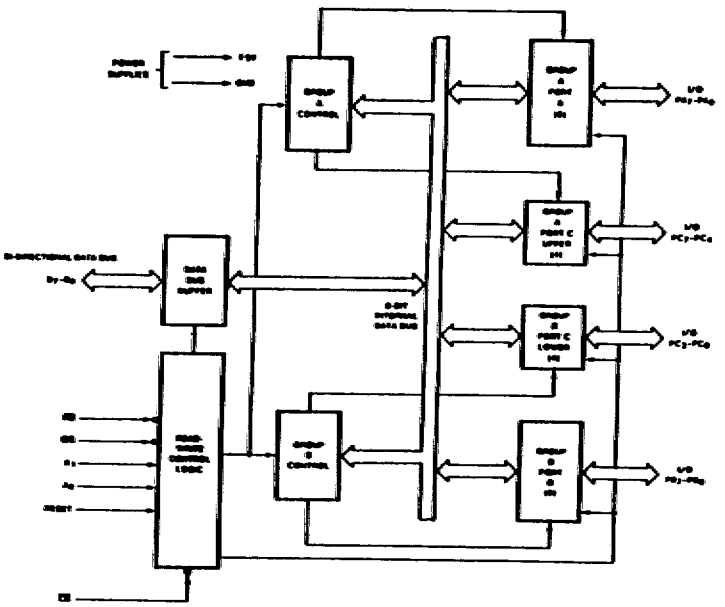
Nominal AC line volts	240
Nominal current rating	4A
1 cycle surge (peak)	85A
Nominal signal I/p resistance	1000 ohms
Signal pickup volts	3V DC
Signal dropout volts	1V DC
Peak repetitive volts (max)	500
Max. contact volts drop	1.6
Max. offstage leakage	5mA
AC volts operating range	24 - 280
Standard isolation volts	4KV RMS
Dissipation watts/amp	1
Operating temp.	-40 to + 100 deg. C
Operating freq.	25 to 65Hz
Turn-on time	0.5 cycle max. zero voltage
Turn-off time	0.5 cycle max. zero current
DV/DT off state	200V/microsecond
DV/DT commutating	Snubbed for rated current at 0.5 power factor

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- Reduces System Package Count
- Improved DC Driving Capability
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range
- 40 Pin DIP Package or 44 Lead PLCC

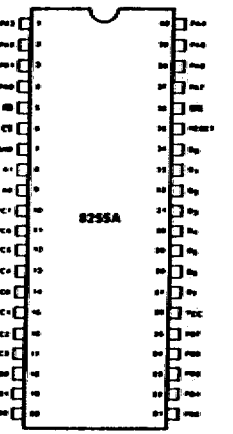
(See Intel Packaging: Order Number: 231369)

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. I has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes o operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be inpu or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. O the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operatior (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.



231308-1

Figure 1. 8255A Block Diagram



231308-2

Figure 2. Pin Configuration

8255A FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communication between the 8255A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

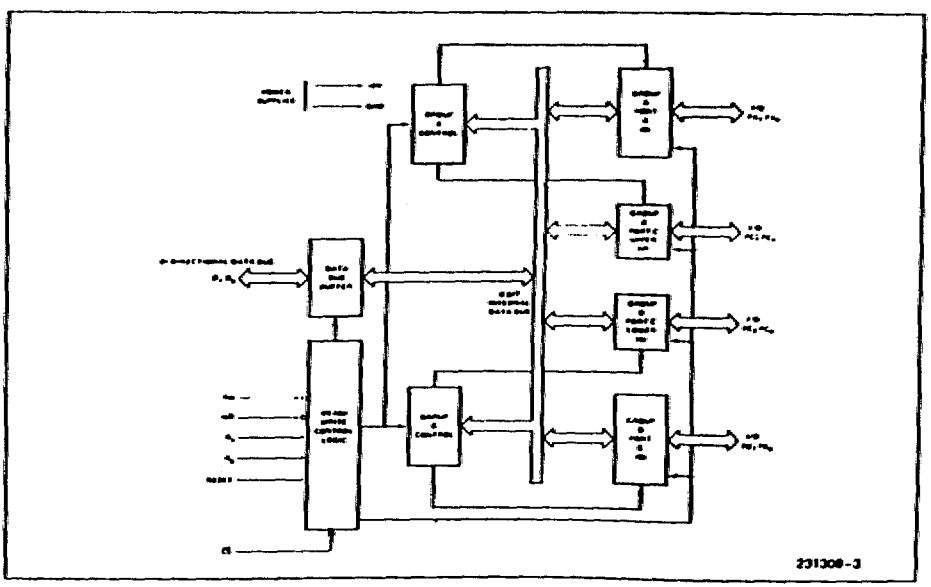


Figure 3. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

8255A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
					Output Operation (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					Disable Function
X	X	X	X	1	Data Bus → 3-State
1	1	0	1	0	Illegal Condition
X	X	1	1	0	Data Bus → 3-State

(RESET)

Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A—Port A and Port C upper (C7-C4)

Control Group B—Port B and Port C lower (C3-C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

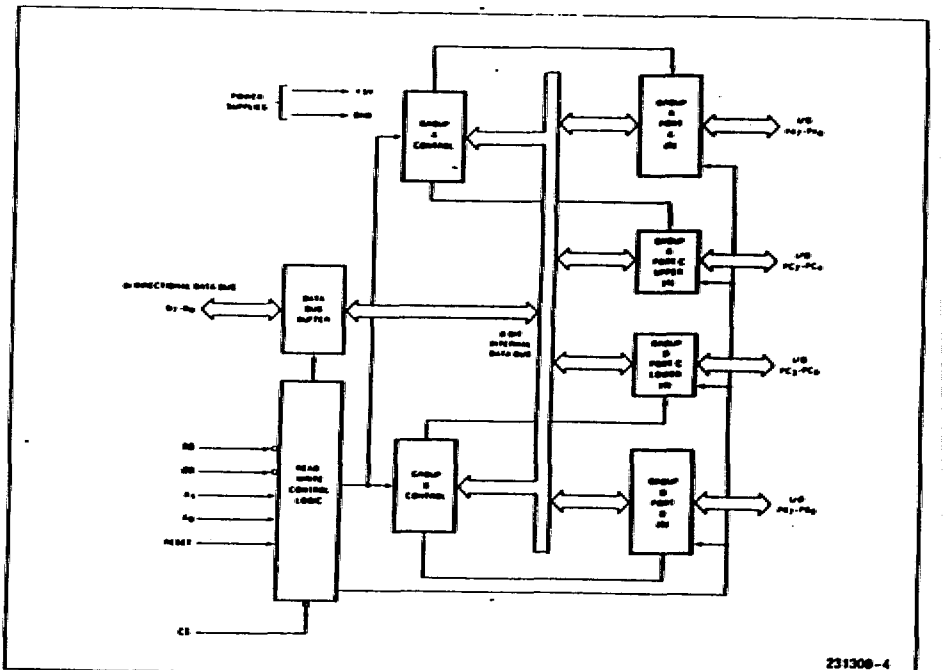
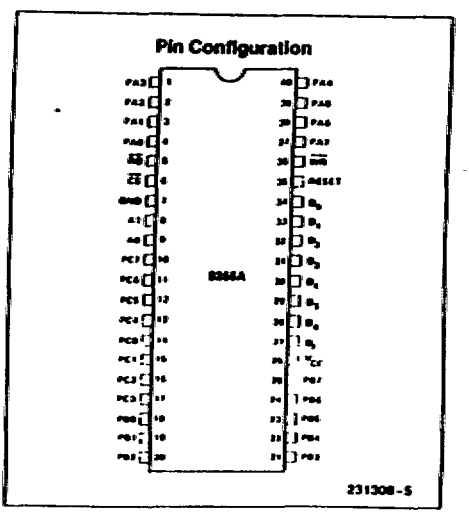


Figure 4. 8225A Block Diagram Showing Group A and Group B Control Functions



Pin Names

D_7–D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0, A1	Port Address
PA7–PA0	Port A (BIT)
PB7–PB0	Port B (BIT)
PC7–PC0	Port C (BIT)
V_{CC}	+5 Volts
GND	0 Volts

8255A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0—Basic Input/Output

Mode 1—Strobed Input/Output

Mode 2—Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

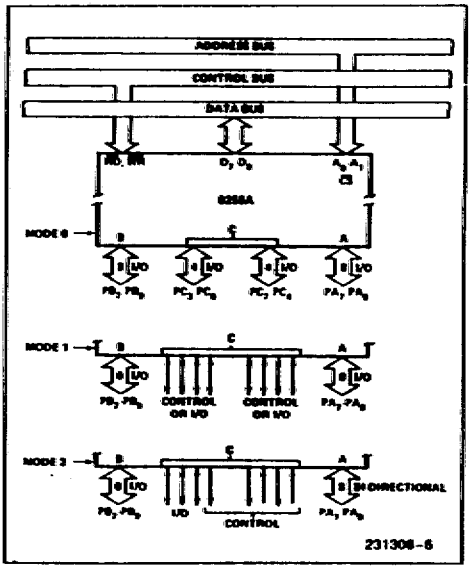


Figure 5. Basic Mode Definitions and Bus Interface

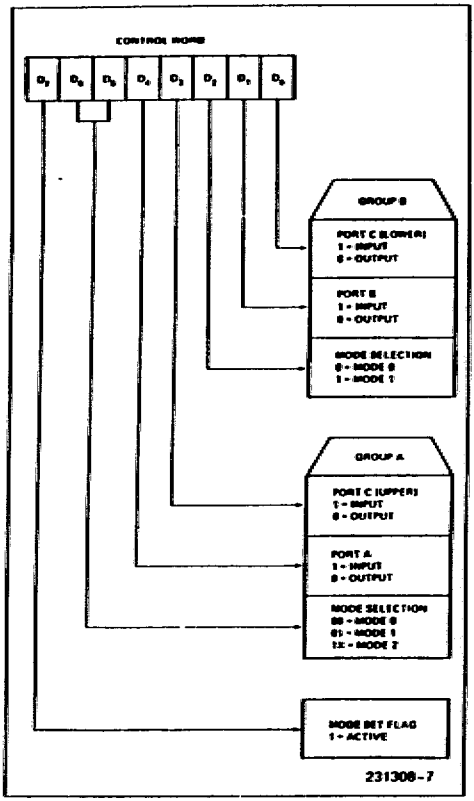


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

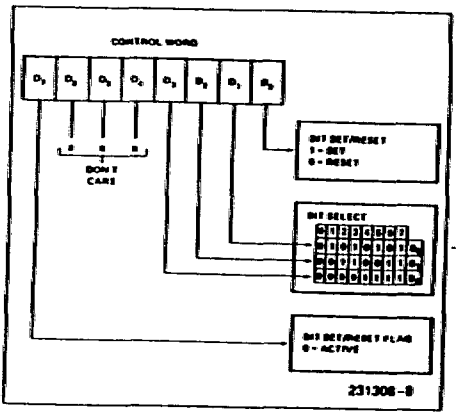


Figure 7. Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET)—INTE is set—Interrupt enable

(BIT-RESET)—INTE is RESET—Interrupt disable

NOTE:
All Mask flip-flops are automatically reset during mode selection and device Reset.

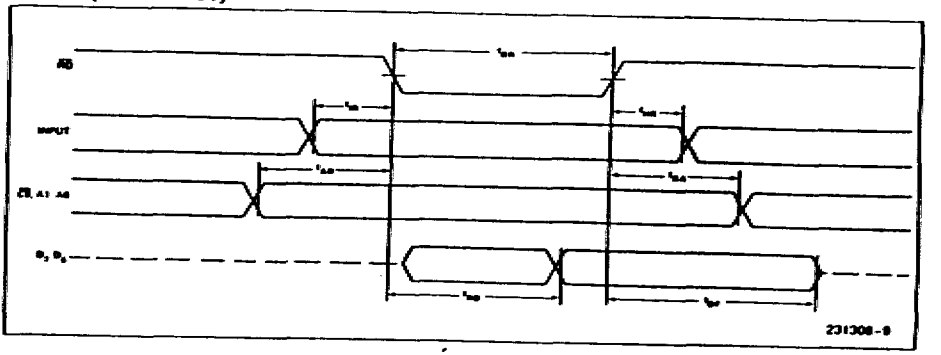
Operating Modes

MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

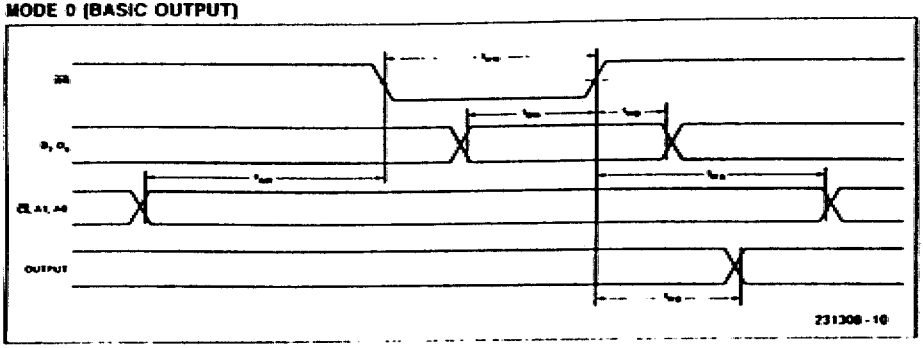
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

MODE 0 (BASIC INPUT)



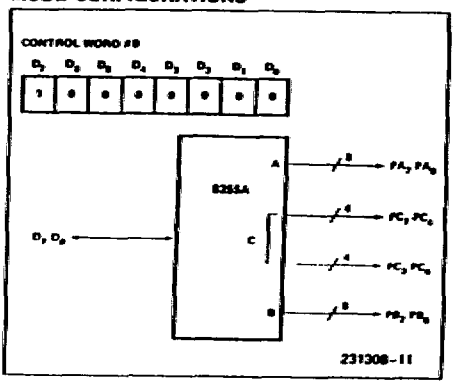
MODE 0 (BASIC OUTPUT)

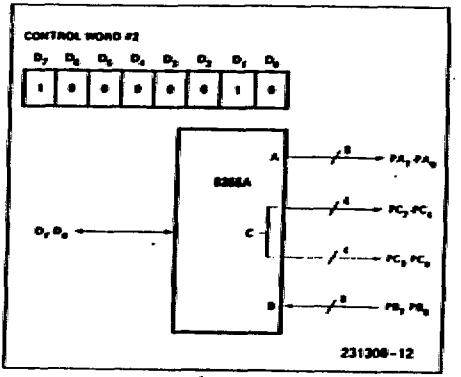


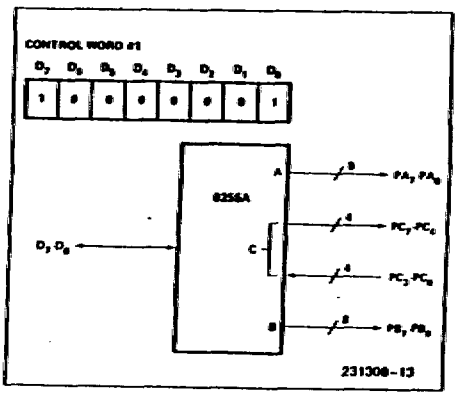
MODE 0 PORT DEFINITION

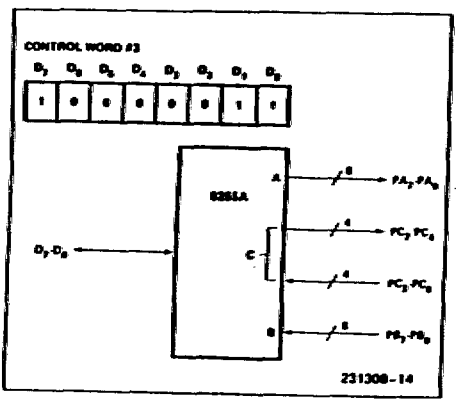
A		B		Group A		#	Group B	
D_4	D_3	D_1	D_0	Port A	Port C (Upper)		Port B	Port C (Lower)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

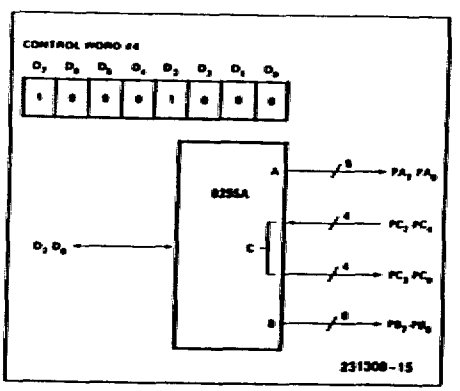
MODE CONFIGURATIONS

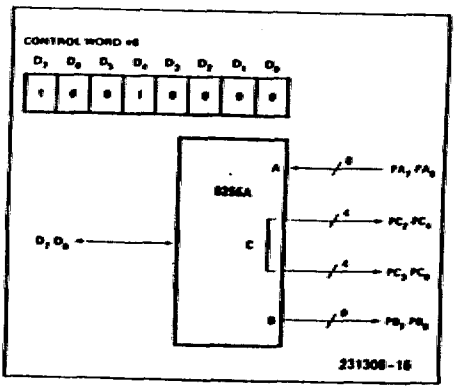


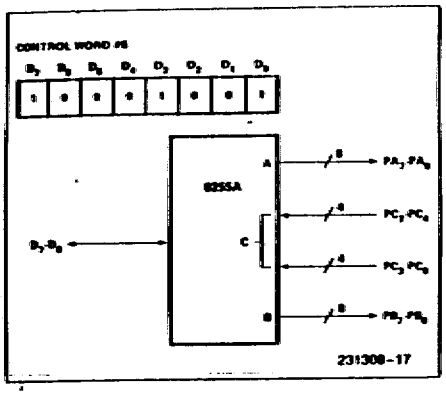








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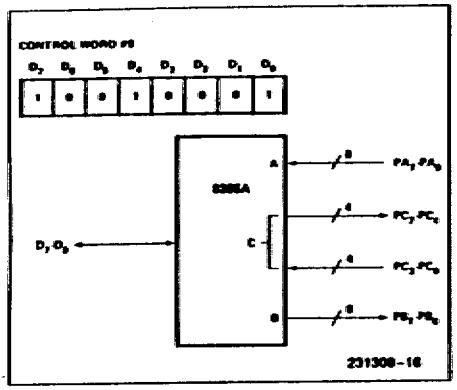
8255A
A
C
B
231308-17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A
C
B
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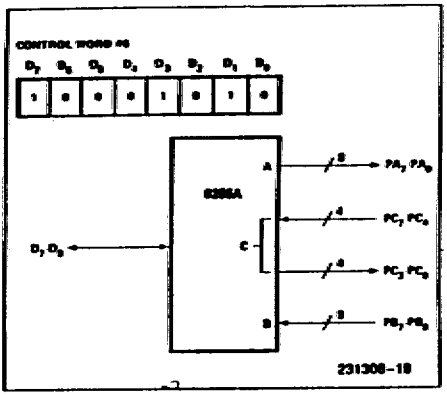
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B
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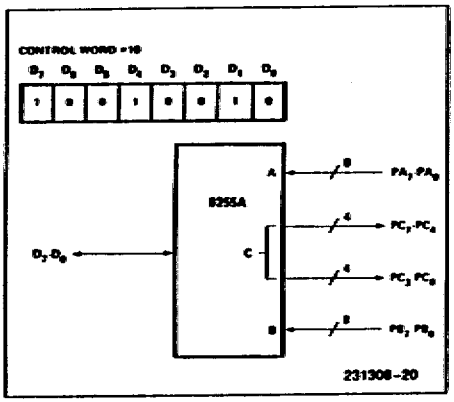
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B
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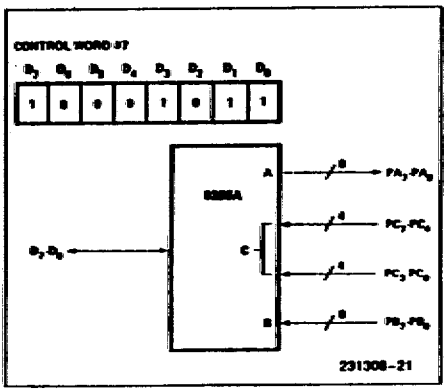
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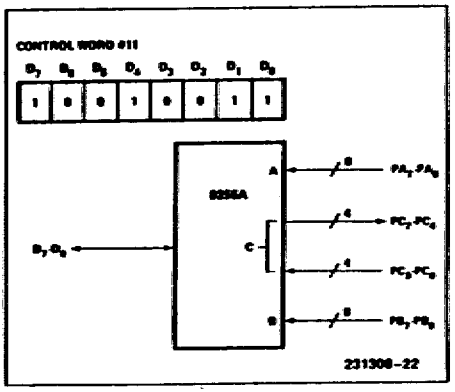
A
C
B
231308-21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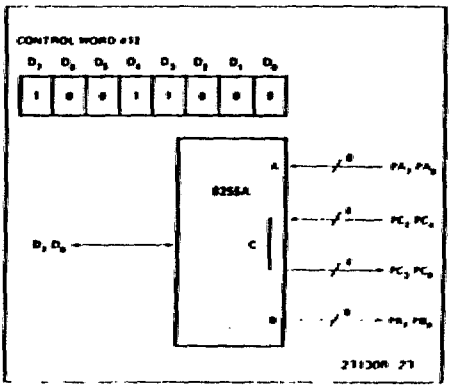
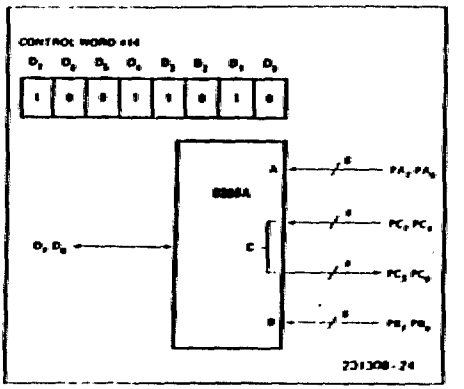
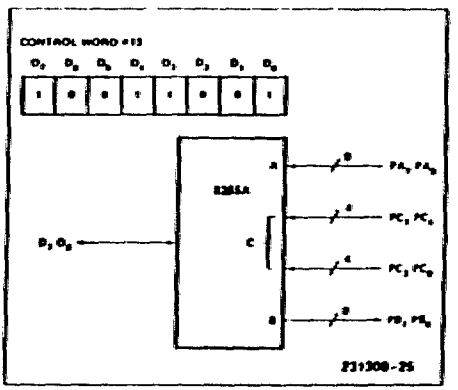
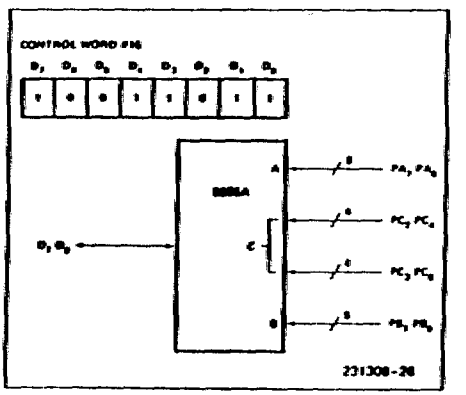
A
C
B
231308-22









Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4

INTE B

Controlled by bit set/reset of PC_2

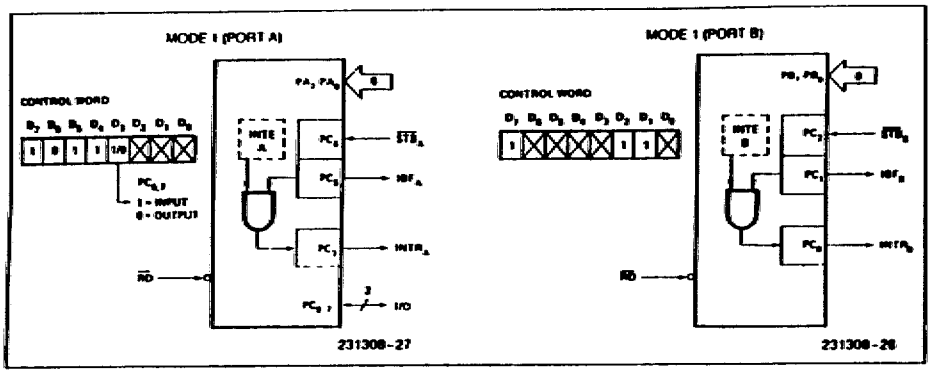


Figure 8. MODE 1 Input

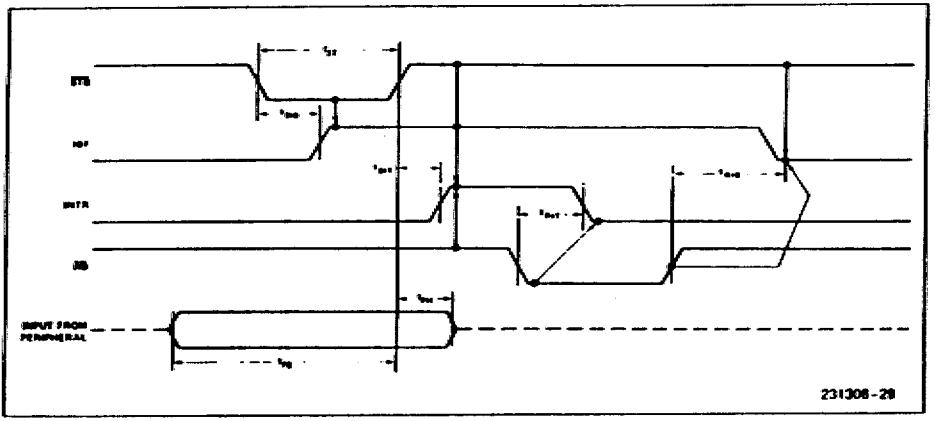


Figure 9. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", $\overline{OBF}$ is a "one", and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.

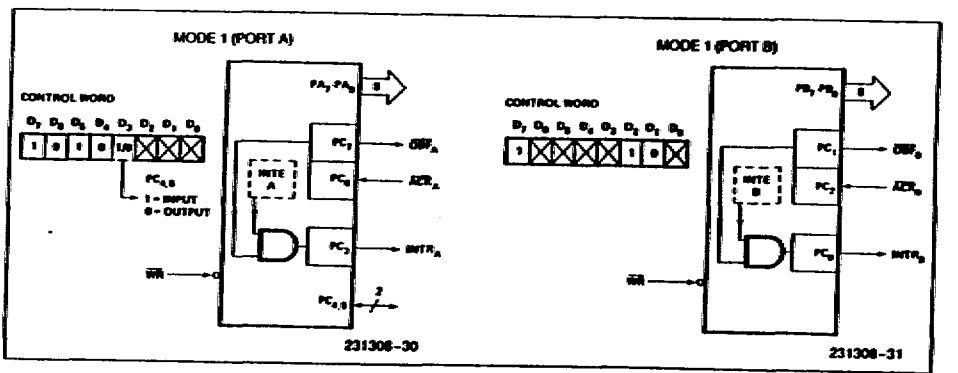


Figure 10. MODE 1 Output

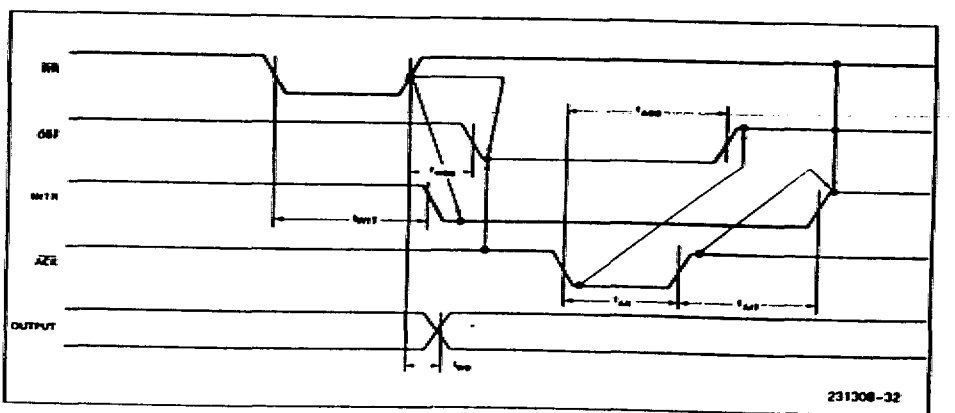


Figure 11. MODE 1 (Strobed Output)

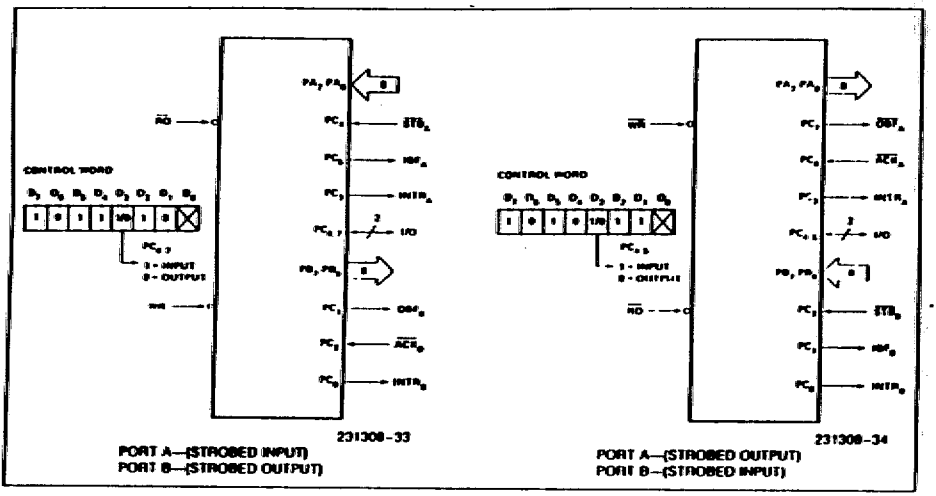


Figure 12. Combinations of MODE 1

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in MODE 1 to support a wide variety of strobed I/O applications.

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

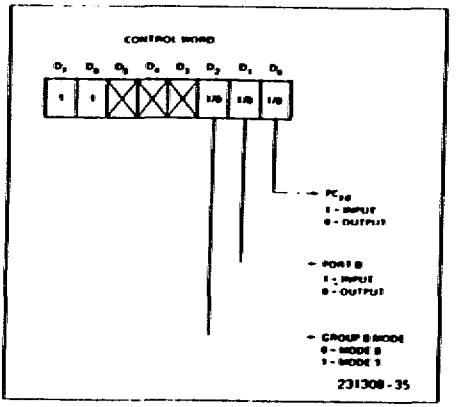


Figure 13. MODE Control Word

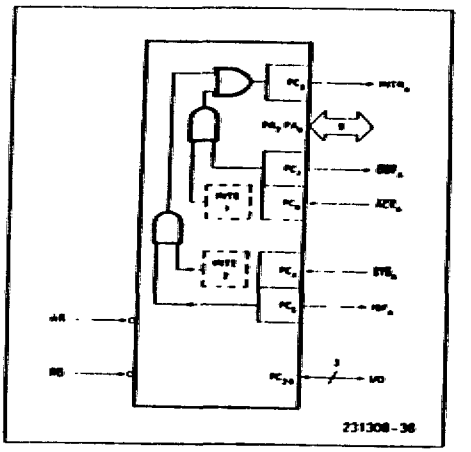
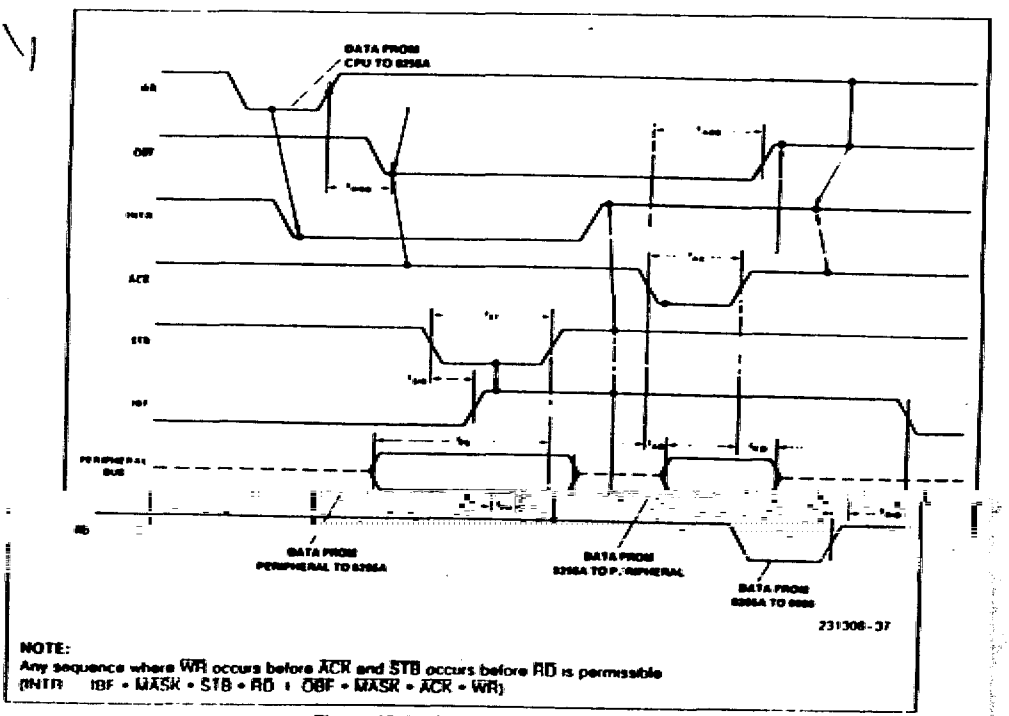


Figure 14. MODE 2



NOTE:
Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible
(INTR = IBF • MASK • STB • RD + OBF • MASK • ACK • WR)

Figure 15. MODE 2 (Bidirectional)

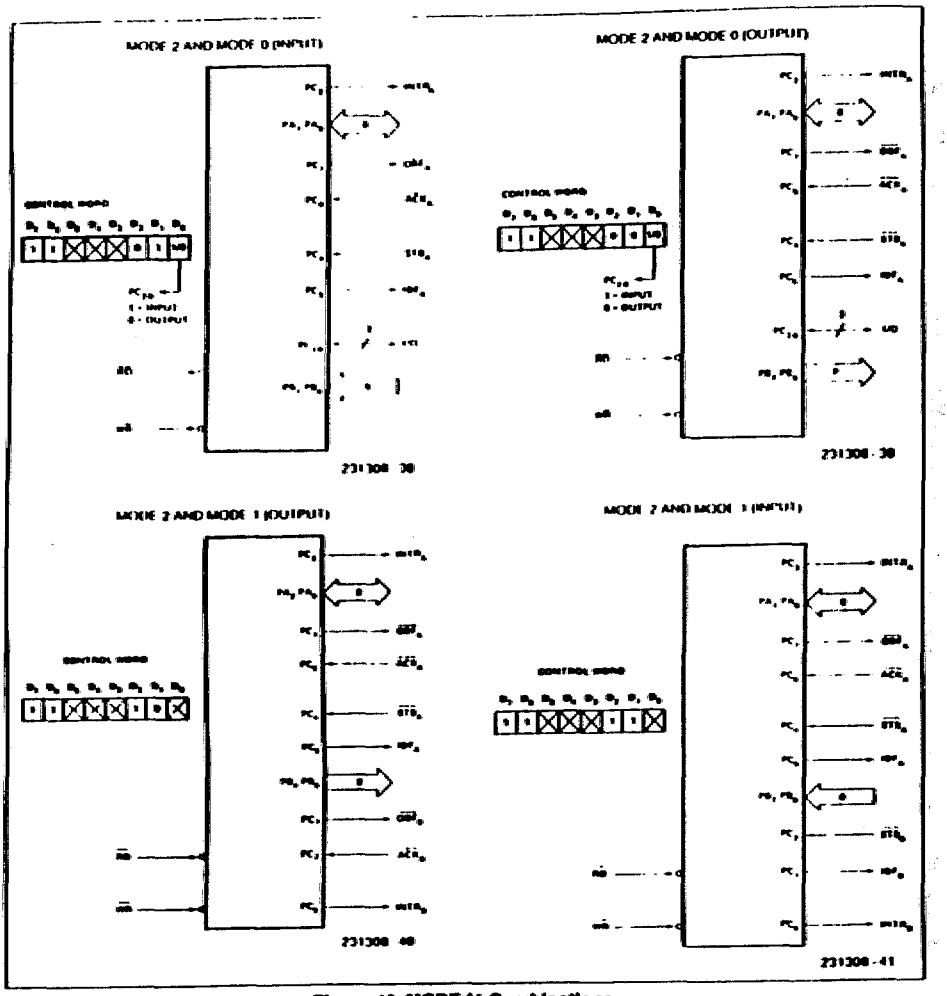


Figure 16. MODE 1/2 Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	⟷	
PA_1	IN	OUT	IN	OUT	⟷	
PA_2	IN	OUT	IN	OUT	⟷	
PA_3	IN	OUT	IN	OUT	⟷	
PA_4	IN	OUT	IN	OUT	⟷	
PA_5	IN	OUT	IN	OUT	⟷	
PA_6	IN	OUT	IN	OUT	⟷	
PA_7	IN	OUT	IN	OUT	⟷	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs—

All input lines can be accessed during a normal Port C read.

If Programmed as Outputs—

Bits in C upper (PC_7–PC_4) must be individually accessed using the bit set/reset function

Bits in C lower (PC_3–PC_0) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

Source Current Capability on Port B and Port C

Any set of eight output buffers, selected randomly from Ports B and C can source 1 mA at 1.5 volts. This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

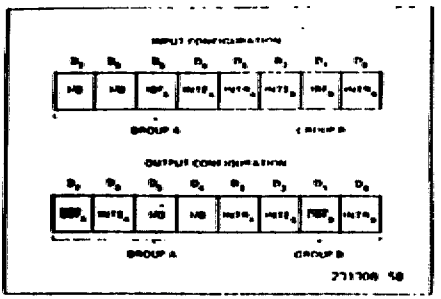


Figure 17. MODE 1 Status Word Format

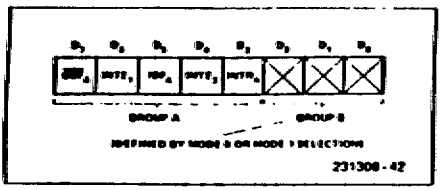


Figure 18. MODE 2 Status Word Format

APPLICATIONS OF THE 8255A

The 8255A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 8255A to exactly "fit" the application. Figures 19 through 25 represent a few examples of typical applications of the 8255A.

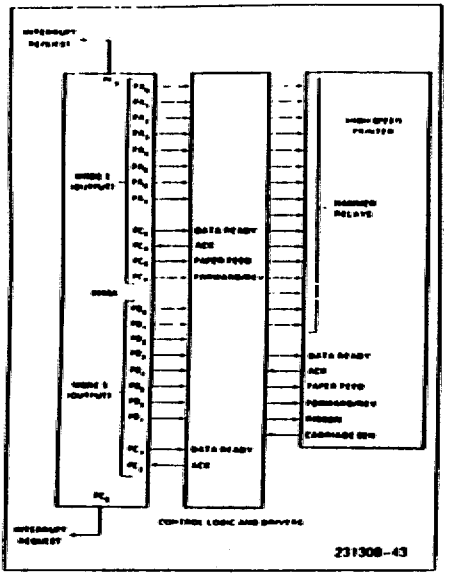


Figure 19. Printer Interface

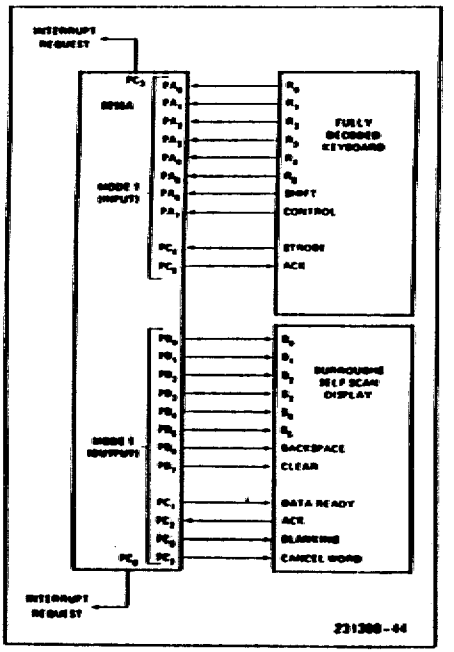


Figure 20. Keyboard and Display Interface

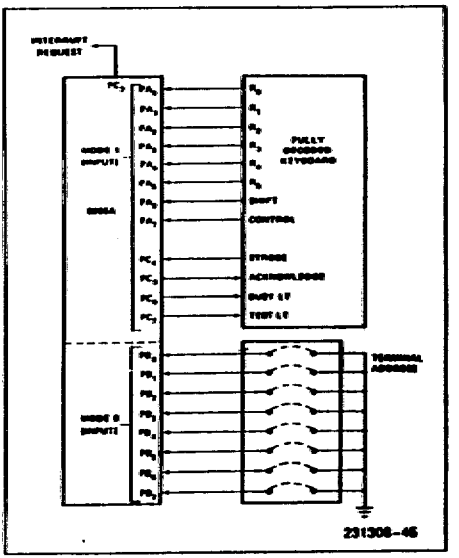


Figure 21. Keyboard and Terminal Address Interface

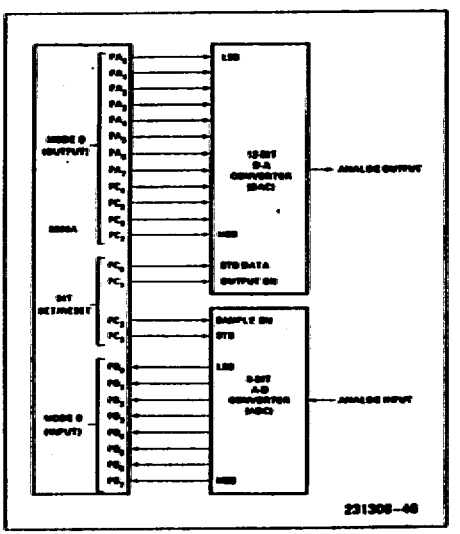


Figure 22. Digital to Analog, Analog to Digital

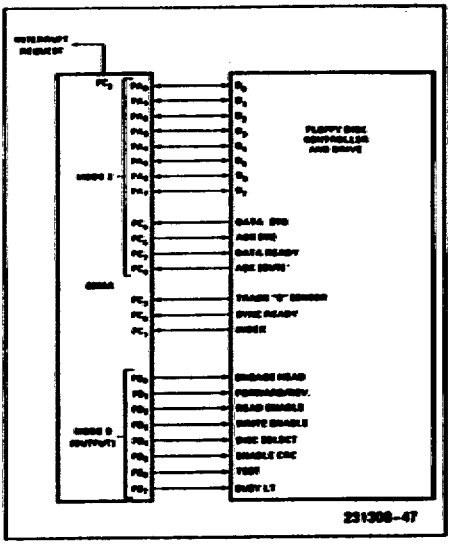


Figure 23. Basic Floppy Disk Interface

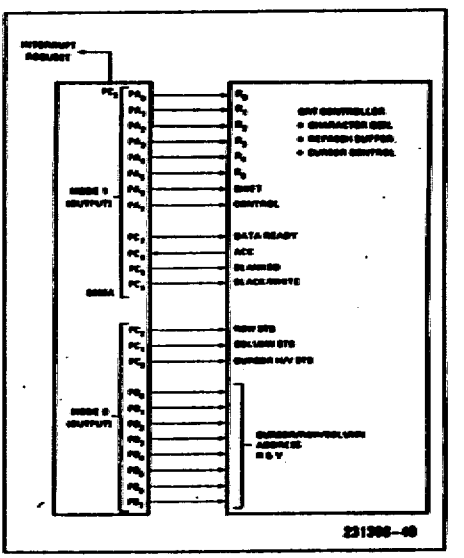


Figure 24. Basic CRT Controller Interface

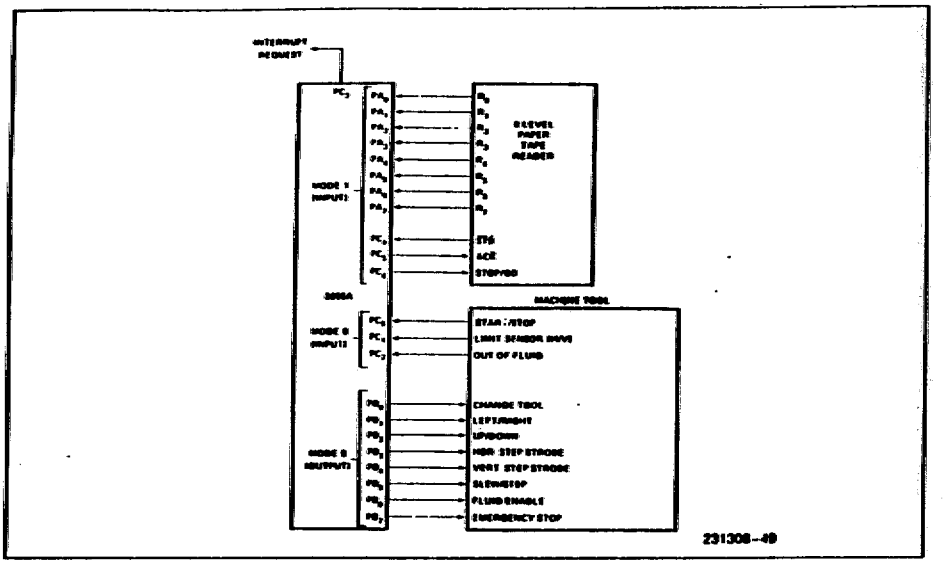


Figure 25. Machine Tool Controller Interface

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = +5V ± 10%, GND = 0V*

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL} (DB)	Output Low Voltage (Data Bus)		0.45*	V	I_{OL} = 2.5 mA
V_{OL} (PER)	Output Low Voltage (Peripheral Port)		0.45*	V	I_{OL} = 1.7 mA
V_{OH} (DB)	Output High Voltage (Data Bus)	2.4		V	I_{OH} = −400 μA
V_{OH} (PER)	Output High Voltage (Peripheral Port)	2.4		V	I_{OH} = −200 μA
I_{DAR}[1]	Darlington Drive Current	−1.0	−4.0	mA	R_{EXT} = 750Ω; V_{EXT} = 1.5V
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0.45V

NOTE:
1. Available on any 8 pins from Port B and C

CAPACITANCE T_A = 25°C, V_{CC} = GND = 0V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	f_c = 1 MHz[4]
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND[4]

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = +5V ± 10%, GND = 0V*

Bus Parameters

READ

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
t_{AR}	Address Stable before READ	0		0		ns
t_{RA}	Address Stable after READ	0		0		ns
t_{RR}	READ Pulse Width	300		300		ns
t_{RD}	Data Valid from READ[1]		250		200	ns
t_{DF}	Data Float after READ	10	150	10	100	ns
t_{RV}	Time between READs and/or WRITEs	850		850		ns

WRITE

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
t_{AW}	Address Stable before WRITE	0		0		ns
t_{WA}	Address Stable after WRITE	20		20		ns
t_{WW}	WRITE Pulse Width	400		300		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		100		ns
t_{WD}	Data Valid after WRITE	30		30		ns

OTHER TIMINGS

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
t_{WB}	WR = 1 to Output[1]		350		350	ns
t_{IR}	Peripheral Data before RD	0		0		ns
t_{HR}	Peripheral Data after RD	0		0		ns
t_{AK}	ACK Pulse Width	300		300		ns
t_{ST}	STB Pulse Width	500		500		ns
t_{PS}	Per. Data before T.E. of STB	0		0		ns
t_{PH}	Per. Data after T.E. of STB	180		180		ns
t_{AD}	ACK = 0 to Output[1]		300		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	20	250	ns

A.C. CHARACTERISTICS (Continued)

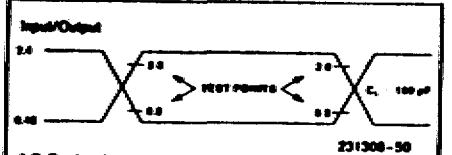
OTHER TIMINGS (Continued)

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
t_{WOB}	WR = 1 to OBF = 0(1)		650		650	ns
t_{AOB}	ACK = 0 to OBF = 1(1)		350		350	ns
t_{SIB}	STB = 0 to IBF = 1(1)		300		300	ns
t_{RIB}	RD = 1 to IBF = 0(1)		300		300	ns
t_{RIT}	RD = 0 to INTR = 0(1)		400		400	ns
t_{SIT}	STB = 1 to INTR = 1(1)		300		300	ns
t_{AIT}	ACK = 1 to INTR = 1(1)		350		350	ns
t_{WIT}	WR = 0 to INTR = 0(1, 3)		650		650	ns

NOTES:
1. Test Conditions: C_L = 150 pF.
2. Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.
3. INTR ↑ may occur as early as $\overline{WR}$ ↓.
4. Sampled, not 100% tested.

*For Extended Temperature EXPRESS, use M8255A electrical parameters.

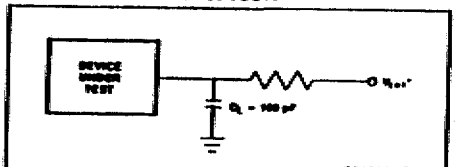
A.C. TESTING INPUT, OUTPUT WAVEFORM



231308-50

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT

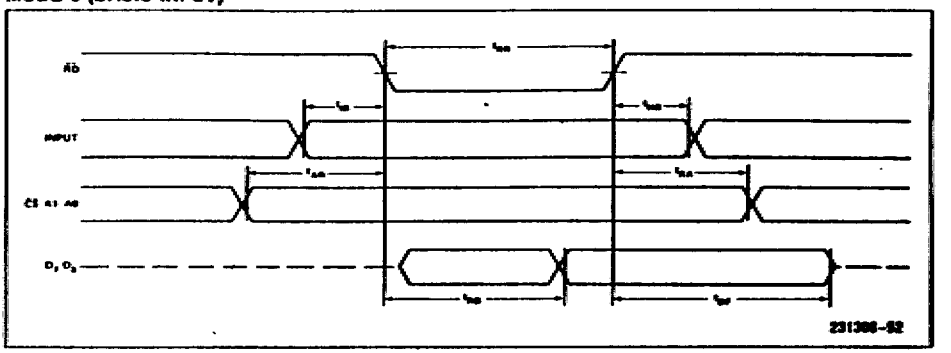


231308-51

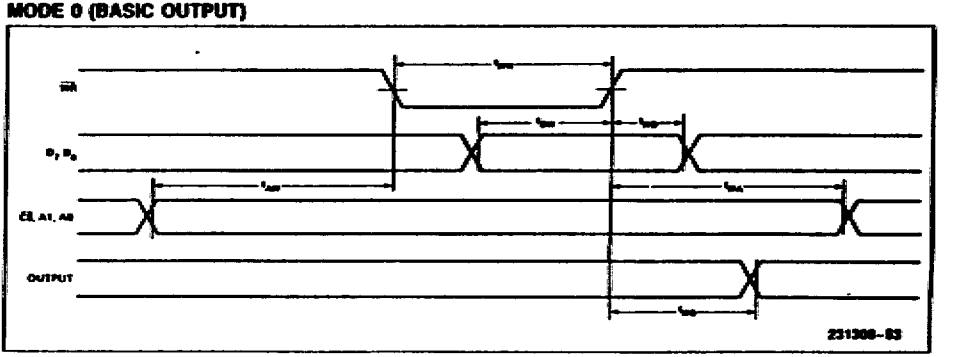
V_{EXT} is set at various voltages during testing to guarantee the specification. C_L includes jig capacitance

WAVEFORMS

MODE 0 (BASIC INPUT)

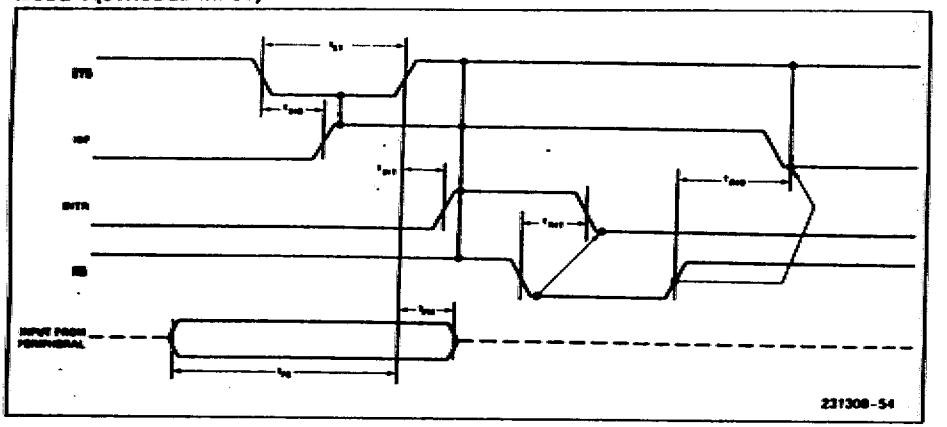


MODE 0 (BASIC OUTPUT)

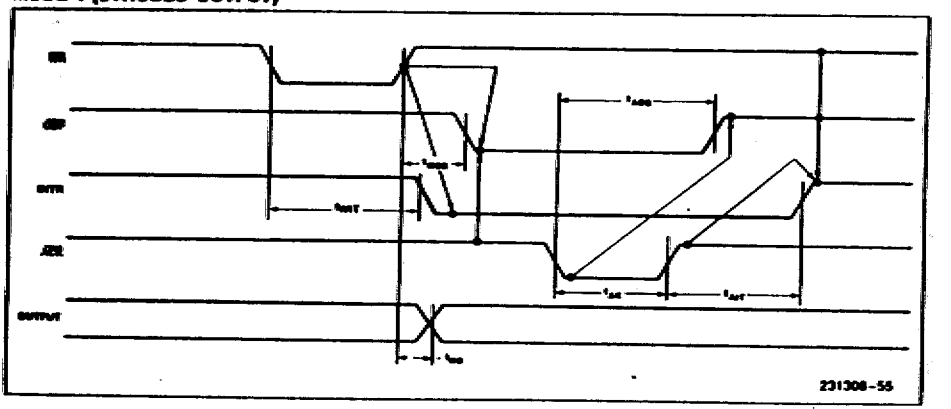


WAVEFORMS (Continued)

MODE 1 (STROBED INPUT)

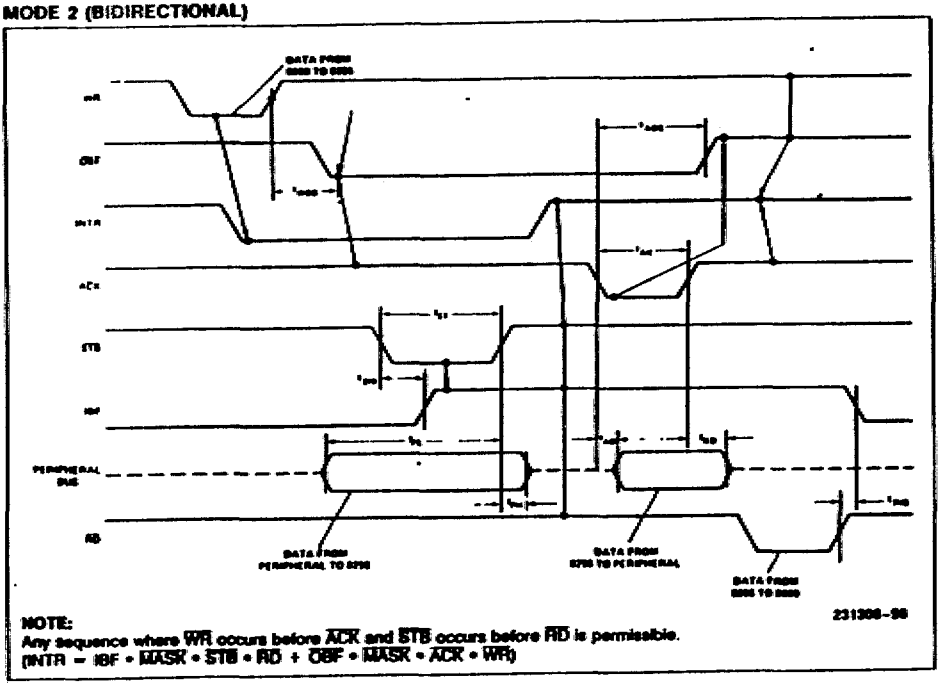


MODE 1 (STROBED OUTPUT)



WAVEFORMS (Continued)

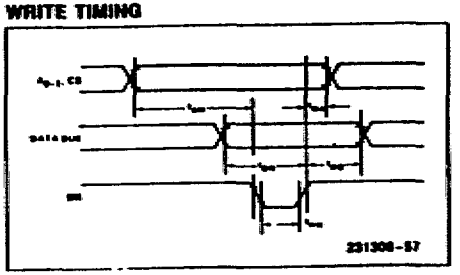
MODE 2 (BIDIRECTIONAL)



231308-56

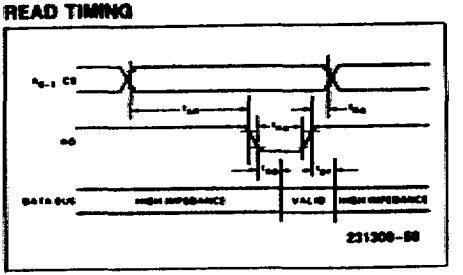
NOTE:
Any sequence where $\overline{WR}$ occurs before ACK and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • MASK • ACK • $\overline{WR}$)

WRITE TIMING



231308-57

READ TIMING



231308-58

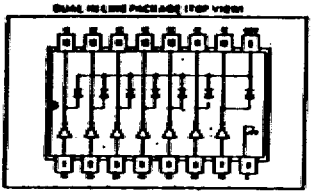
TYPES ULN2001A THRU ULN2006A DARLINGTON TRANSISTOR ARRAYS

[illegible]

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500 mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible with Various Types of Logic
- Relay Driver Applications
- Designed to be Interchangeable with Sprague ULN2001A Series

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

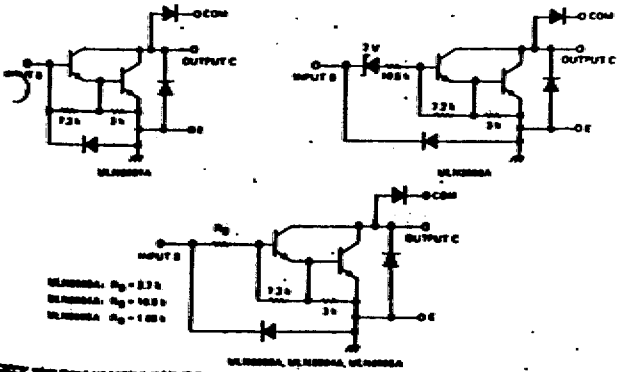


description

The ULN2001A, ULN2002A, ULN2003A, ULN2004A, and ULN2005A are monolithic high-voltage, high-current darlington transistor arrays. Each comprises seven npn darlington pairs. All units feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single darlington pair is 500 milliamperes. Outputs and inputs may each be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-volt (tolerable) interchangeable versions, see the SN75468 through SN75469.

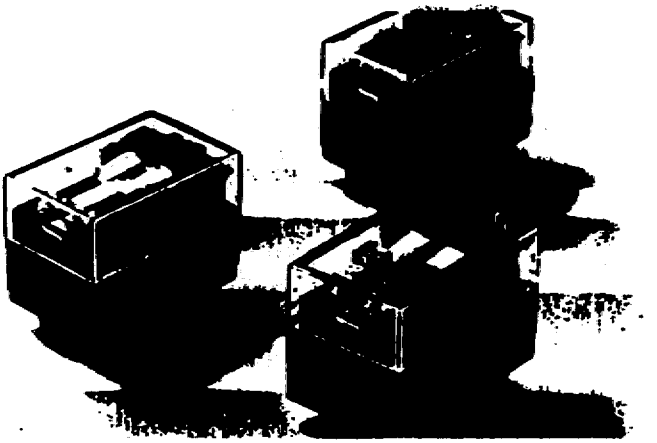
The ULN2001A is a general-purpose array and may be used with DTL, TTL, P-MOS, CMOS, etc. The ULN2002A is specifically designed for use with 14- to 25-volt P-MOS devices and each input has a zener diode and resistor in series to limit the input current to a safe limit. The ULN2003A has a 2.7-kΩ series base resistor for each darlington pair. This allows operation directly with TTL or 5-volt CMOS. The ULN2004A has an appropriate series input resistor to allow its operation directly from CMOS or P-MOS operating supply voltages of 6 to 15 volts. The required input current is below that of the ULN2003A while the required voltage is less than that required by the ULN2003A. The ULN2005A has a 1.05-kΩ series base resistor and is especially designed for use with TTL where higher output current is required and loading of the driving source is not a concern.

schematics (each darlington pair)



FBR321 SERIES

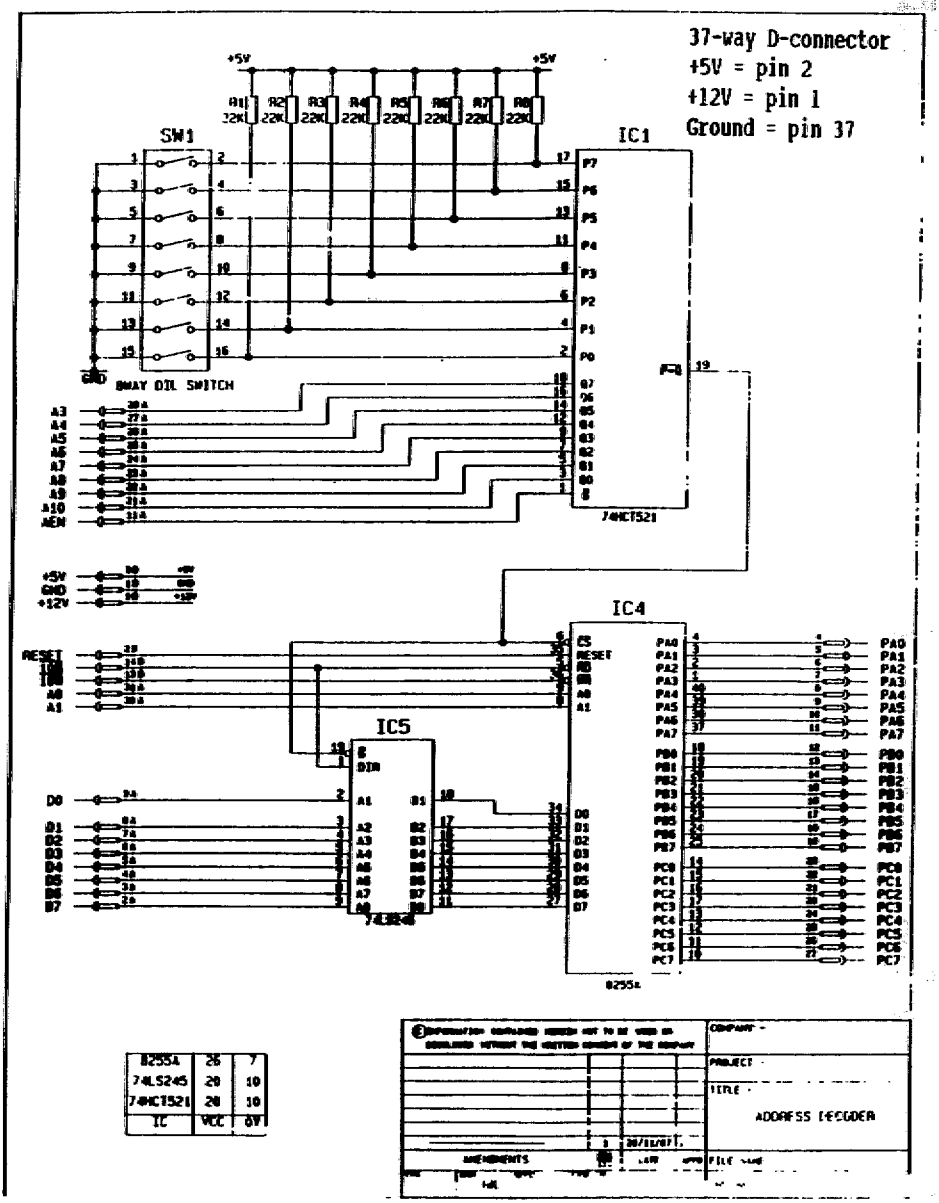
2 x C/O 3A-24VDC; 3A-100VAC



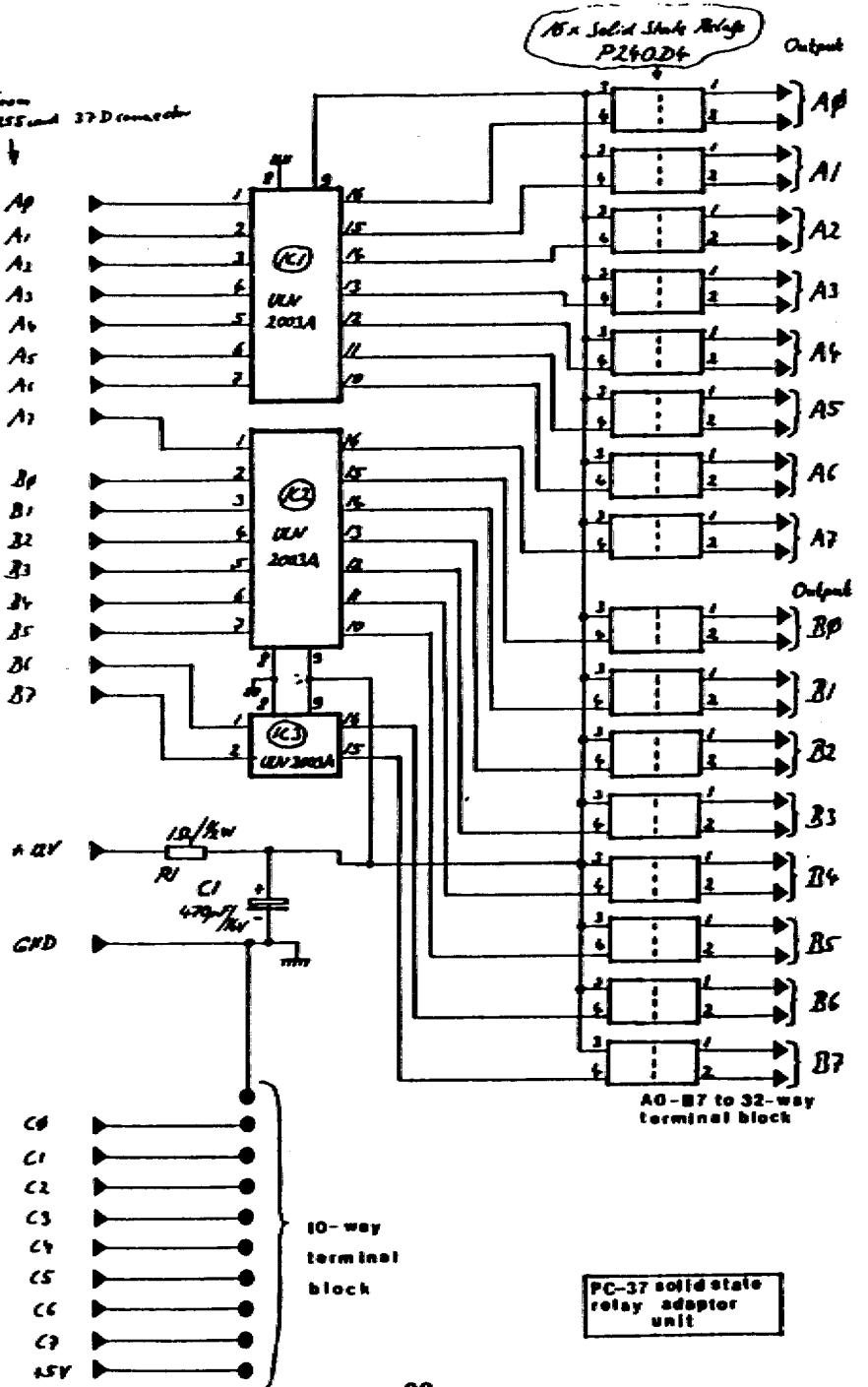
ENGINEERING DATA

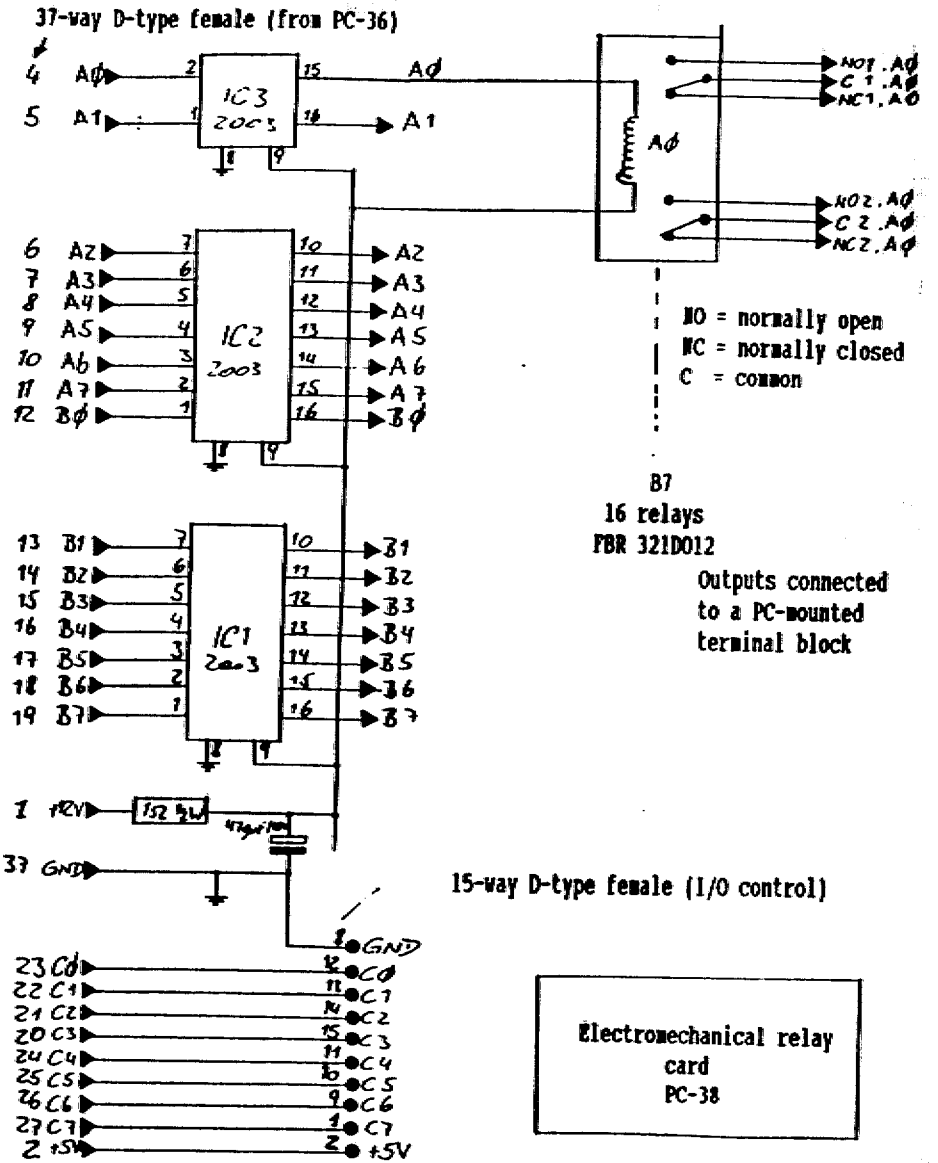
Item	Specifications
Contact Arrangement	DPDT
Contact Rating	3A at 24V DC, resistive 3A at 100V AC, resistive
Initial Contact Resistance	100mΩ max. at 6V DC, 0.5A
Contact Material	Gold overlay silver
Rated Coil Voltage	5, 6, 9, 12, 24V DC
Coil Power Dissipation	0.6W approx. at rated voltage
Coil Temperature Rise	45°C approx. at rated voltage
Insulation Resistance	100MΩ min. at 500V DC (initial)
Dielectric Withstanding Voltage	500V AC for 1 minute
Operate Time	20ms max. at rated voltage
Release Time	10ms max.
Life Expectancy, Mechanical	10×10^6 ops. min.
Electrical	100×10^3 ops. min. at rated load
Vibration	10 to 55Hz (Dual amplitude 1.5mm)
Shock	10G (11ms)
Temperature Range	-30°C to +50°C
Weight	12 gr. approx.

Contact Arrangement	Rated Voltage in V DC	Coil Resistance in Ω ± 15% at 20°C	Pick-up Voltage at 20°C	Type No.
DPDT	12	230	less than 80% of rated voltage	FBR321D012



8255A	26	7
74LS245	20	10
74HCT521	20	10
IC	VCC	0V


16 x Solid State Relays
P240D4
Outputs
from 8255 and 37D connector
A0
A1
A2
A3
A4
A5
A6
A7
B0
B1
B2
B3
B4
B5
B6
B7
IC1
IC2
IC3
ULN 2003A
+12V
10/½W
R1
C1
470μF/16V
GND
C0
C1
C2
C3
C4
C5
C6
C7
+5V
10-way terminal block
A0-B7 to 32-way terminal block
PC-37 solid state relay adaptor unit


37-way D-type female (from PC-36)
IC3 2003
IC2 2003
IC1 2003
A0
A1
A2
A3
A4
A5
A6
A7
B0
B1
B2
B3
B4
B5
B6
B7
+12V
GND
NO1, A0
C1, A0
NC1, A0
NO2, A0
C2, A0
NC2, A0
NO = normally open
NC = normally closed
C = common
B7
16 relays
FBR 321D012
Outputs connected to a PC-mounted terminal block
15-way D-type female (I/O control)
GND
C0
C1
C2
C3
C4
C5
C6
C7
+5V
Electromechanical relay card
PC-38

PC-36 8255 I/O card

Multiple address version

In 1988, a new version of the PC-36 was introduced, which superseded the previous version. There are two basic differences between the new and the old versions:

The card has a new addressing system with 256 possible address locations, selected by DIP switch.

The PC-36 now occupies 8 byte locations rather than four. The four actual registers are duplicated in this space. For example, if the base address is selected as 778H, then the four registers appear at locations 778-77B as well as locations 77C-77F, and may be accessed at either location.

In all other respects the new PC-36 is identical to the older version. The two addresses available on the old PC-36 can be duplicated on the new:

77C (factory default for old and new cards): SW4 on, all other switches off.

7FC: all switches off.

The switch settings for all addresses follow.

Switch Settings. The following table shows which switches must be ON for each address.

0H	SW1, SW2, SW3, SW4, SW5, SW6, SW7, SW8
8H	SW1, SW2, SW3, SW4, SW5, SW6, SW7
10H	SW1, SW2, SW3, SW4, SW5, SW6, SW8
18H	SW1, SW2, SW3, SW4, SW5, SW6
20H	SW1, SW2, SW3, SW4, SW5, SW7, SW8
28H	SW1, SW2, SW3, SW4, SW5, SW7
30H	SW1, SW2, SW3, SW4, SW5, SW8
38H	SW1, SW2, SW3, SW4, SW5
40H	SW1, SW2, SW3, SW4, SW6, SW7, SW8
48H	SW1, SW2, SW3, SW4, SW6, SW7
50H	SW1, SW2, SW3, SW4, SW6, SW8
58H	SW1, SW2, SW3, SW4, SW6
60H	SW1, SW2, SW3, SW4, SW7, SW8
68H	SW1, SW2, SW3, SW4, SW7
70H	SW1, SW2, SW3, SW4, SW8
78H	SW1, SW2, SW3, SW4
80H	SW1, SW2, SW3, SW5, SW6, SW7, SW8
88H	SW1, SW2, SW3, SW5, SW6, SW7
90H	SW1, SW2, SW3, SW5, SW6, SW8
98H	SW1, SW2, SW3, SW5, SW6
A0H	SW1, SW2, SW3, SW5, SW7, SW8
A8H	SW1, SW2, SW3, SW5, SW7
B0H	SW1, SW2, SW3, SW5, SW8
B8H	SW1, SW2, SW3, SW5
C0H	SW1, SW2, SW3, SW6, SW7, SW8
C8H	SW1, SW2, SW3, SW6, SW7
D0H	SW1, SW2, SW3, SW6, SW8
D8H	SW1, SW2, SW3, SW6
E0H	SW1, SW2, SW3, SW7, SW8
E8H	SW1, SW2, SW3, SW7
F0H	SW1, SW2, SW3, SW8
F8H	SW1, SW2, SW3
100H	SW1, SW2, SW4, SW5, SW6, SW7, SW8
108H	SW1, SW2, SW4, SW5, SW6, SW7
110H	SW1, SW2, SW4, SW5, SW6, SW8
118H	SW1, SW2, SW4, SW5, SW6
120H	SW1, SW2, SW4, SW5, SW7, SW8
128H	SW1, SW2, SW4, SW5, SW7
130H	SW1, SW2, SW4, SW5, SW8
138H	SW1, SW2, SW4, SW5
140H	SW1, SW2, SW4, SW6, SW7, SW8
148H	SW1, SW2, SW4, SW6, SW7
150H	SW1, SW2, SW4, SW6, SW8
158H	SW1, SW2, SW4, SW6
160H	SW1, SW2, SW4, SW7, SW8
168H	SW1, SW2, SW4, SW7
170H	SW1, SW2, SW4, SW8
178H	SW1, SW2, SW4
180H	SW1, SW2, SW5, SW6, SW7, SW8
188H	SW1, SW2, SW5, SW6, SW7
190H	SW1, SW2, SW5, SW6, SW8
198H	SW1, SW2, SW5, SW6
1A0H	SW1, SW2, SW5, SW7, SW8
1A8H	SW1, SW2, SW5, SW7
1B0H	SW1, SW2, SW5, SW8
1B8H	SW1, SW2, SW5
1C0H	SW1, SW2, SW6, SW7, SW8
1C8H	SW1, SW2, SW6, SW7
1D0H	SW1, SW2, SW6, SW8
1D8H	SW1, SW2, SW6
1E0H	SW1, SW2, SW7, SW8
1E8H	SW1, SW2, SW7
1F0H	SW1, SW2, SW8
1F8H	SW1, SW2
200H	SW1, SW3, SW4, SW5, SW6, SW7, SW8
208H	SW1, SW3, SW4, SW5, SW6, SW7
210H	SW1, SW3, SW4, SW5, SW6, SW8
218H	SW1, SW3, SW4, SW5, SW6
220H	SW1, SW3, SW4, SW5, SW7, SW8
228H	SW1, SW3, SW4, SW5, SW7
230H	SW1, SW3, SW4, SW5, SW8
238H	SW1, SW3, SW4, SW5
240H	SW1, SW3, SW4, SW6, SW7, SW8
248H	SW1, SW3, SW4, SW6, SW7
250H	SW1, SW3, SW4, SW6, SW8
258H	SW1, SW3, SW4, SW6
260H	SW1, SW3, SW4, SW7, SW8
268H	SW1, SW3, SW4, SW7
270H	SW1, SW3, SW4, SW8
278H	SW1, SW3, SW4
280H	SW1, SW3, SW5, SW6, SW7, SW8
288H	SW1, SW3, SW5, SW6, SW7
290H	SW1, SW3, SW5, SW6, SW8
298H	SW1, SW3, SW5, SW6
2A0H	SW1, SW3, SW5, SW7, SW8
2A8H	SW1, SW3, SW5, SW7
2B0H	SW1, SW3, SW5, SW8
2B8H	SW1, SW3, SW5
2C0H	SW1, SW3, SW6, SW7, SW8
2C8H	SW1, SW3, , SW6, SW7
2D0H	SW1, SW3, SW6, SW8
2D8H	SW1, SW3, SW6
2E0H	SW1, SW3, SW7, SW8
2E8H	SW1, SW3, SW7
2F0H	SW1, SW3, SW8
2F8H	SW1, SW3
300H	SW1, SW4, SW5, SW6, SW7, SW8
308H	SW1, SW4, SW5, SW6, SW7
310H	SW1, SW4, SW5, SW6, SW8
318H	SW1, SW4, SW5, SW6
320H	SW1, SW4, SW5, SW7, SW8
328H	SW1, SW4, SW5, SW7
330H	SW1, SW4, SW5, SW8
338H	SW1, SW4, SW5

340H	SW1, SW4, SW6, SW7, SW8
348H	SW1, SW4, SW6, SW7
350H	SW1, SW4, SW6, SW8
358H	SW1, SW4, SW6
360H	SW1, SW4, SW7, SW8
368H	SW1, SW4, SW7
370H	SW1, SW4, SW8
378H	SW1, SW4
380H	SW1, SW5, SW6, SW7, SW8
388H	SW1, SW5, SW6, SW7
390H	SW1, SW5, SW6, SW8
398H	SW1, SW5, SW6
3A0H	SW1, SW5, SW7, SW8
3A8H	SW1, SW5, SW7
3B0H	SW1, SW5, SW8
3B8H	SW1, SW5
3C0H	SW1, SW6, SW7, SW8
3C8H	SW1, SW6, SW7
3D0H	SW1, SW6, SW8
3D8H	SW1, SW6
3E0H	SW1, SW7, SW8
3E8H	SW1, SW7
3F0H	SW1, SW8
3F8H	SW1
400H	SW2, SW3, SW4, SW5, SW6, SW7, SW8
408H	SW2, SW3, SW4, SW5, SW6, SW7
410H	SW2, SW3, SW4, SW5, SW6, SW8
418H	SW2, SW3, SW4, SW5, SW6
420H	SW2, SW3, SW4, SW5, SW7, SW8
428H	SW2, SW3, SW4, SW5, SW7
430H	SW2, SW3, SW4, SW5, SW8
438H	SW2, SW3, SW4, SW5
440H	SW2, SW3, SW4, SW6, SW7, SW8
448H	SW2, SW3, SW4, SW6, SW7
450H	SW2, SW3, SW4, SW6, SW8
458H	SW2, SW3, SW4, SW6
460H	SW2, SW3, SW4, SW7, SW8
468H	SW2, SW3, SW4, SW7
470H	SW2, SW3, SW4, SW8
478H	SW2, SW3, SW4
480H	SW2, SW3, SW5, SW6, SW7, SW8
488H	SW2, SW3, SW5, SW6, SW7
490H	SW2, SW3, SW5, SW6, SW8
498H	SW2, SW3, SW5, SW6
4A0H	SW2, SW3, SW5, SW7, SW8
4A8H	SW2, SW3, SW5, SW7
4B0H	SW2, SW3, SW5, SW8
4B8H	SW2, SW3, SW5
4C0H	SW2, SW3, SW6, SW7, SW8
4C8H	SW2, SW3, SW6, SW7
4D0H	SW2, SW3, SW6, SW8
4D8H	SW2, SW3, SW6
4E0H	SW2, SW3, SW7, SW8
4E8H	SW2, SW3, SW7
4F0H	SW2, SW3, SW8
500H	SW2, SW4, SW5, SW6, SW7, SW8
508H	SW2, SW4, SW5, SW6, SW7
510H	SW2, SW4, SW5, SW6, SW8
518H	SW2, SW4, SW5, SW6
520H	SW2, SW4, SW5, SW7, SW8
528H	SW2, SW4, SW5, SW7
530H	SW2, SW4, SW5, SW8
538H	SW2, SW4, SW5
540H	SW2, SW4, SW6, SW7, SW8
548H	SW2, SW4, SW6, SW7
550H	SW2, SW4, SW6, SW8
558H	SW2, SW4, SW6
560H	SW2, SW4, SW7, SW8
568H	SW2, SW4, SW7
570H	SW2, SW4, SW8
578H	SW2, SW4
580H	SW2, SW5, SW6, SW7, SW8
588H	SW2, SW5, SW6, SW7
590H	SW2, SW5, SW6, SW8
598H	SW2, SW5, SW6
5A0H	SW2, SW5, SW7, SW8
5A8H	SW2, SW5, SW7
5B0H	SW2, SW5, SW8
5B8H	SW2, SW5
5C0H	SW2, SW6, SW7, SW8
5C8H	SW2, SW6, SW7
5D0H	SW2, SW6, SW8
5D8H	SW2, SW6
5E0H	SW2, SW7, SW8
5E8H	SW2, SW7
5F0H	SW2, SW8
5F8H	SW2
600H	SW3, SW4, SW5, SW6, SW7, SW8
608H	SW3, SW4, SW5, SW6, SW7
610H	SW3, SW4, SW5, SW6, SW8
618H	SW3, SW4, SW5, SW6
620H	SW3, SW4, SW5, SW7, SW8
628H	SW3, SW4, SW5, SW7
630H	SW3, SW4, SW5, SW8
638H	SW3, SW4, SW5
640H	SW3, SW4, SW6, SW7, SW8
648H	SW3, SW4, SW6, SW7
650H	SW3, SW4, SW6, SW8
658H	SW3, SW4, SW6
660H	SW3, SW4, SW7, SW8
668H	SW3, SW4, SW7
670H	SW3, SW4, SW8
678H	SW3, SW4
680H	SW3, SW5, SW6, SW7, SW8
688H	SW3, SW5, SW6, SW7
690H	SW3, SW5, SW6, SW8
698H	SW3, SW5, SW6
6A0H	SW3, SW5, SW7, SW8
6A8H	SW3, SW5, SW7
6B0H	SW3, SW5, SW8
6B8H	SW3, SW5
6C0H	SW3, SW6, SW7, SW8
6C8H	SW3, SW6, SW7
6D0H	SW3, SW6, SW8
6D8H	SW3, SW6

6E0H	SW3, SW7, SW8
6E8H	SW3, SW7
6F0H	SW3, SW8
6F8H	SW3
700H	SW4, SW5, SW6, SW7, SW8
708H	SW4, SW5, SW6, SW7
710H	SW4, SW5, SW6, SW8
718H	SW4, SW5, SW6
720H	SW4, SW5, SW7, SW8
728H	SW4, SW5, SW7
730H	SW4, SW5, SW8
738H	SW4, SW5
740H	SW4, SW6, SW7, SW8
748H	SW4, SW6, SW7
750H	SW4, SW6, SW8
758H	SW4, SW6
760H	SW4, SW7, SW8
768H	SW4, SW7
770H	SW4, SW8
778H	SW4
780H	SW5, SW6, SW7, SW8
788H	SW5, SW6, SW7
790H	SW5, SW6, SW8
798H	SW5, SW6
7A0H	SW5, SW7, SW8
7A8H	SW5, SW7
7B0H	SW5, SW8
7B8H	SW5
7C0H	SW6, SW7, SW8
7C8H	SW6, SW7
7D0H	SW6, SW8
7D8H	SW6
7E0H	SW7, SW8
7E8H	SW7
7F0H	SW8
7F8H	None