

PC-36 and PC-36B

User's Manual

April 1992 Edition

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Glossary

Acknowledge	A handshake line which is used by the receiving device to indicate that it has read the transmitted data.
DIP	An abbreviation for Dual In-line Package.
Handshake Lines	Dedicated signals which allow two different devices to exchange data under asynchronous hardware control. The 8255 on the PC-36B can provide handshaking lines.
LSB	Context sensitive abbreviation for either Least Significant Byte or Least Significant Bit
MSB	Context sensitive abbreviation for either Most Significant Byte or Most Significant Bit
PIA	Peripheral Interface Adapter. The 8255 on the PC-36B board is a PIA. Also referred to as a PPI (Programmable Peripheral Interface).
Programming an 8255 PIA	Writing a Control Word to the 8255 PIA's Control Register. All three ports are configured simultaneously.
Strobe	A handshaking line which is used to signal to a receiving device that there is data to be read.

1

Introduction

This chapter describes the PC-36 and lists the contents of the PC-36 package. For the remainder of this manual, the term PC-36 will refer to both the PC-36 and PC-36B, unless specifically noted.

Overview

The PC-36 is a general purpose digital input/output board. It is built around the industry standard 8255 programmable peripheral interface (PPI) adapter.

The 8255 featured on the PC-36B is the high speed version of the standard 8255AC-2.

The 8255 controls 24 lines of digital I/O. It is very flexible and powerful when interfacing to peripheral equipment and can be programmed for almost any 8-bit or 16-bit I/O application. The 8255 can operate in either unidirectional or bidirectional mode, with or without hardware handshaking.

8255 PIAs

PC-36 can be used for versatile interfacing to:

- Other PC computers, for example another PC with another PC-36 installed, or a PC-14 or PC-192.
- Any other computer with an 8-bit or 16-bit parallel interface.
- Centronics compatible printers and plotters.
- Relays (electro-mechanical and solid state) and opto-isolators.
- Switches of various types.
- Relay boards (PC-37 and PC-38) and industrial I/O mounting racks.
- Panel meters, instruments and test equipment which have digital readouts and controls.
- Sensors, transducers, instruments and test equipment with frequency (pulse) outputs and controls.

These are a few examples of where the PC-36 can serve as a digital I/O system controller in laboratories, industry, production or part of a dedicated instrument for process monitoring and control.

The board plugs into any fully bussed slot of an IBM PC/XT/AT or PS/2 model 25 or 30 or any compatible ISA or EISA machine, including 8088, 286, 386 or 486 based systems. It occupies four consecutive I/O addresses. The base I/O address can be set in the range 0h to 7F8h with a DIP switch on the board.

The PC-36B features wait state generation circuitry. This ensures that all host computer's I/O bus cycles are long enough for the PC-36B. Zero, 1, 2, 4 or 8 wait states are selectable with a jumper block on the board.

The power supplies +12V, +5V (and -12V, -5V on the PC-36B) and ground are available on the external connector of the board.

Features

- Twenty four lines of programmable digital inputs or outputs.
- Three modes of parallel data transfer:
 - Simple inputs and outputs.
 - Strobed inputs and outputs with handshaking.
 - Bidirectional input/output with handshaking.
- Jumper selectable wait state generator on the PC-36B allows trouble free operation in all high speed systems.
- All external connections (including all power supplies) available directly at the rear of the host computer.
- Wide base address selection range; many boards may be paralleled.
- TTL and CMOS compatible
- Driver software supplied, complete with C and BASIC source code.
- Includes LabWindows drivers.

PC-36 package contents

The PC-36 package should contain:

- PC-36 interface board.
- The PC-36 and PC-36B user's manual.
- The Data Acquisition Driver Software Manual.
- Two 5¼" 360 Kb diskettes containing PC-36B utility and demonstration software and the Data Acquisition Driver Library.

If the package is missing any of the components or damaged in any way, the contact your distributor.

Installation

Configuration

There are two aspects of the PC-36 that can be configured. These are:

- The base address. This is the address where the computer will find the board. It is set to an address between 0h and 7F8h with the eight switches on the DIP switch block. Note that this address is in the computer's I/O address space.
- PC-36B Wait state generation. If the host computer generates abnormally fast I/O bus cycles then it may be necessary to slow these down when the computer accesses the PC-36B. The board can do this without affecting any other I/O bus cycles. The number of additional wait states inserted in a PC-36B bus cycle is controlled by jumper on the board.

Setting the base address

The PC-36 uses a block of four I/O addresses. The base address setting controls the address where this block begins. This must be set so that the PC-36 does not use any addresses that are used by another device or card. If more than one PC-36 is to be installed in the computer then each card must have a different base address setting.

The base address may be assigned to any location from 0h to 7F8h, on eight byte boundaries. The factory default base address is 310h. Refer to Table 1 below for a guide on addresses used by standard I/O devices and Table 4 in Appendix A for a list of the base address switch settings.

The base address is set by adjusting the eight switches in the DIP switch on the board. Switch number 1 is used to compare address line A10, number 2 for A9 and so on up to switch 8 which is used to compare address line A3. In general, if a switch is set to the off position, then its corresponding address weighting contributes to the base address. See Figure 1 for the DIP switch weightings.

For example switches 2 (corresponding to address line A9), 3 (corresponding to A8) and 7 (corresponding to A4) off yield a base address of $200h + 100h + 10h = 310h$.

Address (hex)	Standard Device
000-1FF	Internal system board
200-20F	Games port
210-217	Expansion unit
220-24F	Reserved
250-257	Not assigned
258-25F	Intel "Above Board"
260-277	Not assigned
278-26F	Reserved
280-2EF	Not assigned
2F0-2F7	LPT2
2F8-2FF	COM2
300-31F	Prototype board
320-32F	Hard disk
330-377	Not assigned
378-37F	LPT1
380-38F	SDLC communications
390-39F	Not assigned
3A0-3AF	Binary communications
3B0-3BF	Monochrome display adapter
3C0-3CF	Reserved
3D0-3DF	Colour graphics adapter
3E0-3E7	Reserved
3E3-3EF	Not assigned
3F0-3F7	Floppy disk
3F8-3FF	COM1
400-FFF	Not used; refer to text

Table 1: Standard I/O Addresses.

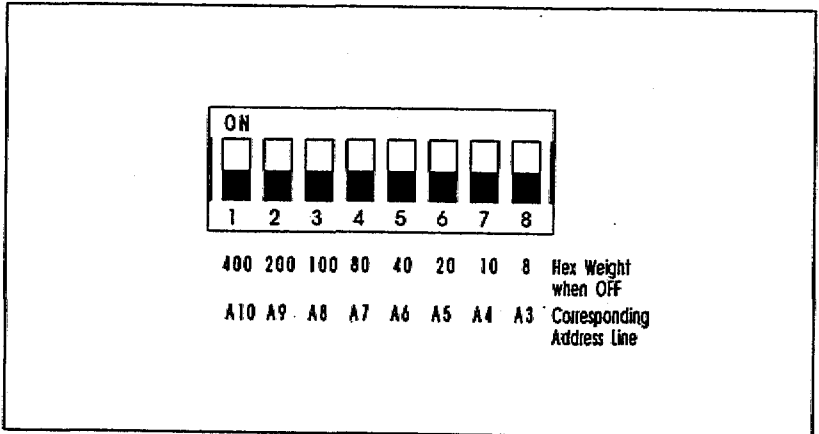


Figure 1: DIP Switch Address Weights [in hex].

I/O Addresses
from 400h to
7FFh

Note that addresses from 400h to 7FFh cannot normally be used because these addresses are not normally decoded by other I/O devices and cards in the 0h to 3FFh range.

The PC-36 however (and most other members of the PC-XX family) can use these additional addresses if (and only if) there is no board or device at address 400h less than the address of the PC-36 or the board at the address 400h less also decodes the extra addresses.

A PC-36 may be installed at address 300h and another PC-36 at address 700h. (400h locations apart.) However it would not be advisable to install a PC-36 at address 778h because the printer port LPT1 uses a base address of 378h and does not normally decode the extra addresses.

Most other members of the PC-XX family of boards decode the extra addresses and may safely be installed 400h locations apart.

If your computer has boards not listed in Table 1 installed (such as LAN adapters, back-up boards or other engineering boards) then consult the manuals for these boards for information on the address ranges used. In most cases a base address of either 300h or 310h is a good choice. Address 310h is also the factory default address.

Generating additional wait states on the PC-36B

The number of additional wait states inserted in I/O bus cycles addressing the PC-36B is controlled by the position of the wait state jumper JP1. This is marked 'Wait State Selection' on the board. Refer to Figure 2 for the wait state jumper positions. The factory default setting is for zero wait states.

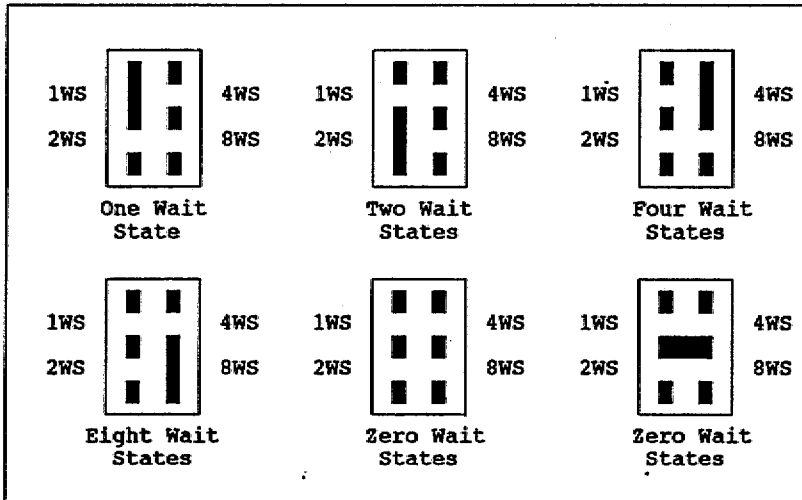


Figure 2: Wait State Jumper Settings.

Only a very small number of computers will require additional wait states. If the PC-36B card in your computer seems to be returning incorrect readings then increase the number of wait states until correct results are obtained. If the card does not produce correct results with the maximum number of additional wait states inserted then either the host computer or the card is faulty and should be serviced.

Installation

Installing the PC-36 is straightforward. You will need a screwdriver to match the screws on the computer's cover and expansion slot bracket.

- a) Switch off the computer and all attached devices.
- b) Unplug the power cord from the computer and all attached devices. Failure to do this may result in hazardous conditions, as there may be dangerous voltage levels present on externally connected cables.
- c) Remove the top cover of the PC or the access port to the I/O channel. If you are not sure how to do this, consult the manual supplied with the system unit.
- d) Choose any unused 8-bit or 16-bit expansion adapter slot and remove the screw from the top of the blank bracket corresponding to the chosen slot. Remove the bracket.
- e) Align the gold plated edge connector of the PC-36 with the edge socket on the computer system board and align the board bracket with the rear adapter slot on the computer's case. Firmly press the board down into the edge socket. Ensure that the board's edge connector is seated in the socket and has not slipped sideways past the socket.
- f) Tighten the mounting bracket of the PC-36 to the back panel rail of the computer.
- g) Replace the computer's cover. Plug in all cords and cables. Switch on the power. The PC-36 is now installed and ready for operation.

Interconnections

The PC-36 plugs into any of the computer's expansion slots, along the board's gold plated edge connector. The board communicates to the external world via a connector mounted in its bracket. This chapter describes these connectors.

Connections to the computer backplane

The PC-36 board may be plugged into any slot of the computer backplane (with the exception of the J8 slot of IBM XT's). All communication to and from the host computer is via this connector. The board forms part of the processor's I/O space.

If the PC-36 sometimes behaves erratically then there is the possibility that the gold plated contacts on the edge connector may have become dirty or abraded, especially if the card is installed and removed many times from various different computers. This condition can be corrected simply by cleaning the contacts with an ordinary pencil eraser.

User connector

The PC-36 interfaces to the external world via a 37 way D-type male connector mounted in the board's bracket.

The DB37 connector carries the following signals:

- The Port A, Port B and Port C digital input/output/handshake lines of the 8255.
- Power supplies of +5V, -5V, +12V, -12V and digital ground.

Figure 3 shows these connections, together with their pin assignments. Note that the pin connections refer to the pin numbers of the connector when looking into the connector from the rear of the computer. The pin numbers are embossed onto the connector itself.

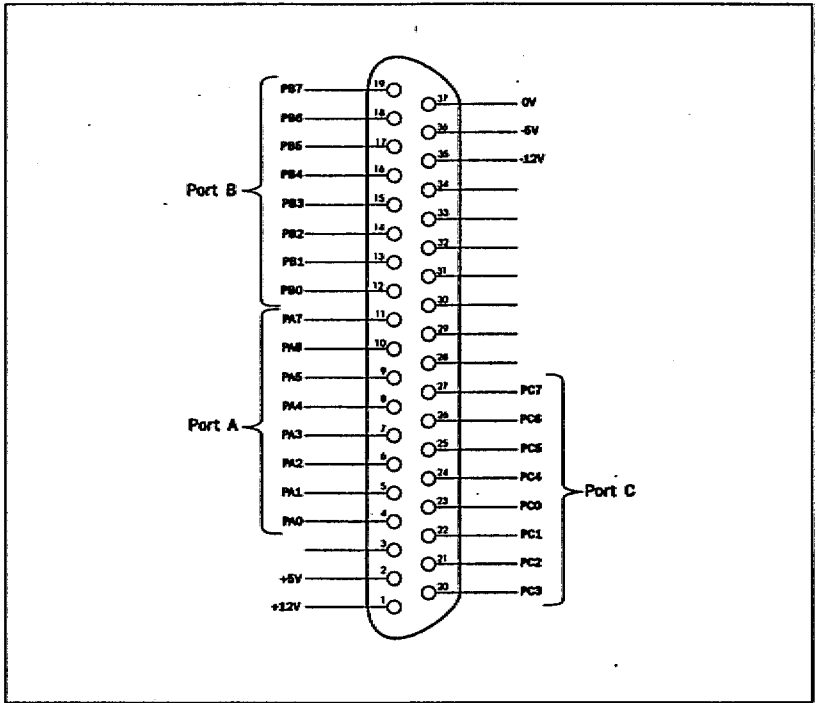


Figure 3: PC-36 connector, as seen from the rear of the PC.

Some of the lines of Port C take on different meanings when an 8255 is programmed to operate in strobed input or output mode or bidirectional bus mode. They are summarised in the following table and described below that. See Chapter 5: *Programming Guide* for full details on the use of these signals.

Port C Line	Simple I/O: Mode 0	Strobed Input: Mode 1	Strobed Output: Mode 1	Bidirectional Bus: Mode 2
C7	I/O	I/O	/OBF _A	/OBF _A
C6	I/O	I/O	/ACK _A	/ACK _A
C5	I/O	IBF _A	I/O	IBF _A
C4	I/O	/STB _A	I/O	/STB _A
C3	I/O	INTR _A	INTR _A	INTR _A
C2	I/O	/STB _B	/ACK _B	I/O
C1	I/O	IBF _B	/OBF _B	I/O
C0	I/O	INTR _B	INTR _B	I/O

Table 2: Port C Line Usage.

The symbol 'l' indicates that a signal is active low.

When an 8255 is used in one of the handshaking modes, the /STB and IBF lines are used to synchronise input data transfers. The /OBF and /ACK lines are used to synchronise output transfers. The signals in the table above have the following functions:

Name	Type	Description
/STB	External Input	Strobe Input: A low on this handshaking line loads data from the peripheral bus into the input latch.
IBF	External Output	Input Buffer Full: A high on this line indicates that the external data has been loaded into the input latch. This is an input acknowledge signal.
/ACK	External Input	Acknowledge: The external device asserts this line low to indicate that the data written to the port by the program has been accepted.
/OBF	External Output	Output Buffer Full: The 8255 asserts this line low to indicate to the external device that the program has written data to the selected port. This line can be used to strobe the data into the external device.
INTR	External Output	Interrupt Request: This signal becomes active (high) when the 8255 requires service. For input operations, it indicates that there is data in the corresponding port to be read by the program. For output operations it indicates that the external device has accepted the data and thus the program can write another byte to the 8255.
/RD	Internal Input	Read Signal: This signal is generated by the control lines of the host computer. It is activated when the program executes an Input Instruction from any PC-36B register.
/WR	Internal Input	Write Signal: This signal is generated by the control lines of the host computer. It is activated when the program executes an Output Instruction to any PC-36B register.

Power supplies

The +12V, -12V, +5V and -5V power supplies are available, together with digital ground, user connector. These can be used to power external circuitry. As a rough guide, no more than about 250 mA should be drawn from these power supplies or the PC-36 board, the host computer or the power supply may be damaged permanently. Check the computer's power supply ratings for maximum current; this is especially important for the -12V and -5V supplies.

4

Register Structure

At the lowest level, the PC-36 is programmed using I/O port input and output instructions. This chapter contains information on all of the PC-36's registers. Although programming the board is not difficult, it is time consuming and requires detailed knowledge of both the PC-36 and the host PC's operating system. This manual provides the former. As an alternative, a set of software library functions is provided. These cover all of the board's features and should suit most applications. The Driver Library is described in a companion manual to this. In case routines need to be custom written for a specific purpose, it is often quicker to base them on the driver system, by loading and modifying routines from the driver library source code. This chapter and Chapter 5: *Programming Guide* provide full information on how this is done.

The PC-36 occupies 4 consecutive addresses in the computer's I/O space. The layout of these registers is shown in Table 3: *PC-36 Register Structure*. The offset of the registers are given as offset addresses from the base address of the board. The board base address is set with the DIP switch as detailed in Chapter 2: *Installation*.

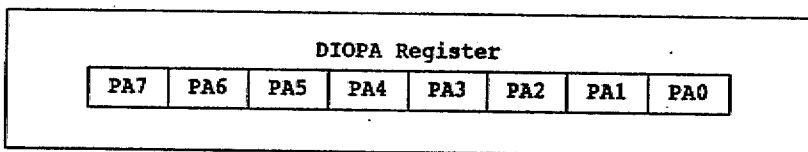
Offset	Write	Read
0	Port A (DIOPA)	Port A (DIOPA)
1	Port B (DIOPB)	Port B (DIOPB)
2	Port C (DIOPC)	Port C (DIOPC)
3	Control Register (DIOCTRL)	---

Table 3: *PC-36 Register Structure*.

The remainder of this chapter describes these registers in detail.

DIOPA - Port A of the 8255 (offset 0, read/write)

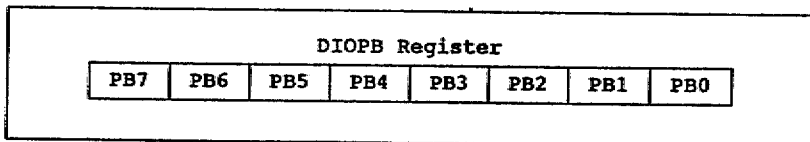
This register is port A of the 8255. It can be operated in one of three modes as described in Chapter 5 *Programming Guide*. The operating mode is set by writing to the DIOCTRL register, described below.



The bits PA7 (MSB) down to PA0 (LSB) reflect the status of the port's I/O lines. Depending on the programmed I/O mode of the port, the lines may be inputs, outputs or bidirectional.

DIOPB - Port B of the 8255 (offset 1, read/write)

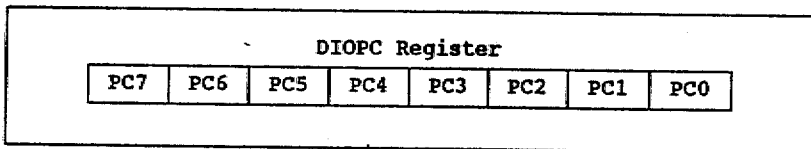
This register is port B of the 8255. It can be operated in one of three modes as described in Chapter 5 *Programming Guide*. The operating mode is set by writing to the DIOCTRL register, described below.



The bits PB7 (MSB) down to PB0 (LSB) reflect the status of the port's I/O lines. Depending on the programmed I/O mode of the port, the lines may be inputs, outputs or bidirectional.

DIOPC - Port C of the 8255 (offset 2, read/write)

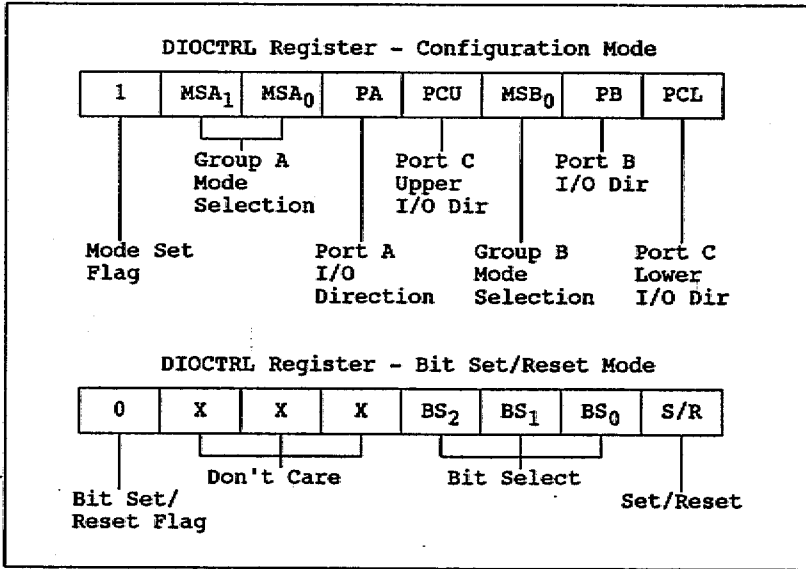
This register is port C of the 8255. It can be operated in one of three modes as described in Chapter 5 *Programming Guide*. The operating mode is set by writing to the DIOCTRL register, described below.



The bits PC7 (MSB) down to PC0 (LSB) reflect the status of the port's I/O lines. Depending on the programmed I/O mode of the port, the lines may be inputs, outputs or handshake lines.

DIOCTRL - Control register of the 8255 (offset 3, write only)

This register is used to control the operating modes of the 8255 or to set and reset individual bits in port C of the device. The layout of this register is shown below. Note that the function and bit names of the register depend on the setting of bit 7.



Bit 7: Function select: If this bit is set when the register is written to then the register is in configuration mode. If the bit is 0 then the register is in bit set/reset mode.

The functions of the remaining bits are described below, depending on the setting of bit 7.

Configuration Mode - Invoked when bit 7 is set

Bits 6-5: Group A mode select: These two bits set the mode of the group A ports. These are port A and the upper four lines of port C. The bit combinations are as follows:

MSA ₁	MSA ₀	Group A I/O Mode
0	0	Mode 0, simple I/O
0	1	Mode 1, strobed I/O
1	X	Mode 2, bidirectional bus

Bit 4: Port A I/O Mode: If this bit is set, then port A functions as an input. If it is 0, then port A is configured as an output.

Bit 3: Port C Upper I/O Mode: If this bit is set, then the upper four lines of port C function as inputs. If the bit is 0, then the lines become outputs.

Bit 2 : Group B mode select: This bit sets the mode of the group B ports. These are port B and the lower four lines of port C. The bit combinations are as follows:

MSB ₀	Group B I/O Mode
0	Mode 0, simple I/O
1	Mode 1, strobed I/O

Note that group B can only be used for simple or strobed I/O.

Bit 1 : Port B I/O Mode: If this bit is set, then port B functions as an input. If it is 0, then port B is configured as an output.

Bit 0 : Port C Lower I/O Mode: If this bit is set, then the lower four lines of port C function as inputs. If the bit is 0, then the lines become outputs.

Bit Set/Reset Mode - Invoked when bit 7 is clear

Bits 6-5 : These bits have no effect in this function.

Bits 3-1 : Bit Select: these bits select the bit in port C which is to be modified. A code of 000 selects port C line 0 to set or reset, 001 selects line 1 and so on up to 111 which selects line 7.

Bit 0 : Set/Reset: This bit specifies the state into which the selected port C line will be placed. Writing a 1 will make the line go high and a 0 makes it go low. This operation has no effect on the other lines of port C.

Programming Guide

This chapter describes programming the PC-36B board at the lowest level. While this is fairly straightforward, it requires detailed knowledge of the system hardware. As an alternative, the driver software supplied with the board can be used. Then the user need not read this section and can refer instead to the *Data Acquisition Driver Software Manual*, which describes the driver software which accompanies the PC-36B. Advantages of using the supplied driver are:

- Detailed knowledge is not required of the board, the host computer or the interface software.
- The Driver Library is callable from most high level languages
- The Driver Library takes into account multiple boards (both the PC-36 and other supported boards) in the same computer.

Users and developers who need to incorporate special routines into their application will need to read this chapter.

Once the PC-36 has been installed in the computer and the external connections made, the board is in an operational state. The PC-36 occupies four consecutive I/O addresses, starting at the board's base address as set by the base address DIP switch. Programming the PC-36 is done solely with port input and output instructions. Reading and writing to its addresses allows the board to be configured and data transferred to and from the board. Refer to Chapter 4 for the I/O register map of the PC-36.

Reading or writing to the ports typically takes the form of the one following instructions:

Language	Port Read	Port Write
'C	<code>data = inp(addr);</code>	<code>outp(addr, data);</code>
Pascal	<code>data := port[addr];</code>	<code>port[addr] := data;</code>
Assembly Language	<code>mov al, data</code> <code>mov dx, addr</code> <code>in al, dx</code>	<code>mov al, data</code> <code>mov dx, addr</code> <code>out dx, al</code>

Where: `addr` is the address is the address in the address map of the PC-36 and
`data` is the byte read or written.

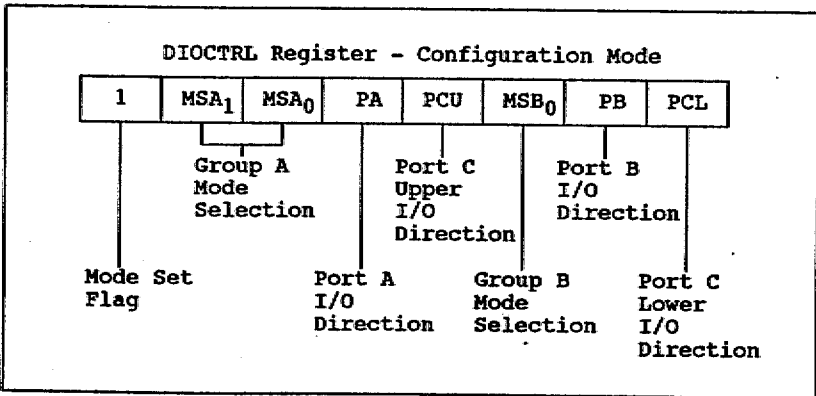
Programming the 8255 PIA

The PC-36 is based around the industry standard 8255 Peripheral Interface Adaptor (PIA) integrated circuit. This chapter provides detailed programming information on the 8255 for the PC-36. Further information on the 8255 can be found in the Intel Microprocessor and Peripheral Product Data Book.

Introduction

The 8255 is a general purpose peripheral interface having 24 programmable I/O lines. The 24 lines are divided into three 8-bit ports (named port A, port B and port C). The ports may be programmed either as two groups of 12 lines (group A and group B) or as the three individual 8-bit ports. The ports/groups may be operated in three modes: simple I/O, strobed I/O and bidirectional I/O. The 8255 also has a single bit set/reset feature for port C.

Before any I/O can be done, the mode and direction of the ports/groups of the 8255 must be set. This is done simply by writing one byte of configuration information to the control register of the 8255. The 8255 then operates in the specified mode until it is reset or new configuration information is written to the control register. The format of this register is repeated below for reference.



Bit 7 of the DIOCTRL register must be set when programming the configuration of the 8255.

The mode is set for each of the two groups of the 8255 and the direction is set for the individual ports. Note that the direction of port C is independently programmable in two 4-line nibbles.

Mode 0: Simple I/O

This mode is used for simple input and output operations for each of the ports. No handshaking is used. Data is simply read from or written to a selected port.

The following characterise Mode 0:

- Two 8-bit ports (ports A and B) and two 4-bit ports (upper and lower nibble of port C).
- Any port can be configured for input or output.
- Outputs are latched, inputs are not latched.
- Data transfer by polled I/O.

Mode 0 Programming

To use the 8255 in mode 0:

- Write to the control register a byte to configure the 8255 to be in mode 0 and the three ports for the desired data direction.
- Then read or write from the I/O port corresponding to an 8255 port (port A, B or C) as many times as necessary to obtain or transfer the required amount of data.

Mode 0 Programming Examples

```
#define BaseAddr    0x310    /* PC-36 base address at 310 hex */
#define DIOPA      0        /* Offset of port A of the 8255 */
#define DIOPB      1        /* Offset of port B */
#define DIOPC      2        /* Offset of port C */
#define DIOCTRL    3        /* Offset of the control register */

void main( void )
{
    unsigned int porta, portb, portc, portctrl, data, outval = 0x1B;

    /* Calculate register addresses */
    porta = BaseAddr + DIOPA;
    portb = BaseAddr + DIOPB;
    portc = BaseAddr + DIOPC;
    portctrl = BaseAddr + DIOCTRL;

    /* 0x90 = 1001 0000, port A to input, ports B and C for output */
    outp( portctrl, 0x90 );

    /* Read data from port A and write data to port B and C */
    data = inp( porta );
    outp( portb, 0x3F );
    outp( portc, outval );
}
```

Mode 1: Strobed I/O

In this mode data transfers are controlled by handshaking signals. Some of the port C lines are used for these control signals. Hence they take on different functions and names.

The following characterise Mode 1:

- Two groups, group A and B. Each group consists of an 8-bit data port and three control lines.
- Certain port C lines take on special functions.
- The data ports can be either input or output ports.
- Both inputs and outputs are latched.
- One 2-bit simple I/O port.
- Data transfer by polled I/O.

With both groups configured in mode 1, a single 8255 can read or write data 16-bits wide.

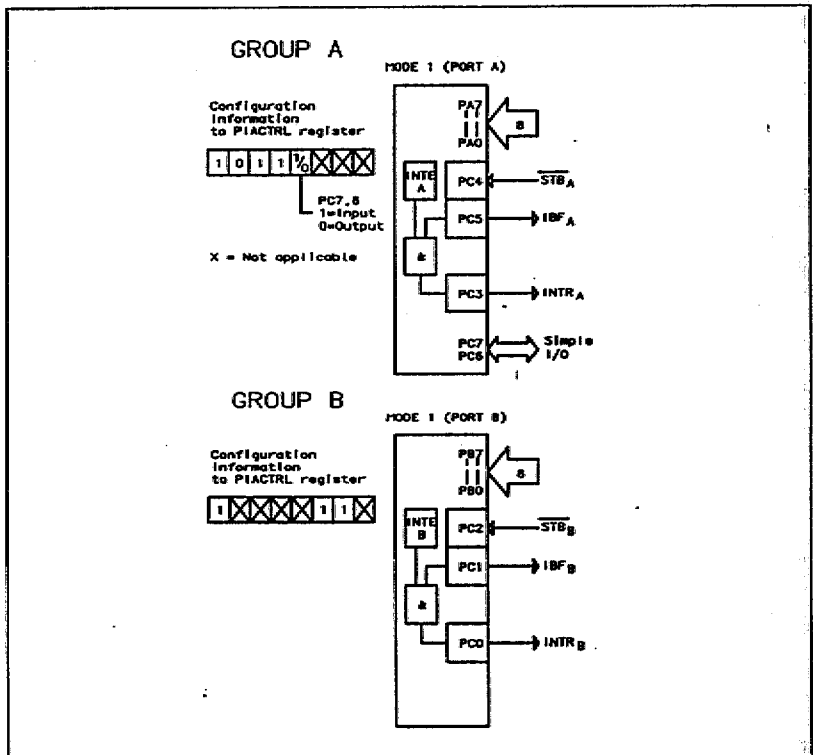


Figure 4: Mode 1 Input of an 8255.

Mode 1 Programming

To use the 8255 in mode 1 input with handshaking:

- Write to the control register a byte to configure the 8255 for mode 1 and the appropriate group for data input.
- The program continually monitors the IBF line (see below) by reading port C.
- The external device pulls the /STB input line on the digital I/O connector low and this loads data into the input port.
- The IBF output line goes high on the digital I/O connector to indicate that the data has been loaded into the input latch.
- This also causes the corresponding IBF bit in port C to be set and the program can thus read the data.
- The external device can now pull the /STB low again to make the program read another byte of data and hence repeat the cycle.

The program could also enable the INTR line with the INTE flip-flop and then monitor INTR instead of the IBF line. Note that the interrupt signals from the 8255 are not connected to the host computer from the PC-36.

Anytime a group of the 8255 is in mode 1 input, the status of the handshaking lines and interrupt signals can be obtained by reading port C. The byte read contains the following information:

Port C Mode 1 Input Status Information							
C7	C6	IBF _A	INTE _A	INTR _A	INTE _B	IBF _B	INTR _B

Where C7 and C6 correspond to the status of the lines of the two-bit port, port C.

See Appendix B for Mode 1 timing specifications.

To use the 8255 in mode 1 output with handshaking:

- Write to the control register a byte to configure the 8255 for mode 1 and the appropriate group for data output.
- The program continually monitors the Output Buffer Full (/OBF) line by reading port C, waiting for it to go high. A high indicates that the last data written to the port has been read by the external device.
- Then the program can write new data to the port.
- The /OBF line to the I/O connector goes low to indicate to the peripheral device that there is data to be from the 8255.
- The external device pulls the Acknowledge (/ACK) input low after reading the data.
- This makes the /OBF line go high again and the cycle may be repeated until all the required data has been written.

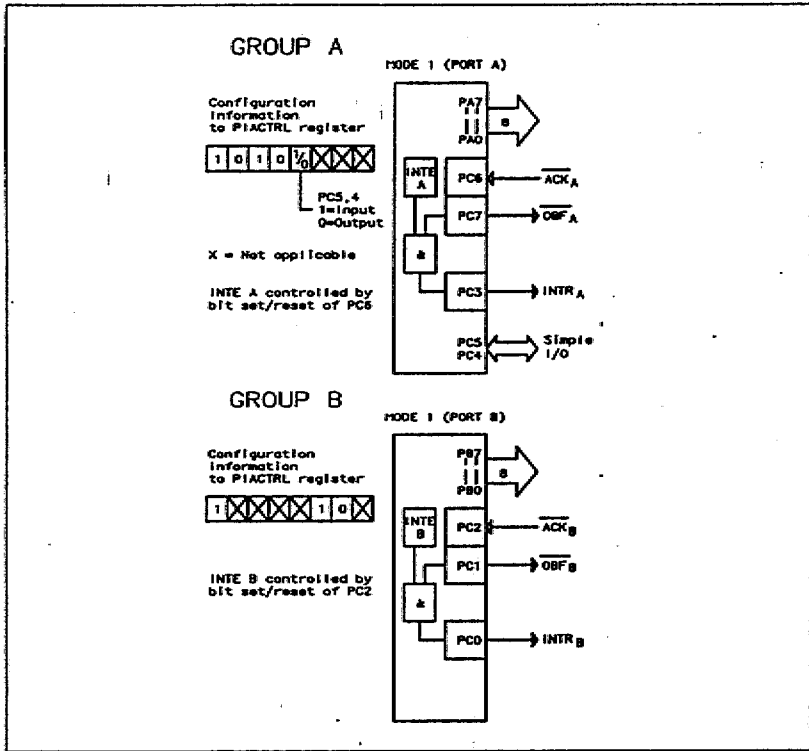
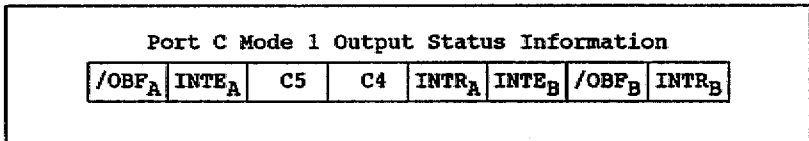


Figure 5: Mode 1 Output of an 8255.

The program could also enable the INTR line with the Interrupt Enable (INTE) flip-flop and then monitor INTR instead of the /OBF line. Note that the interrupt signals from the 8255 are not connected to the host computer from the PC-36.

Anytime a group of the 8255 is in mode 1 output, the status of the handshaking lines and interrupt signals can be obtained by reading port C. The byte read contains the following information:



Where C5 and C4 correspond to the status of the two-bit port, port C.

See Appendix B for Mode 1 timing specifications.

Mode 1 Programming Examples

```

#define BaseAddr      0x310      /* PC-36 base address at 310 hex */
#define DIOPA         0          /* Offset of port A of the first 8255 */
#define DIOPB         1          /* Offset of port B */
#define DIOPC         2          /* Offset of port C */
#define DIOCTRL       3          /* Offset of the control register */

void main( void )
{
  unsigned int porta, portb, portc, portctrl, data, outval = 0x1B;

  /* Calculate register addresses */
  porta = BaseAddr + DIOPA;
  portb = BaseAddr + DIOPB;
  portc = BaseAddr + DIOPC;
  portctrl = BaseAddr + DIOCTRL;

  /* 0xB0 = 1011 0000, port A to input in mode 1,
  outp( portctrl, 0xB0 ); /* ports B and C for output in mode 0 */

  while( !( inp(portc) & 0x20 ) ); /* Wait for IBFA to become set */

  data = inp( porta ); /* Read the data from port A */

  /* 0xA0 = 1010 0000, port A to output in mode 1,
  outp( portctrl, 0xA0 ); /* ports B and C for output in mode 0 */

  while( !( inp(portc) & 0x80 ) ); /* Wait for /OBFA to become set */

  outp( porta, outval ); /* Write the data to port A */
}

```

Mode 2: Strobed Bidirectional Bus I/O

This mode provides a means for communicating with an external device using an 8-bit bus for both transmitting and receiving data. Both input and output handshaking signals similar to mode 1 are provided to maintain proper bus flow discipline.

The following characterise Mode 2:

- Only group A operates in mode 2.
- One 8-bit bidirectional port, functions as both input and output.
- Five of the port C lines take on special functions.
- Both inputs and outputs are latched.
- One 3-bit simple I/O port.
- Data transfer by polled I/O.

With group A of the 8255 on the PC-36 configured in mode 2, the board provides the function of an 8-bit wide bidirectional data bus.

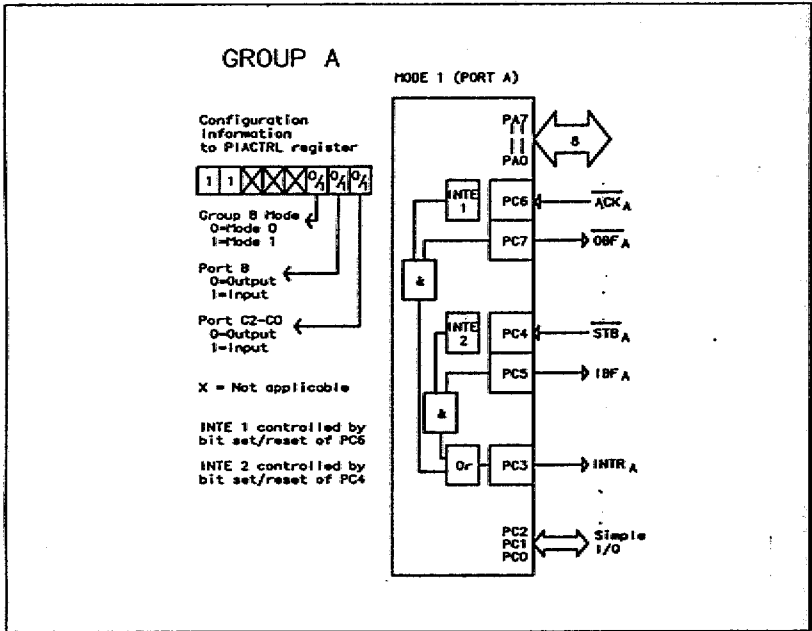


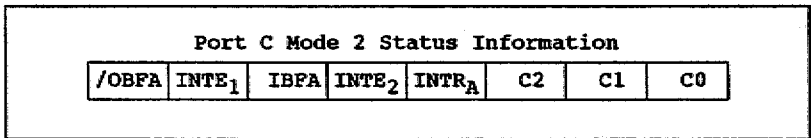
Figure 6: Mode 2 of an 8255.

Mode 2 Programming

To use the 8255 in mode 2 with bidirectional handshaking:

- Write to the control register a byte to configure the 8255 for mode 2.
- The program continually monitors both the IBFA and /OBFA lines by reading port C.
- If the port C bit corresponding to IBFA is set, this indicates that the external device has written data into the input latch. The program must therefore read the data from the port A.
- If the port C bit corresponding to /OBFA is set, this indicates that the external device has read the data written by the program to port A. It must therefore write more data to port A.
- This process can be repeated until the required amount of data has been read and written.

Anytime the 8255 is in mode 2, the status of the handshaking lines and interrupt signals can be obtained by reading port C. The byte read contains the following information:



Where C2, C1 and C0 correspond to the status of the lines of the three-bit port, port C.

See Appendix B for Mode 2 timing specifications.

Mode 2 Programming Examples

```

#define BaseAddr    0x310    /* PC-36 base address at 310 hex */
#define DIOPA       0        /* Offset of port A of the first 8255 */
#define DIOPB       1        /* Offset of port B */
#define DIOPC       2        /* Offset of port C */
#define DIOCTRL     3        /* Offset of the control register */

void main( void )
{
  unsigned int porta, portb, portc, portctrl;
  unsigned int sts, data, outval = 0x1B;

  /* Calculate register addresses */
  porta = BaseAddr + DIOPA;
  portb = BaseAddr + DIOPB;
  portc = BaseAddr + DIOPC;
  portctrl = BaseAddr + DIOCTRL;

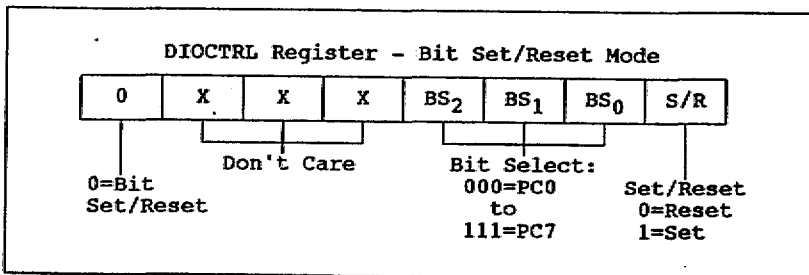
  /* 0xC0 = 1100 0000, port A to input in mode 2,
  ports B and C for output in mode 0 */
  outp( portctrl, 0xC0 );

  while( !( sts = (inp(portc) & 0xA0) ) ); /* Wait for IBFA or */
                                          /* /OBF to become set */
  if( sts & 0x80 ) /* /OBF was set */
    outp( porta, outval ); /* Write some data to port A */
  else /* IBF was set */
    data = inp( porta ); /* Read the data from port A */
}

```

Single Bit Set/Reset

Any of the eight bits of port C can be set or reset using a single output instruction to the DIOCTRL register. When port C is being used as status/control for port A or B, any of these bits can be set or reset just as if they were data output ports. The format of the byte to write to the DIOCTRL register to set or reset a port C bit is repeated below.



Mixed Mode Programming

An 8255 is not constrained to operate in one mode only. For example, Port A may operate in mode 2 and port B may then operate in either mode 1 or mode 0. For any combination, some or all of the port C lines are used for control or status. The remaining port C lines may be used in mode 0 either as inputs or outputs.

A read operation of port C returns all the port C lines except the /ACK and /STB lines. In their place will appear the status of the Interrupt Enable flip-flops (INTE_x). This is illustrated in Figures 4 to 6 above and the status information bytes which follow the figures.

A write operation to port C will only affect lines programmed as mode 0 outputs. To write to any port C output programmed as a mode 1 output or to change an interrupt enable flip-flop, the Bit Set/Reset operation must be used.

Bit Set/Reset

Using the Bit Set/Reset command, any port C line programmed as an output (including INTR, IBF and /OBF) can be written or an interrupt enable flag set or reset. Lines programmed as inputs (including /ACK and /STB) are not affected by this command. Writing to these lines will affect the interrupt enable flags.

Driver Software

Full driver software is supplied as part of the PC-36B package. It is called the Data Acquisition Driver Software Library, and is provided in two equivalent forms:

- A ready to use, precompiled, driver software library, with routines callable from most high level languages.
- Complete 'C' source code for all driver routines.

The Driver Library allows programmers to control the PC-36 board via high level function calls, so allowing the user to write custom software applications without having to understand the low level operation of the board.

Also included with the driver package is complete source code, in C for the entire driver package. This allows advanced users to modify existing code, rather than having to start writing low level code from scratch.

The Data Acquisition Driver Library supports not only the PC-36B board, but a number of other boards too. This chapter presents a quick reference to the functions in the Driver Library that apply to the PC-36B board. Full details on using the library functions, the source code and a full function reference are provided in the companion manual to this, *The Data Acquisition Driver Software Manual*.

A Note about Using the Driver Library

If you are using the Driver Library to operate the board, unless you know exactly what you are doing, **always** control the board with calls to the Driver Library and do not bypass the Driver Library and read or write directly to or from the board. This is because the Driver Library keeps an internal software copy of the state of the board. If you communicate to the board directly, this will obviously not update the software copy of the board's state. Hence, subsequent calls to the Driver Library may not produce the desired results, or the board may behave erratically or unpredictably.

In summary, do not allow the board's state to get out of sync with the software copy of its state.

Quick Function Reference

The Data Acquisition Driver, when used with the PC-36 board has eight appropriate function calls. These are the following:

Function Name	Brief Description
<code>Init_brd</code>	Initialises one of up to eight boards. This function initialises the hardware of the board if necessary and informs the driver system of the board's presence. It must be called before any other function calls are made to the board.
<code>DIO_cfg_line</code>	Configures lines or groups of lines in a digital I/O port. Allows the smallest unit in a port to be configured.
<code>DIO_prt_cfg</code>	Configures the operating mode of a port. This function is a subset of the <code>DIO_cfg_line</code> function.
<code>DIO_in_port</code>	Returns digital data from the specified port.
<code>DIO_out_port</code>	Writes digital data to the specified port.
<code>DIO_in_line</code>	Returns the state of a single line of the specified port.
<code>DIO_out_line</code>	Sets the state of a single line of the specified port.
<code>DIO_prt_status</code>	Returns a status byte indicating the status of an individual I/O port.

Hardware Specifications

External interface

Number of I/O lines:	24 in three 8-bit digital ports
Input voltage:	Logic 0: -0.5 - 0.8V Logic 1: 2V - 5V
Output voltage:	Logic 0: 0.45V max Logic 1: 2.4V min
Output current:	Low state: 1.7mA max High state -200uA min
Maximum Darlington drive current:	-4.0mA; from ports B and C only
Maximum power:	1W total maximum power from all three ports
Power supply current at I/O connector:	250mA from +5V typ, others vary up to 250mA depending on host computer power supply rating
Other lines:	All computer power supplies available on I/O connector
I/O connector:	37 way male DB37 Amphenol or equivalent

Host computer interface

Bus type:	XT, AT, ISA, EISA
I/O address selection:	From 0h to 7F8h on 8 byte boundaries, DIP switch selectable.
I/O wait states (PC-36B):	0, 1, 2, 4 or 8 jumper selectable. Only affects cycles directed at the card.
Number of registers:	Four 8-bit
Word size:	8-bits
Word transfer rate:	10 MHz max ¹
Power requirements:	+5V Max 250 mA +12V 0.0 mA -12V 0.0 mA -5V 0.0 mA

¹ This figure is the maximum transfer rate of the PC-36 hardware. In practise, the limiting factors are the host computer and software speed. On an 8MHz AT, an assembly program continuously writing a constant to an output port achieves a transfer rate of around 500kHz.

Environmental

Absolute maximum input voltage:	7V
Absolute minimum input voltage:	-0.5V
Operating temperature:	0°C to 70°C.
Storage temperature:	-55°C to 150°C.
Relative humidity:	5% to 90% non-condensing
Board size	PC-36 10.7 x 10.8 cm
	PC-36B 10.3 x 9.5 cm

Appendix A

Base Address Switch Settings

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
0h	ON	ON	ON	ON	ON	ON	ON	ON	0h
8h	ON	ON	ON	ON	ON	ON	ON	OFF	8h
10h	ON	ON	ON	ON	ON	ON	OFF	ON	10h
18h	ON	ON	ON	ON	ON	ON	OFF	OFF	18h
20h	ON	ON	ON	ON	ON	OFF	ON	ON	20h
28h	ON	ON	ON	ON	ON	OFF	ON	OFF	28h
30h	ON	ON	ON	ON	ON	OFF	OFF	ON	30h
38h	ON	ON	ON	ON	ON	OFF	OFF	OFF	38h
40h	ON	ON	ON	ON	OFF	ON	ON	ON	40h
48h	ON	ON	ON	ON	OFF	ON	ON	OFF	48h
50h	ON	ON	ON	ON	OFF	ON	OFF	ON	50h
58h	ON	ON	ON	ON	OFF	ON	OFF	OFF	58h
60h	ON	ON	ON	ON	OFF	OFF	ON	ON	60h
68h	ON	ON	ON	ON	OFF	OFF	ON	OFF	68h
70h	ON	ON	ON	ON	OFF	OFF	OFF	ON	70h
78h	ON	ON	ON	ON	OFF	OFF	OFF	OFF	78h
80h	ON	ON	ON	OFF	ON	ON	ON	OFF	80h
88h	ON	ON	ON	OFF	ON	ON	OFF	ON	88h
90h	ON	ON	ON	OFF	ON	ON	OFF	ON	90h
98h	ON	ON	ON	OFF	ON	ON	OFF	OFF	98h
A0h	ON	ON	ON	OFF	ON	OFF	ON	ON	A0h
A8h	ON	ON	ON	OFF	ON	OFF	ON	OFF	A8h
B0h	ON	ON	ON	OFF	ON	OFF	OFF	ON	B0h
B8h	ON	ON	ON	OFF	ON	OFF	OFF	OFF	B8h
C0h	ON	ON	ON	OFF	OFF	ON	ON	ON	C0h
C8h	ON	ON	ON	OFF	OFF	ON	ON	OFF	C8h
D0h	ON	ON	ON	OFF	OFF	ON	OFF	ON	D0h
D8h	ON	ON	ON	OFF	OFF	ON	OFF	OFF	D8h
E0h	ON	ON	ON	OFF	OFF	OFF	ON	ON	E0h
E8h	ON	ON	ON	OFF	OFF	OFF	ON	OFF	E8h
F0h	ON	ON	ON	OFF	OFF	OFF	OFF	ON	F0h
F8h	ON	ON	ON	OFF	OFF	OFF	OFF	ON	F8h
100h	ON	ON	OFF	ON	ON	ON	ON	ON	100h
108h	ON	ON	OFF	ON	ON	ON	ON	OFF	108h
110h	ON	ON	OFF	ON	ON	ON	OFF	ON	110h
118h	ON	ON	OFF	ON	ON	ON	OFF	OFF	118h
120h	ON	ON	OFF	ON	ON	OFF	ON	ON	120h
128h	ON	ON	OFF	ON	ON	OFF	ON	OFF	128h
130h	ON	ON	OFF	ON	ON	OFF	OFF	ON	130h
138h	ON	ON	OFF	ON	ON	OFF	OFF	OFF	138h
140h	ON	ON	OFF	ON	OFF	ON	ON	ON	140h
148h	ON	ON	OFF	ON	OFF	ON	ON	OFF	148h
150h	ON	ON	OFF	ON	OFF	ON	OFF	ON	150h
158h	ON	ON	OFF	ON	OFF	ON	OFF	OFF	158h
160h	ON	ON	OFF	ON	OFF	OFF	ON	ON	160h
168h	ON	ON	OFF	ON	OFF	OFF	ON	OFF	168h
170h	ON	ON	OFF	ON	OFF	OFF	OFF	ON	170h
178h	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	178h
180h	ON	ON	OFF	OFF	ON	ON	ON	ON	180h
188h	ON	ON	OFF	OFF	ON	ON	ON	OFF	188h
190h	ON	ON	OFF	OFF	ON	ON	OFF	ON	190h
198h	ON	ON	OFF	OFF	ON	ON	OFF	OFF	198h
1A0h	ON	ON	OFF	OFF	ON	OFF	ON	ON	1A0h
1A8h	ON	ON	OFF	OFF	ON	OFF	ON	OFF	1A8h
1B0h	ON	ON	OFF	OFF	ON	OFF	OFF	ON	1B0h
1B8h	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	1B8h
1C0h	ON	ON	OFF	OFF	OFF	ON	ON	ON	1C0h
1C8h	ON	ON	OFF	OFF	OFF	ON	ON	OFF	1C8h
1D0h	ON	ON	OFF	OFF	OFF	ON	OFF	ON	1D0h
1D8h	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	1D8h
1E0h	ON	ON	OFF	OFF	OFF	OFF	ON	ON	1E0h
1E8h	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	1E8h
1F0h	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	1F0h
1F8h	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	1F8h

Table 4: Base Address Switch Settings.

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
200h	ON	OFF	ON	ON	ON	ON	ON	ON	200h
208h	ON	OFF	ON	ON	ON	ON	ON	OFF	208h
210h	ON	OFF	ON	ON	ON	ON	OFF	ON	210h
218h	ON	OFF	ON	ON	ON	ON	OFF	OFF	218h
220h	ON	OFF	ON	ON	ON	OFF	ON	ON	220h
228h	ON	OFF	ON	ON	ON	OFF	ON	OFF	228h
230h	ON	OFF	ON	ON	ON	OFF	OFF	ON	230h
238h	ON	OFF	ON	ON	ON	OFF	OFF	OFF	238h
240h	ON	OFF	ON	ON	OFF	ON	ON	ON	240h
248h	ON	OFF	ON	ON	OFF	ON	ON	OFF	248h
250h	ON	OFF	ON	ON	OFF	ON	OFF	ON	250h
258h	ON	OFF	ON	ON	OFF	ON	OFF	OFF	258h
260h	ON	OFF	ON	ON	OFF	OFF	ON	ON	260h
268h	ON	OFF	ON	ON	OFF	OFF	ON	OFF	268h
270h	ON	OFF	ON	ON	OFF	OFF	OFF	ON	270h
278h	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	278h
280h	ON	OFF	ON	OFF	ON	ON	ON	ON	280h
288h	ON	OFF	ON	OFF	ON	ON	ON	OFF	288h
290h	ON	OFF	ON	OFF	ON	ON	OFF	ON	290h
298h	ON	OFF	ON	OFF	ON	ON	OFF	OFF	298h
2A0h	ON	OFF	ON	OFF	ON	OFF	ON	ON	2A0h
2A8h	ON	OFF	ON	OFF	ON	OFF	ON	OFF	2A8h
2B0h	ON	OFF	ON	OFF	ON	OFF	OFF	ON	2B0h
2B8h	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	2B8h
2C0h	ON	OFF	ON	OFF	OFF	ON	ON	ON	2C0h
2C8h	ON	OFF	ON	OFF	OFF	ON	ON	OFF	2C8h
2D0h	ON	OFF	ON	OFF	OFF	ON	ON	OFF	2D0h
2D8h	ON	OFF	ON	OFF	OFF	ON	OFF	ON	2D8h
2E0h	ON	OFF	ON	OFF	OFF	ON	ON	ON	2E0h
2E8h	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	2E8h
2F0h	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	2F0h
2F8h	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	2F8h
300h	ON	OFF	OFF	ON	ON	ON	ON	ON	300h
308h	ON	OFF	OFF	ON	ON	ON	ON	OFF	308h
310h	ON	OFF	OFF	ON	ON	ON	OFF	ON	310h
318h	ON	OFF	OFF	ON	ON	ON	OFF	OFF	318h
320h	ON	OFF	OFF	ON	ON	OFF	ON	ON	320h
328h	ON	OFF	OFF	ON	ON	OFF	ON	OFF	328h
330h	ON	OFF	OFF	ON	ON	OFF	OFF	ON	330h
338h	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	338h
340h	ON	OFF	OFF	ON	OFF	ON	ON	ON	340h
348h	ON	OFF	OFF	ON	OFF	ON	ON	OFF	348h
350h	ON	OFF	OFF	ON	OFF	ON	OFF	ON	350h
358h	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	358h
360h	ON	OFF	OFF	ON	OFF	ON	ON	ON	360h
368h	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	368h
370h	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	370h
378h	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	378h
380h	ON	OFF	OFF	OFF	ON	ON	ON	ON	380h
388h	ON	OFF	OFF	OFF	ON	ON	ON	OFF	388h
390h	ON	OFF	OFF	OFF	ON	ON	OFF	ON	390h
398h	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	398h
3A0h	ON	OFF	OFF	OFF	ON	OFF	ON	ON	3A0h
3A8h	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	3A8h
3B0h	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	3B0h
3B8h	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	3B8h
3C0h	ON	OFF	OFF	OFF	OFF	ON	ON	ON	3C0h
3C8h	ON	OFF	OFF	OFF	OFF	ON	ON	ON	3C8h
3D0h	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	3D0h
3E0h	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	3E0h
3E8h	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	3E8h
3F0h	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	3F0h
3F8h	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3F8h

Table 4: Base Address Switch Settings (continued).

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
400h	OFF	ON	ON	ON	ON	ON	ON	ON	400h
408h	OFF	ON	ON	ON	ON	ON	ON	OFF	408h
410h	OFF	ON	ON	ON	ON	ON	OFF	ON	410h
418h	OFF	ON	ON	ON	ON	ON	OFF	OFF	418h
420h	OFF	ON	ON	ON	ON	ON	OFF	ON	420h
428h	OFF	ON	ON	ON	ON	ON	OFF	ON	428h
430h	OFF	ON	ON	ON	ON	ON	OFF	OFF	430h
438h	OFF	ON	ON	ON	ON	ON	OFF	OFF	438h
440h	OFF	ON	ON	ON	ON	OFF	ON	ON	440h
448h	OFF	ON	ON	ON	ON	OFF	ON	ON	448h
450h	OFF	ON	ON	ON	ON	OFF	ON	OFF	450h
458h	OFF	ON	ON	ON	ON	OFF	ON	OFF	458h
460h	OFF	ON	ON	ON	ON	OFF	OFF	ON	460h
468h	OFF	ON	ON	ON	ON	OFF	OFF	ON	468h
470h	OFF	ON	ON	ON	ON	OFF	OFF	OFF	470h
478h	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	478h
480h	OFF	ON	ON	OFF	ON	ON	ON	ON	480h
488h	OFF	ON	ON	OFF	ON	ON	ON	OFF	488h
490h	OFF	ON	ON	OFF	ON	ON	OFF	ON	490h
498h	OFF	ON	ON	OFF	ON	ON	OFF	OFF	498h
4A0h	OFF	ON	ON	OFF	ON	OFF	ON	ON	4A0h
4A8h	OFF	ON	ON	OFF	ON	OFF	ON	OFF	4A8h
4B0h	OFF	ON	ON	OFF	ON	OFF	OFF	ON	4B0h
4B8h	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	4B8h
4C0h	OFF	ON	ON	OFF	OFF	ON	ON	ON	4C0h
4C8h	OFF	ON	ON	OFF	OFF	ON	ON	OFF	4C8h
4D0h	OFF	ON	ON	OFF	OFF	ON	OFF	ON	4D0h
4D8h	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	4D8h
4E0h	OFF	ON	ON	OFF	OFF	OFF	ON	ON	4E0h
4E8h	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	4E8h
4F0h	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	4F0h
4F8h	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	4F8h
500h	OFF	ON	OFF	ON	ON	ON	ON	ON	500h
508h	OFF	ON	OFF	ON	ON	ON	ON	OFF	508h
510h	OFF	ON	OFF	ON	ON	ON	OFF	ON	510h
518h	OFF	ON	OFF	ON	ON	ON	OFF	OFF	518h
520h	OFF	ON	OFF	ON	ON	OFF	ON	ON	520h
528h	OFF	ON	OFF	ON	ON	OFF	ON	OFF	528h
530h	OFF	ON	OFF	ON	ON	OFF	OFF	ON	530h
538h	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	538h
540h	OFF	ON	OFF	ON	OFF	ON	ON	ON	540h
548h	OFF	ON	OFF	ON	OFF	ON	ON	OFF	548h
550h	OFF	ON	OFF	ON	OFF	ON	OFF	ON	550h
558h	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	558h
560h	OFF	ON	OFF	ON	OFF	OFF	ON	ON	560h
568h	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	568h
570h	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	570h
578h	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	578h
580h	OFF	ON	OFF	OFF	ON	ON	ON	ON	580h
588h	OFF	ON	OFF	OFF	ON	ON	ON	OFF	588h
590h	OFF	ON	OFF	OFF	ON	ON	OFF	ON	590h
598h	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	598h
5A0h	OFF	ON	OFF	OFF	ON	OFF	ON	ON	5A0h
5A8h	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	5A8h
5B0h	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	5B0h
5B8h	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	5B8h
5C0h	OFF	ON	OFF	OFF	OFF	ON	ON	ON	5C0h
5C8h	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	5C8h
5D0h	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	5D0h
5D8h	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	5D8h
5E0h	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	5E0h
5E8h	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	5E8h
5F0h	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	5F0h
5F8h	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	5F8h

Table 4: Base Address Switch Settings (continued).

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
600h	OFF	OFF	ON	ON	ON	ON	ON	ON	600h
608h	OFF	OFF	ON	ON	ON	ON	ON	OFF	608h
610h	OFF	OFF	ON	ON	ON	ON	OFF	ON	610h
618h	OFF	OFF	ON	ON	ON	ON	OFF	OFF	618h
620h	OFF	OFF	ON	ON	ON	OFF	ON	ON	620h
628h	OFF	OFF	ON	ON	ON	OFF	ON	OFF	628h
630h	OFF	OFF	ON	ON	ON	OFF	OFF	ON	630h
638h	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	638h
640h	OFF	OFF	ON	ON	OFF	ON	ON	ON	640h
648h	OFF	OFF	ON	ON	OFF	ON	ON	OFF	648h
650h	OFF	OFF	ON	ON	OFF	ON	OFF	ON	650h
658h	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	658h
660h	OFF	OFF	ON	ON	OFF	ON	ON	ON	660h
668h	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	668h
670h	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	670h
678h	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	678h
680h	OFF	OFF	ON	OFF	ON	ON	ON	ON	680h
688h	OFF	OFF	ON	OFF	ON	ON	ON	OFF	688h
690h	OFF	OFF	ON	OFF	ON	ON	OFF	ON	690h
698h	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	698h
6A0h	OFF	OFF	ON	OFF	ON	ON	OFF	ON	6A0h
6A8h	OFF	OFF	ON	OFF	ON	OFF	ON	ON	6A8h
6B0h	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	6B0h
6B8h	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	6B8h
6C0h	OFF	OFF	ON	OFF	OFF	ON	ON	ON	6C0h
6C8h	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	6C8h
6D0h	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	6D0h
6D8h	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	6D8h
6E0h	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	6E0h
6E8h	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	6E8h
6F0h	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	6F0h
6F8h	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	6F8h
700h	OFF	OFF	OFF	ON	ON	ON	ON	ON	700h
708h	OFF	OFF	OFF	ON	ON	ON	ON	OFF	708h
710h	OFF	OFF	OFF	ON	ON	ON	OFF	ON	710h
718h	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	718h
720h	OFF	OFF	OFF	ON	ON	OFF	ON	ON	720h
728h	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	728h
730h	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	730h
738h	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	738h
740h	OFF	OFF	OFF	ON	OFF	ON	ON	ON	740h
748h	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	748h
750h	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	750h
758h	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	758h
760h	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	760h
768h	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	768h
770h	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	770h
778h	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	778h
780h	OFF	OFF	OFF	OFF	ON	ON	ON	ON	780h
788h	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	788h
790h	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	790h
798h	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	798h
7A0h	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	7A0h
7A8h	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	7A8h
7B0h	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	7B0h
7B8h	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	7B8h
7C0h	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	7C0h
7C8h	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	7C8h
7D0h	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	7D0h
7D8h	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	7D8h
7E0h	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	7E0h
7E8h	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	7E8h
7F0h	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	7F0h
7F8h	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	7F8h

Table 4: Base Address Switch Settings (continued).

Appendix B

Timing Specifications for 8255 Modes 1 and 2

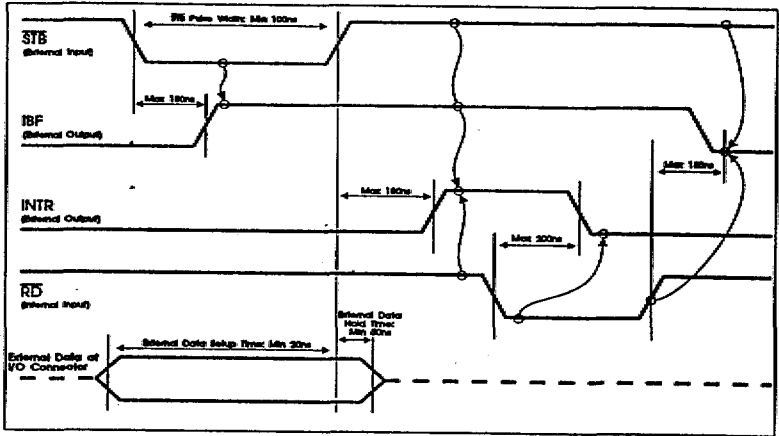


Figure 7: Strobed Input (Mode 1).

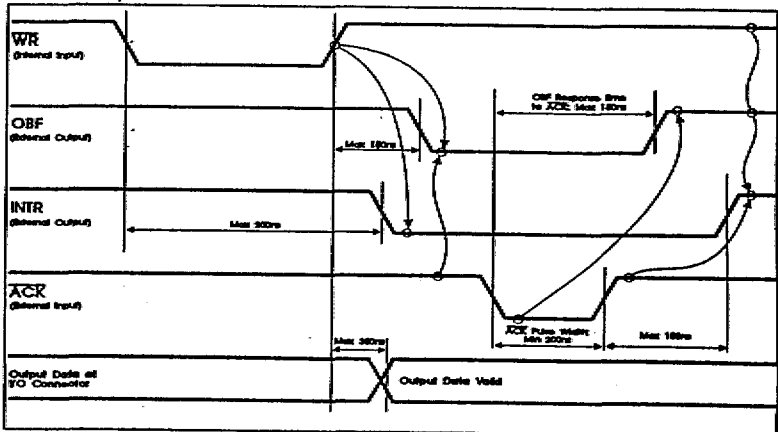


Figure 8: Strobed Output (Mode 1).

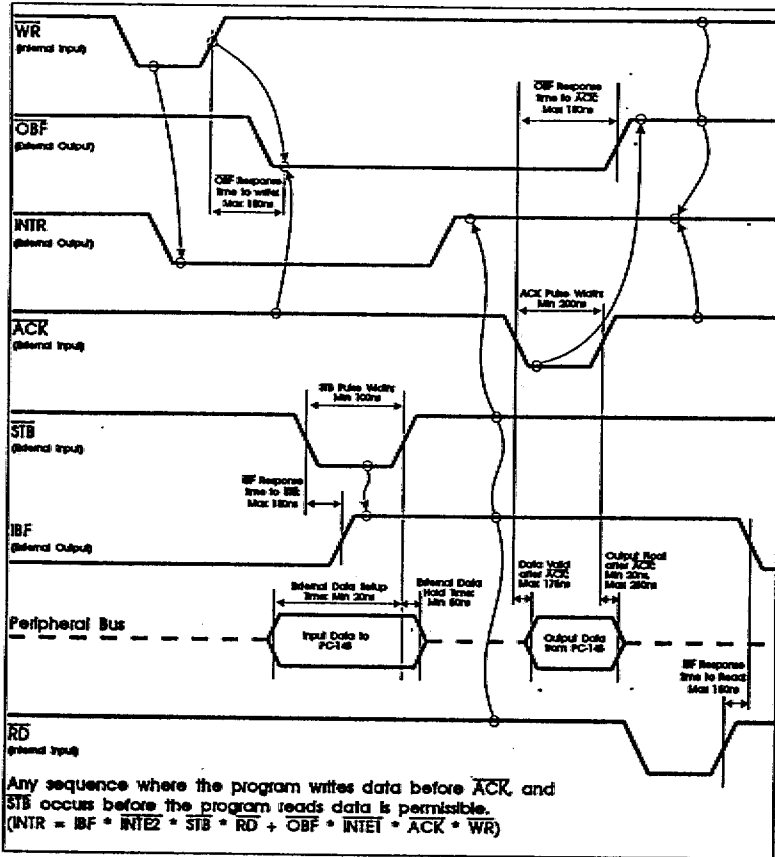


Figure 9: Bidirectional Bus (Mode 2).

Appendix C

User Serviceable Parts

The 8255 is mounted in a socket. If any external shorts or transients damage the PC-36 then replacing the 8255 PIA chip may well correct the problem. The device may be replaced with any 8255 equivalent, but to ensure the high speed specifications of the PC-36B it is recommended that the replacement is a NEC71055-10 or better.

Nothing more than a screwdriver is required to remove the device from its socket. When refitting the replacement device, make sure it is inserted the correct way around, with the notch in the device lined up with the notch in the socket and the indicator on the board legend.