

PC 192A

**Enhanced 192 Channel Digital I/O
Card**

User's Manual

**For the IBM PC, PC/XT, PC/AT, PS/2
386, 486, ISA and EISA computers**

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Introduction

The PC 192A is an enhanced parallel digital I/O interface board for the IBM PC/XT/AT, 486, Pentium, ISA and EISA Computers. It provides 192 Digital I/O lines built around the industry standard 8255 type Programmable Peripheral Interface (PPI) adapter Ics.

The PC 192A fits into one of the IBM PC/AT 8 bit expansion slot.

Typical applications

- * Industrial control
- * Process Control
- * Laboratory Automation
- * Energy management
- * Product testing

Key Features

- * On-board wait state generation allows operation on high speed computers
- * Provides 192 digital I/O channels configured in blocks of three 8 bits
- * All 8255 PPI modes are supported for example:
 - a) Simple inputs and outputs
 - b) Strobed inputs and outputs with handshaking
 - c) Bidirectional input/output with handshaking
- * Interrupt level for each PPI selectable from IRQ2 thru IRQ15
- * Wide base address selection range so that multiple boards can be paralleled
- * EDR Driver software libraries for C, Pascal, Qbasic Basic and Visual Basic is provided for easy programming.
- * EDR Driver software libraries (DLL) for Windows V3.11 or Win95 are included
- * Third Party Software like LabView for Windows, LabTech Notebook, DasyLab and TestPoint are also provided.

PC 192A Package

The PC 192A package consists of:

- * PC 192A Interface Card
- * PC 192A User's Manual
- * EDR Developers Toolkit User Manual + 5¼ or 3½' diskette
- * 8 x IDC50 Male to Male Connector Lead
- * One 5¼' OR 3½' diskette containing the PC 192A drivers and demonstration software

If any of the items is missing, contact your dealer immediately specifying which components are missing.

Chapter 1: Installation

There are two aspects of the PC 192A that must be configured:

1.1) The Base Address

This address determines where the board is accessed. This can be set by a 8-way DIP switch found on the PC 192A Board. The address range are from 0 to 1fffh.

1.2) Wait State generation

Some computers have very high I/O bus cycles. In this case it is necessary to slow down these cycles when the computer accesses the PC 192A Board. Additional wait states can be set by means of a jumper on the PC 192A Board.

1.3) IRQ JumperSettings

Jumpers on board the card selects an IRQ line for Port C0 and C3 of each 8255 PPI. This is normally applicable if the 8255 PPI is in mode 1 (strobed I/O) or Mode 2 (bidirectional data bus). You can use Port C0 and C3 in mode 0 as well. In this case Port C should be configured as inputs and the IRQ lines will be toggled externally (non-latched).

1.1) Setting the base address

The PC 192A occupies a block of 64 consecutive I/O addresses. The base address setting controls where the block starts. This base address must be unique to the PC 192A only and no other card must occupy this address. If multiple PC 192A boards are installed in one computer then each board must have a different base address.

The base address can be assigned to any location from 0 to 1fffh in 64 byte boundaries. Table 1 shows the I/O addresses occupied by standard interface cards. Refer to the Base Address Setting Table in Appendix A for a list of the various base address settings that the PC 192A can occupy.

The base address setting can be set by adjusting the 8-way dip switch on the PC 192A. Each line on the DIP switch switch compares an address line in I/O space. Switch number 1 compares address line A13; switch number 2: address A12 while switch number 8 compares address line A6. Factory default setting is 300h.

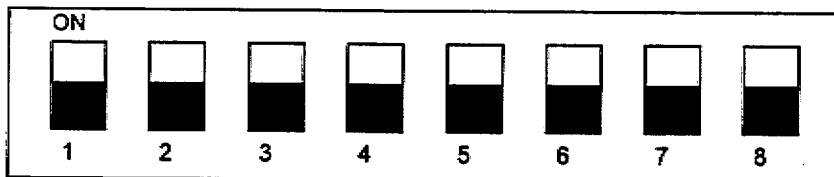
If one of the switches are OFF, then it contributes to the base address. An example is as follows:

Base Address = Switch 5 (Addr A9) + Switch 6 (addr A8)
 = 200 + 100
 = 300h

Table 1: Addresses for standard I/O devices

Address	Standard device
000-1FF	Internal system board
200-20F	Games port
210-217	Expansion unit
220-24F	Reserved
250-257	Not assigned
258-25F	Intel 'Above Board'
260-277	Not assigned
278-26F	Reserved
280-2EF	Not assigned
2F0-2F7	LPT2
2F8-2FF	COM2
300-31F	Prototype Board
320-32F	Hard Disk
330-377	Not assigned
378-37F	LPT1
380-38F	SDLC communications
390-39F	Not assigned
3A0-3AF	Binary comms
3B0-3BF	Mono Display Adaptor
3C0-3CF	Reserved
3D0-3DF	CGA
3E0-3E7	Reserved
3E3-3EF	Not assigned
3F0-3F7	Floppy disk
3F8-3FF	COM1
400-FFF	Not used see below

Table 1: Standard I/O Addresses



2000 1000 800 400 200 100 80 40 Hex Weight when OFF
 A13 A12 A11 A10 A9 A8 A7 A6 Corresponding Address line

Figure 1: Dip Switch Address Weight (in Hex)

Note that addresses from 400h-7FFh cannot normally be used because these addresses are not normally decoded by some cards and I/O devices in the 0h to 3FFh range.

The PC 192A (and most other members of the PC-XX family) can use these address, if and only if the board at address 400h less than the address of the PC 192A also decodes the extra address.

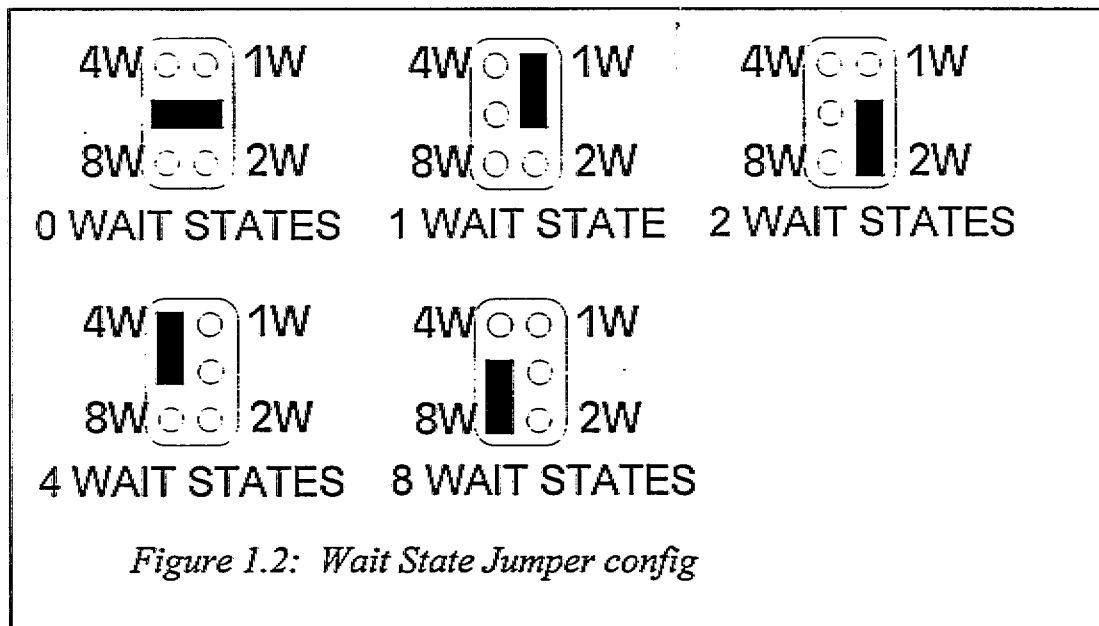
For example, a PC 192A can be installed at address 300h and another one at address 700h (400h locations apart). However, it would not be advisable to install a PC 192A at address 7F8h. This is because communications port COM1 is installed at 3F8h and does not normally decode these extra addresses.

If your computer has boards not listed in Table 1 (such as LAN adaptors, back-up boards or other engineering boards), you should consult the User's Manual for these boards for information on the address ranges used.

In most cases, base address of 300h is a good choice. Address 300h is also the factory default base address setting.

1.2) Wait State Generation on the PC 192A

Additional wait states can be inserted in the I/O bus cycle by changing the jumper setting on JP1 on the PC 192A. This jumper is marked 'Wait State Jumper' on the PC 192A board. Refer to figure 1.2 for the wait state jumper settings. Note that the factory default setting is zero wait states.



In most cases, only a very small number of computers require additional wait states. If the PC 192A seems to be giving incorrect results then try increasing the wait states until correct results are obtained. If the board still does not produce correct results even after the maximum number of wait states has been inserted then the PC 192A or the host computer are defective and should be serviced.

1.3) Interrupt Jumper Settings

Eight subsystems on the PC 192A are used to generate interrupts to the host computer. They are:

PIN FUNCTION	8255 PPI NO	DESCRIPTION
0INTRA	0 PORT C0	Port C0 of 1st 8255 PPI
0INTRB	0 PORT C3	Port C3 of 1st 8255 PPI
1INTRA	1 PORT C0	Port C0 of 2nd 8255 PPI
1INTRB	1 PORT C3	Port C3 of 2nd 8255 PPI
2INTRA	2 PORT C0	Port C0 of 3rd 8255 PPI
2INTRB	2 PORT C3	Port C3 of 3rd 8255 PPI
3INTRA	3 PORT C0	Port C0 of 4th 8255 PPI
3INTRB	3 PORT C3	Port C3 of 4th 8255 PPI
4INTRA	4 PORT C0	Port C0 of 5th 8255 PPI
4INTRB	4 PORT C3	Port C3 of 5th 8255 PPI
5INTRA	5 PORT C0	Port C0 of 6th 8255 PPI
5INTRB	5 PORT C3	Port C3 of 6th 8255 PPI
6INTRA	6 PORT C0	Port C0 of 7th 8255 PPI
6INTRB	6 PORT C3	Port C3 of 7th 8255 PPI
7INTRA	7 PORT C0	Port C0 of 8th 8255 PPI
7INTRB	7 PORT C3	Port C3 of 8th 8255 PPI

Table 1.3: Port Lines used to generate interrupts

The above interrupts are generated if the PPI is set to Mode 1. Full details on the function and use of the interrupts are given later in the manual.

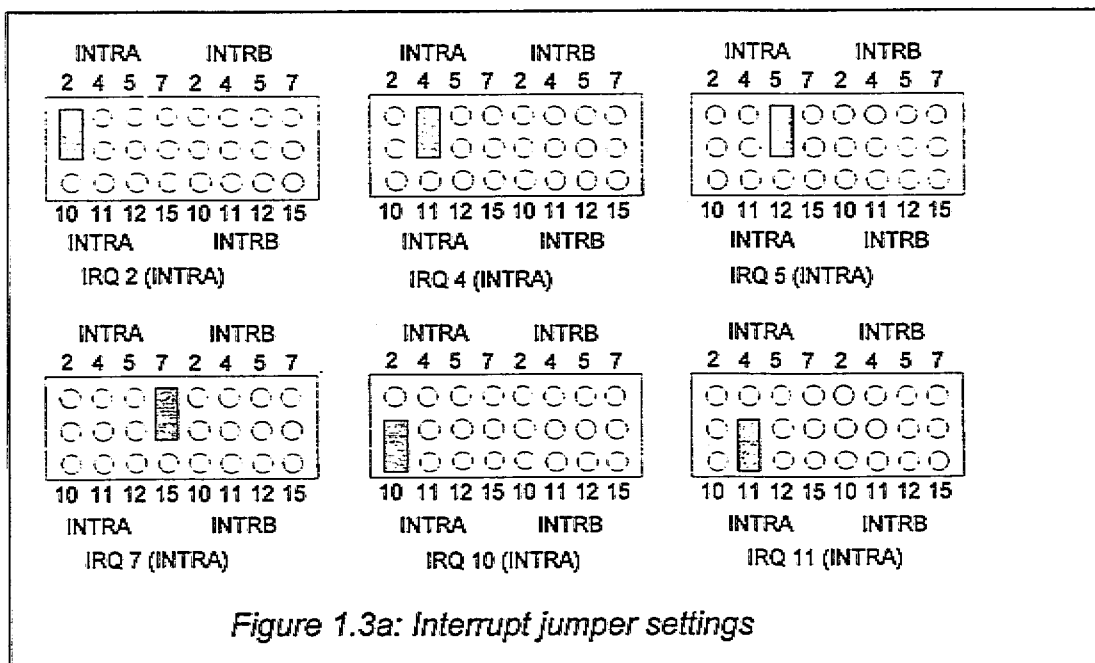


Figure 1.3a: Interrupt jumper settings

Figure 3 shows the interrupt jumper settings for INTRA of the PPI (ie: Port C0). Jumpers can also be placed on the INTRB side of the header in order to link INTRB of the PPI (ie: Port C3) to the interrupt system.

In a standard PC, the interrupt levels are allocated as follows:

Level	Allocation
IRQ0	System timer
IRQ1	Keyboard
IRQ2/IRQ9	Display Adaptor
IRQ3	COM1 (if installed)
IRQ4	COM2 (if installed)
IRQ5	LPT2 (if installed)
IRQ6	Floppy disk controller
IRQ7	LPT1 (if installed)
IRQ10	Not used
IRQ11	Not used
IRQ12	Used by PS/2 Mouse (if installed)
IRQ13	Coprocessor
IRQ14	Primary IDE Harddisk (if installed)
IRQ15	Secondary IDE Harddisk (if installed)

Table 1.3b: Standard interrupt settings

On PC ATs, IRQ2 is used by the system board itself and any interrupt requests on IRQ2 is transparently rerouted to IRQ9.

The default IRQ setting on the PC 192A is IRQ5. Note that unless the interrupt line is specifically enabled by software, the interrupt output from the PC 192A is tri-stated (ie: not connected). It is also tri-stated upon power-up.

1.4) +5V Jumper Settings

Each of the Eight I/O connectors has its own individual jumper to enable or disable the supply of +5V power to external devices. Figure 1.4 illustrates it graphically:

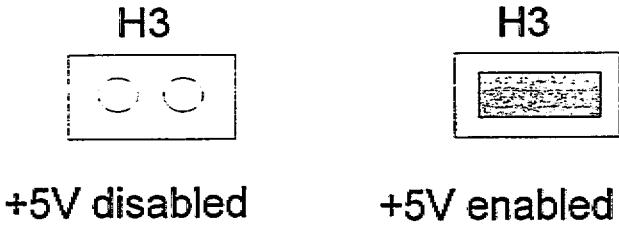


Figure 1.4a: +5V Enable/Disable Jumper Setting

The Jumper attached to each port are as follows:

PPI Number	PPI Connector No	+5V Power JP No
0	H2	H3
1	H4	H5
2	H6	H7
3	H8	H9
4	H10	H11
5	H12	H13
6	H14	H15
7	H16	H17

Table 1.4b: +5V Jumper Reference for each 8255 PPI

If the jumper is IN, then power will be supplied to external devices via Pin 49 on the IDE Header. If the jumper is OUT then no power will be supplied and the computer's power will be isolated from the external devices.

 **Warning**

The maximum permissible current draw on the I/O connector is 100mA. Exceeding this can cause irreparable damage to the PC 192.

DO NOT connect the +5V supply from the computer to an external power supply. If an external power supply has its own power, the corresponding connector's jumper should be removed.

1.5) Connecting the PC 192A to the PC Backplane

- Requirements:
- * XT/286/386/486, ISA, EISA, Pentium Computer
 - * Phillips Screw Driver (or one to match screw on the computer cabinet and bracket)
 - * 8 bit or 16 bit bus slot

Procedure:

- a) Switch off the computer and all attached devices
- b) Unplug power cord from the computer and all attached devices.

Warning

Failure to disconnect all power cables can result in hazardous conditions, as there may be dangerous voltage levels present in externally connected cables.

- c) Remove the top cover from the PC. If you are not sure how to do this, consult the manual supplied with the system unit.
- d) Choose any 8 or 16 bit expansion slot and remove the screw from the metal bracket fixed corresponding to the chosen slot.
- e) Align the gold plated edge connector with the edge socket and the rear adaptor slot with the board bracket. Firmly press the board down into the socket on the computer's system board. Ensure that the board's edge connector is in the socket and has not slipped sideways past the socket.
- f) Replace the screw on the bracket and tighten the screw to the back panel.
- g) Replace the computer's cover. Plug in all cables and switch the computer power on. The PC 192A is now installed.

Note (IBM XT installation)

If you are installing the PC 192A in an XT then the interrupts 9 thru 15 will not be available for use.

CHAPTER 2: Interconnections

2.0) Introduction

The PC 192A thermocouple board plugs into any ISA expansion slot at the gold finger edge connectors J1/J2 and J3/J4. The board communicates to the user circuit via IDE connectors mounted on the PC board. This chapter describes these connectors.

2.1) Connections to the IBM Bus

The PC 192A board may be plugged into any slot of the computer backplane with the exception of J8 slot of the IBM XTs. All data transfers to and from the host computer is channelled via this connectors.

2.2) IDC50 User Connector

The PC 192A interfaces to the external world via eight 50 way IDE male connectors.

PC7	1	2	GND
PC6	3	4	GND
PC5	5	6	GND
PC4	7	8	GND
PC3	9	10	GND
PC2	11	12	GND
PC1	13	14	GND
PC0	15	16	GND
PB7	17	18	GND
PB6	19	20	GND
PB5	21	22	GND
PB4	23	24	GND
PB3	25	26	GND
PB2	27	28	GND
PB1	29	30	GND
PB0	31	32	GND
PA7	33	34	GND
PA6	35	36	GND
PA5	37	38	GND
PA4	39	40	GND
PA3	41	42	GND
PA2	43	44	GND
PA1	45	46	GND
PA0	47	48	GND
+5V	49	50	GND

Figure 4: PC 192 I/O connector

Figure 4 graphically shows the connector together with their pin assignments. Note that the pin connections refer to the pin numbers of the connector when looking into the

connector from the rear of the computer. Also note that the pin numbers are embossed on the connector itself.

The Connectors associated with each 8255 PPI is shown below:

8255 PPI	CONNECTOR NO
0	H2
1	H4
2	H6
3	H8
4	H10
5	H12
6	H14
7	H16

Table 2.2a: PPI Connector identification

2.3) Making Connections

The digital I/O lines on the PC 192A are directly compatible with most forms of TTL and CMOS logic operating from +5V supplies. Detailed specifications on the digital I/O lines are found in Appendix A: Specifications.

The +5V power line on each connector may be individually enabled or disabled by the jumpers. See Chapter 1 for details.

2.4) 8255 PPI Port C Analysis

Some of Port C take on different meanings when the 8255 PPI is programmed to operate in strobed I/O or bidirectional bus mode. They are summarised below in table 2.4a.

Port C Line	Simple I/O Mode 0	Strobed Input Mode 1	Strobed Output: Mode 1	Birectional Bus: Mode 2
C7	I/O	I/O	/OBF _A	/OBF _A
C6	I/O	I/O	/ACK _A	/ACK _A
C5	I/O	IBF _A	I/O	IBF _A
C4	I/O	/STB _A	I/O	/STB _A
C3	I/O	INTR _A	INTR _A	INTR _A
C2	I/O	/STB _B	/ACK _B	I/O
C1	I/O	IBF _B	/OBF _B	I/O
C0	I/O	INTR _B	INTR _B	I/O

Table 2.4a: Port C Line Usage

The symbol '/' indicates that a signal is active low.

When an 8255 PPI is used in on of the handshaking modes, the /STB and IBF lines are used to synchronise input data transfers. The /OBF and /ACK lines are used to synchronise the output data transfers. The signals in the table have the following functions:

Name	Type	Description
/STB	External Input	Strobe Input: A low on this handshaking line loads the data from the peripheral bus into the input latch.
IBF	External Output	Input Buffer Full: A high on this line indicates that the external data has been loaded into the input latch. This is an input acknowledge signal.
/ACK	External Input	Acknowledge: The external device asserts this line low to indicate that the data written to the port by the program has been accepted
/OBF	External Output	Output Buffer Full: The 8255 PPI asserts this line low to indicate to the external device that the program has written data to the selected port. This line can be used to strobe the data into the external device.
INTR	Internal Output	Interrupt Request: This signal becomes active high when the 8255 PPI is requesting service from the host computer. For input operations, it

indicates that there is data in the corresponding port to be read by the program. For output operations, it indicates that the external device has accepted the data and thus the program can write another byte to the 8255 PPI. An interrupt line must be selected with the interrupt jumpers and the appropriate interrupt enable bits must be set, both in the 8255 PPI and the interrupt enable register in order to allow this signal to reach the host computer.

/RD Internal Input

Read Signal: This signal is generated by the control lines of the host computer. It is activated when the program executes an Input instruction from any of the PC 192A registers.

/WR Internal Input

Write Signal: This signal is generated by the control lines of the host computer. It is activated when the program executes an Output instruction from any of the PC 192A registers.

Figure 2.4b: Port C Handshaking Lines

2.5) Power supply connections

The +5V power with digital ground are available on the IDE50 Connector on each of the eight 8255 PPI ports. The +5V power can be enabled/disabled via jumpers. Refer to the silkscreen text/jumpers in the PC 192A Board.

CHAPTER 3: Register Structure

3.0) Introduction

At the lowest level, the PC 192A can be programmed using I/O input and output instructions. This chapter contains the information on all the PC 192A registers. Although programming the board is not difficult, it is time consuming and requires detailed knowledge of the PC 192A as well as the operation of the host PC and its operating system. In order to simplify the process, a set of driver libraries is provided. The use of these libraries allow access to all the board's functions and is described in Chapter 5: Programming guide.

The PC 192A occupies 64 consecutive addresses in the computer's I/O space. The layout of these registers are shown in Table 4: PC 192A register structure. The offset of the registers are given as offset addresses from the base address of the board. This base address is set with the Dip Switch as detailed in Chapter 2: Installation.

Offset	Read	Write
0	PPI 0: Port A (DIO0A)	PPI 0: Port A (DIO0A)
1	PPI 0: Port B (DIO0B)	PPI 0: Port B (DIO0B)
2	PPI 0: Port C (DIO0C)	PPI 0: Port C (DIO0C)
3	PPI 0: Control Register (DIO0CTL)	
4	PPI 1: Port B (DIO1B)	PPI 1: Port B (DIO1B)
5	PPI 1: Port B (DIO1B)	PPI 1: Port B (DIO1B)
6	PPI 1: Port C (DIO1C)	PPI 1: Port C (DIO1C)
7	PPI 1: Control Register (DIO2CTL)	
8	PPI 2: Port A (DIO2A)	PPI 2: Port A (DIO2A)
9	PPI 2: Port B (DIO2B)	PPI 2: Port B (DIO2B)
10	PPI 2: Port C (DIO2C)	PPI 2: Port C (DIO2C)
11	PPI 2: Control Register (DIO2CTL)	
12	PPI 3: Port A (DIO3A)	PPI 3: Port A (DIO3A)
13	PPI 3: Port B (DIO3B)	PPI 3: Port B (DIO3B)
14	PPI 3: Port C (DIO3C)	PPI 3: Port C (DIO3C)
15	PPI 3: Control Register (DIO3CTL)	
16	PPI 4: Port A (DIO4A)	PPI 4: Port A (DIO4A)
17	PPI 4: Port B (DIO4B)	PPI 4: Port B (DIO4B)
18	PPI 4: Port C (DIO4C)	PPI 4: Port C (DIO4C)
19	PPI 4: Control Register (DIO4CTL)	
20	PPI 5: Port A (DIO5A)	PPI 5: Port A (DIO5A)
21	PPI 5: Port B (DIO5B)	PPI 5: Port B (DIO5B)
22	PPI 5: Port C (DIO5C)	PPI 5: Port C (DIO5C)
23	PPI 5: Control Register (DIO5CTL)	

Offset	Read	Write
24	PPI 6: Port A (DIO6A)	PPI 6: Port A (DIO6A)
25	PPI 6: Port B (DIO6B)	PPI 6: Port B (DIO6B)
26	PPI 6: Port C (DIO6C)	PPI 6: Port C (DIO6C)
27	PPI 6: Control Register (DIO6CTL)	
28	PPI 7: Port A (DIO7A)	PPI 7: Port A (DIO7A)
29	PPI 7: Port B (DIO7B)	PPI 7: Port B (DIO7B)
30	PPI 7: Port C (DIO7C)	PPI 7: Port C (DIO7C)
31	PPI 7: Control Register (DIO7CTL)	
32	IRQ Enable Register 0 (IRQEN0)	IRQ Enable Register 0 (IRQEN0)
33	IRQ Enable Register 1 (IRQEN1)	IRQ Enable Register 1 (IRQEN1)

Table 4: PC 192A register structure

3.1) DIOA - Port A Register of first PPI (offset 0, read/write)

This register is port A of the first PPI. It can be operated in one of three modes. The operating mode is set by writing to the DIO0CTRL register, as described below.

DIOA Register (read/write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A7	0A6	0A5	0A4	0A3	0A2	0A1	0A0

Bit 0 thru 7: The bits 0A7 (MSB) down to 0A0 (LSB) reflect the status of Port A I/O lines. Depending on the programmed I/O mode of the port, the lines may be inputs, outputs or bidirectional.

3.2) DIOB - Port B Register of first PPI (offset 1, read/write)

This register is port B of the first PPI. It can be operated in one of three modes. The operating mode is set by writing to the DIO0CTRL register, as described below.

DIOB Register (read/write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B7	0B6	0B5	0B4	0B3	0B2	0B1	0B0

Bit 0 thru 7: The bits 0B7 (MSB) down to 0B0 (LSB) reflect the status of Port B I/O lines. Depending on the programmed I/O mode of the port, the lines may be inputs, outputs or bidirectional.

3.3) DIOC - Port C Register of first PPI (offset 2, read/write)

This register is port C of the first PPI. It can be operated in one of three modes. The operating mode is set by writing to the DIO0CTRL register, as described below.

DIOC Register (read/write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0C7	0C6	0C5	0C4	0C3	0C2	0C1	0C0

Bit 0 thru 7: The bits 0C7 (MSB) down to 0C0 (LSB) reflect the status of Port C I/O lines. Depending on the programmed I/O mode of the port, the lines may be inputs, outputs or bidirectional.

3.4) DIO0CTRL - Control register of the first PPI (offset 3, write only)

This register is used to control the operating modes of the first PPI or set and reset individual bits in port C of the PPI. The layout of the register is shown below. Note that the function and bit names of the register depend on the setting of bit 7.

DIO0CTRL Register (write only) - Configuration Mode

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	MAS ₁	MSA ₀	PA	PCU	MSB ₀	PB	PCL

↑ Mode Set Flag ↑ Group A Mode Selection ↑ Port A I/O Direction ↑ Port C Upper I/O direction ↑ Group B Mode Selection ↑ Port B I/O dir ↑ Port C Lower I/O dir

DIO0CTRL Register (write only) - Bit Set/Reset Mode

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	x	x	x	BS2	BS1	BS0	S/R

↑ Bit Set/Reset Flag ↑ Don't Care ↑ Bit Select ↑ Set / Reset

Bit 0 thru 7: Function Select: Setting this bit to 1 set the register in Configuration Mode. Writing a 0 to this bit configures this register in Set/Reset Mode.

The functions of the remaining bits are described below depending on the setting of bit 7:

Configuration Mode

Bits 6-5: Group A mode select: These two bits set the mode of the Group A Ports. These are Port A and the upper four lines of port C. The bit combination are as follows:

MSA ₁	MSA ₀	Group A I/O Mode
0	0	Mode 0, simple I/O
0	1	Mode 1, Strobed I/O
1	x	Mode 2, Bidirectional bus

Bit 4: Port A I/O Direction: If this bit is set, then Port A functions as an input. If it is 0, then Port A is configured as an output.

Bit 3: Port C Upper I/O Direction: If this bit is set, then the upper four lines of Port C function as inputs. If the bit is 0, then the lines become outputs.

Bit 2: Group B Mode Select: This bit sets the mode of the group B ports. These are Port B and the lower four lines of Port C. The bit combinations are as follows:

MSB ₀	Group B I/O Mode
0	Mode 0, Simple I/O
1	Mode 1, Strobed I/O

Bit 1: Port B I/O Direction: If this bit is set, then Port B functions as an input. If it is 0, then Port B is configured as an output.

Bit 0: Port C Lower I/O Direction: If this bit is set, then the lower four lines of Port C functions as inputs. If the bit is 0, then the lines become outputs.

Note

Group B can only be used for simple or strobed I/O

Bit Set/Reset Mode

- Bits 6-5: These bits have no effect in this function.
- Bits 3-1: Bit Select: These bits select the bit in port C which is to be modified. A code of 000 selects Port C line 0 to set or reset. 001 selects line 1 and so on up to 111 which selects line 7.
- Bit 0: Set/Reset: This bit specifies the state into which the selected Port C line will be placed. Writing a 1 will make the line go high and a 0 makes it go low. This operation has no effect on the other lines of Port C.

3.5) IEN0 - Interrupt / Status register 0 (offset 32: read/write)

This register contains control/status bits for enabling the interrupts from the 8255 PPIs (PPI0 thru PPI3) to the PC Bus. On power up or reset, all these bits are in a reset state. Hence all the Port lines are disabled from the PC bus.

IEN0 Register (Read / Write mode)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3PC3	3PC0	2PC3	2PC0	1PC3	1PC0	0PC3	0PC0

- Bit 0-1: Enable Interrupt from PPI0: Setting this bit to 1 enables the first interrupt outputs (Port C0 and C3) from the first PPI on to the PC bus. With the PPI in mode 1 or mode 2, this electrically connects the $INTR_A$ and $INTR_B$ line to the selected interrupt lines of the host computer. Writing a zero to this bit disables the two Interrupts from the PC I/O channel.

Reading back these bits determines the status of the first PPI interrupt enable lines.

- Bit 2-3: Enable Interrupt from PPI1: Setting this bit to 1 enables the interrupt outputs (Port C0 and C3) from the second PPI on to the PC bus. With the PPI in mode 1 or mode 2, this electrically connects the $INTR_A$ and $INTR_B$ line to the selected interrupt lines of the host computer. Writing a zero to this bit disables the two Interrupts from the PC I/O channel.

Reading back these bits determines the status of the second PPI interrupt enable lines (ie: Port C0 corresponds to Bit 0 and Port C3 corresponds to Bit 1).

- Bit 4-5: Enable Interrupt from PPI2: Setting this bit to 1 enables the interrupt outputs (Port C0 and C3) from the third PPI on to the PC bus. With the PPI in mode 1 or mode 2, this electrically connects the $INTR_A$ and $INTR_B$ line to the selected interrupt lines of the host computer. Writing a zero to this bit disables the two Interrupts from the PC I/O channel.

Reading back these bits determines the status of the third PPI interrupt enable lines (ie: Port C0 corresponds to Bit 0 and Port C3 corresponds to Bit 1).

Bit 6-7: Enable Interrupt from PPI3: Setting this bit to 1 enables the interrupt outputs (Port C0 and C3) from the fourth PPI on to the PC bus. With the PPI in mode 1 or mode 2, this electrically connects the $INTR_A$ and $INTR_B$ line to the selected interrupt lines of the host computer. Writing a zero to this bit disables the two Interrupts from the PC I/O channel.

Reading back these bits determines the status of the fourth PPI interrupt enable lines (ie: Port C0 corresponds to Bit 0 and Port C3 corresponds to Bit 1).

☞ Additional External Interrupts

Note that the Port C0 and Port C3 lines are enabled onto the selected PC I/O Bus IRQ line by the bit regardless of the mode setting of the 8255 PPI. This means that if Port C0 and C3 lines are not being used for digital I/O, they can be used as additional unlatched external interrupt inputs.

3.6) IEN1 - Interrupt / Status register 1 (offset 33: read/write)

This register contains control/status bits for enabling the interrupts from the 8255 PPIs (PPI4 thru PPI7) to the PC Bus. On power up or reset, all these bits are in a reset state. Hence all the Port lines are disabled from the PC bus.

IEN1 Register (Read / Write mode)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
7PC3	7PC0	6PC3	6PC0	5PC3	5PC0	4PC3	4PC0

Bit 0-1: Enable Interrupt from PPI4: Setting this bit to 1 enables the interrupt outputs (Port C0 and C3) from the **fifth PPI** on to the PC bus. With the PPI in mode 1 or mode 2, this electrically connects the $INTR_A$ and $INTR_B$ line to the selected interrupt lines of the host computer. Writing a zero to this bit disables the two Interrupts from the PC I/O channel.

Reading back these bits determines the status of the **fifth PPI** interrupt enable lines.

Bit 2-3: Enable Interrupt from PPI5: Setting this bit to 1 enables the interrupt outputs (Port C0 and C3) from the **sixth PPI** on to the PC bus. With the PPI in mode 1 or mode 2, this electrically connects the $INTR_A$ and $INTR_B$ line to the selected interrupt lines of the host computer. Writing a zero to this bit disables the two Interrupts from the PC I/O channel.

Reading back these bits determines the status of the **sixth PPI** interrupt enable lines (ie: Port C0 corresponds to Bit 0 and Port C3 corresponds to Bit 1).

Bit 4-5: Enable Interrupt from PPI6: Setting this bit to 1 enables the interrupt outputs (Port C0 and C3) from the third PPI on to the PC bus. With the PPI in mode 1 or mode 2, this electrically connects the $INTR_A$ and $INTR_B$ line to the selected interrupt lines of the host computer. Writing a zero to this bit disables the two Interrupts from the PC I/O channel.

Reading back these bits determines the status of the sixth PPI interrupt enable lines (ie: Port C0 corresponds to Bit 0 and Port C3 corresponds to Bit 1).

Bit 6-7: Enable Interrupt from PPI7: Setting this bit to 1 enables the interrupt outputs (Port C0 and C3) from the fourth PPI on to the PC bus. With the PPI in mode 1 or mode 2, this electrically connects the $INTR_A$ and $INTR_B$ line to the selected interrupt lines of the host computer. Writing a zero to this bit disables the two Interrupts from the PC I/O channel.

Reading back these bits determines the status of the eighth PPI interrupt enable lines (ie: Port C0 corresponds to Bit 0 and Port C3 corresponds to Bit 1).

Additional External Interrupts

Note that the Port C0 and Port C3 lines are enabled onto the selected PC I/O Bus IRQ line by the bit regardless of the mode setting of the 8255 PPI. This means that if Port C0 and C3 lines are not being used for digital I/O, they can be used as additional unlatched external interrupt inputs.

Chapter 4: Programming Guide

4.0) Introduction

This chapter describes programming the PC 192A at its lowest level. In order to accomplish this, detailed knowledge of chapter 4 and the system hardware is required.

As an alternative to low level programming, driver software is provided with the PC 192A. This is described in Chapter 5.

The advantages of using the driver software are:

- a) Detailed knowledge of the PC 192A is not required.
- b) The Driver Libraries supports multiple boards. In other words, you can cascade boards in the same computer.
- c) The Driver Library is callable from most high level languages.

Programmers who need to incorporate special routines into their application will need to read this chapter. Examples are application programs written in Clarion, Clipper, etc.

Once the PC 192A has been installed into the computer and external connections are made, the board is in an operational state. The PC 192A occupies 64 consecutive I/O addresses starting from the board's base address. The base address is set by the DIP Switch on the PC 192A. Programming the PC 192A is done by using the input/output instructions. Reading and writing to these addresses allows data to be moved to and from the PC 192A.

Reading and writing to these ports typically takes on the form of one of the following instructions:

Language	Port Read	Port Write
'C'	value = inp(addr);	outp(addr, value);
Pascal	value := port[addr];	port[addr] := value;
Assembly	mov al, value mov dx, addr in al, dx	mov al, value mov dx, addr out dx, al
where:	addr is the I/O location of the PC 192A registers value is the byte read or written to the register	

Mode 0 Programming

To use the 8255 in mode 0:

- i) Write a single byte to the control register to set the 8255 PPI into mode 0 with the three ports configured for the desired data direction.
- ii) Read or write from the I/O port corresponding to an 8255 PPI port (Port A, B or C) as many times as necessary to obtain or transfer the required amount of data.

4.3) Mode 1: Strobed I/O

In this mode data transfers are controlled by handshaking signals and hardware interrupts. Some of the port C lines are used for these control signals. Hence they take on a different functions and names. Refer to Chapter 3: Register Structure for an in depth analysis of the bit functions.

The following characterise Mode 1:

- * Two groups, Group A and B. Each group consists of an 8 bit data port and three control lines.
- * Certain Port C lines take on special functions.
- * The data ports can be either input or output ports.
- * Both inputs and outputs are latched.
- * One 20 bit simple I/O Port
- * Data transfer by interrupts or polled I/O.

With both groups configured in mode 1, a single 8255 PPI can be read or write data 16 bits wide.

GROUP A

Configuration Info
to PIACNTRL Register

1	0	1	1	1/0	X	X	X
---	---	---	---	-----	---	---	---

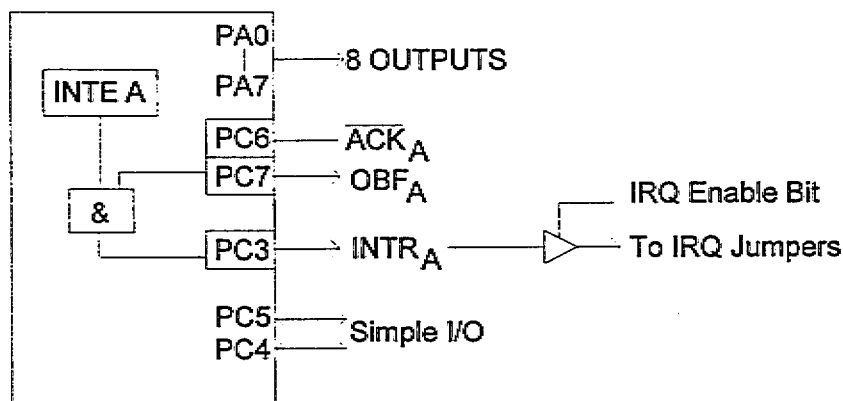
PC7,6

1 = Input

0 = Output

X = Not applicable

MODE 1 (PORT A)



GROUP B

Configuration Info
to PIACNTRL Register

1	X	X	X	X	1	1	X
---	---	---	---	---	---	---	---

X = Not Applicable

MODE 1 (PORT B)

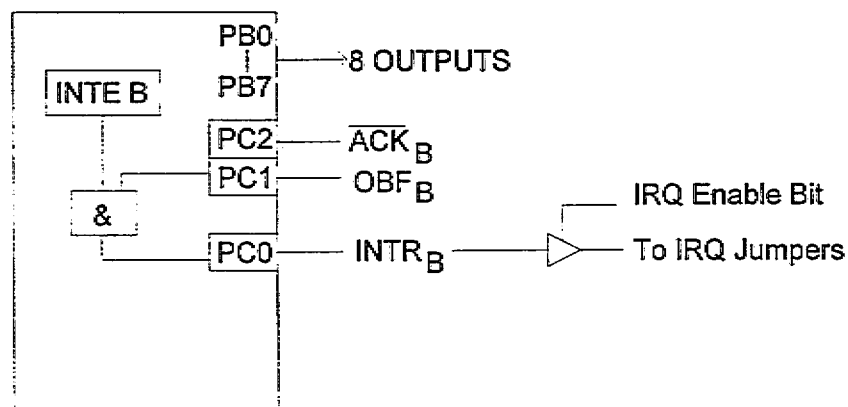


Figure 4.3: Mode 1 Input of an 8255

Mode 1 Programming

To use the 8255 PPI in mode 1 input with interrupts:

- Write a byte to control register to configure the 8255 PPI for mode 1 and the appropriate group for data input.
- With the bit set/reset operation, write a 1 to the Interrupt Enable Flip-Flop (INTE) of the desired port of the appropriate 8255 PPI.
- Write a byte to the IEN0 or IEN1 register to enable interrupts from the appropriate 8255 PPI to the host computer.
- The external device pulses the Strobe ($/STB$) input line on the digital I/O Connector low. The trailing edge of this loads the data into the input port.
- The Input Buffer Full (IBF) output line goes high on the digital I/O connector to indicate that the data has been loaded into the input latch.

- f) When the external device pulls the /STB line high, the Interrupt Request line (INTR) goes high. This indicates to the host computer that there is data to be read from the 8255 PPI.
- g) The computer reads the data using an interrupt service routine (ISR) and by doing so, automatically resets the INTR signal.
- h) The external device can now pulse the /STB low again to make the PC 192A read another byte of data and hence repeat the cycle.

Whenever a group of the 8255 PPI is in mode 1 input, the status of the handshaking lines and interrupt signals can be obtained by reading Port C. The byte read contains the following information:

Port C Mode 1 Input Status Information

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C7	C6	IBF _A	INTE _A	INTR _A	INTE _B	IBF _B	INTR _B

The 8255 PPI may alternatively be used in mode 1 and the data read by polled transfer.

The method is as follows:

- a) Write a byte to control register to configure the 8255 PPI for mode 1 and the appropriate group for data input.
- b) The program continually monitors the IBF line by reading Port C.
- c) The external device pulses the Strobe (/STB) input line on the digital I/O Connector low. The trailing edge of this loads the data into the input port.
- d) The Input Buffer Full (IBF) output line goes high on the digital I/O connector to indicate that the data has been loaded into the input latch.
- e) This also causes the corresponding IBF bit in port C to be set and the program can thus read the data.
- f) The external device can now pulse the /STB low again to make the PC 192A read another byte of data and hence repeat the cycle.

The program could also enable the INTR line with the INTE flip-flop and then monitor INTR instead of the IBF line. In this case, interrupts to the host computer are not enabled in the IEN0 or IEN1 register.

GROUP A

Configuration Info
to PIACNTRL Register

1	0	1	0	1/0	X	X	X
---	---	---	---	-----	---	---	---

↑
PC5, 4
1 = Input
0 = Output
X = Not applicable

GROUP B

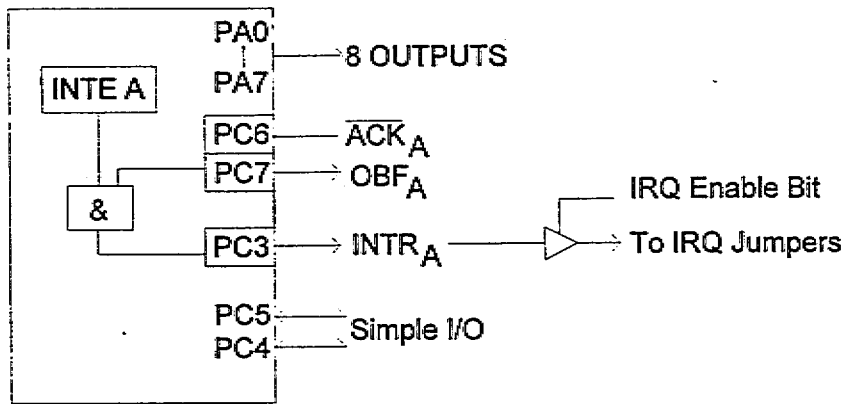
Configuration Info
to PIACNTRL Register

1	X	X	X	X	1	0	X
---	---	---	---	---	---	---	---

INTE B controlled by bit
set/reset of PC2

= Not Applicable

MODE 1 (PORT A)



MODE 1 (PORT B)

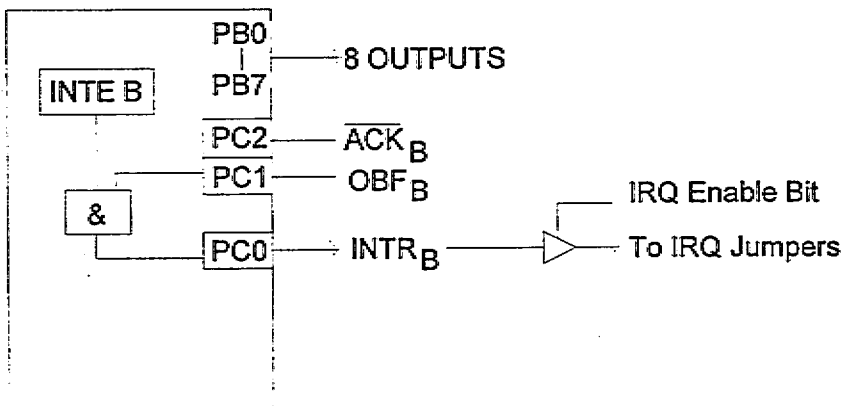


Figure 4.3b: Mode 1 Output of an 8255

To use the 8255 PPI in mode 1 output with interrupts:

- a) Write a byte to control register to configure the 8255 PPI for mode 1 and the appropriate group for data output.
- b) With the bit set/reset operation, write a 1 to the Interrupt Enable Flip-Flop (INTE) of the desired port of the appropriate 8255 PPI.
- c) The 8255 PPI Interrupt Request Output (INTR) then goes high.
- d) Write a byte to the IEN0 or IEN1 register to enable interrupts from the appropriate 8255 PPI to the host computer.
- e) The host computer detects the INTR line is active. From an Interrupt Service Routine (ISR), it writes a byte to the output port. This automatically resets the INTR line.
- e) The Output Buffer Full (/OBF) line to the digital I/O connector goes low to indicate that there is data to be read by the external device from the 8255 PPI.

- f) The external device pulses the Acknowledge (/ACK) input low and then high again to indicate that it has read the data.
- g) This makes the INTR line go high again and the cycle may be repeated until all the required data has been written.

Whenever a group of the 8255 PPI is in mode 1 output, the status of the handshaking lines and interrupt signals can be obtained by reading Port C. The byte read contains the following information:

Port C Mode 1 Output Status Information

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/OBF _A	INTE _A	C5	C4	INTR _A	INTE _B	/OBF _B	INTR _B

The 8255 PPI may alternatively be used in mode 1 and the data written by polled transfer.

This is done as follows:

- a) Write a byte to control register to configure the 8255 PPI for mode 1 and the appropriate group for data output.
- b) The program continually monitors the /OBF line by reading Port C, waiting for it to go high. A high indicates that the last data written to the port has been read by the external device.
- c) Then the program can write new data to the port.
- d) The /OBF line to the digital I/O connector goes low to indicate that there is data to be read by the external device from the 8255 PPI.
- e) The external device pulls the /ACK input low to read the data.
- f) This makes the /OBF line go high again and the cycle may be repeated until all the required data has been written.

The program could also enable the INTR line with the INTE flip-flop and then monitor INTR instead of the /OBF line. In this case, interrupts to the host computer are not enabled in the IEN0 and IEN1 (Interrupt Enable Register).

4.4) Mode 2: Strobed Bidirectional Bus I/O

This mode provides a means for communicating with an external device using an 8-bit bus for both transmitting and receiving data. Both input and output handshaking signals similar to mode 1 are provided to maintain proper bus flow discipline. Hardware interrupts signal the host computer that the port needs attention.

The following characterise Mode 2:

- * Only group A operates in mode 2.
- * One 8-bit bidirectional port, functions as both input and output.
- * Five of the port C lines take on special functions.
- * Both inputs and outputs are latched.
- * One 3-bit simple I/O port available on each PPI
- * Data transfer by interrupts or polled I/O.

With all eight 8255 PPI of the PC 192A configured in mode 2, the board provides the function of a full 64 bit wide bidirectional data bus.

GROUP A

Configuration Info
to PIACNTRL Register

1	1	X	X	X	0/1	1/0	1/0
---	---	---	---	---	-----	-----	-----

Group B Mode

0 = Mode 0

1 = Mode 1

Port B

0 = Output

1 = Input

Port C2-C0

0 = Output

1 = Input

X = Not Applicable

INTE 1 controlled by
bit set/reset of PC6

INTE 2 controlled by
bit set/reset of PC4

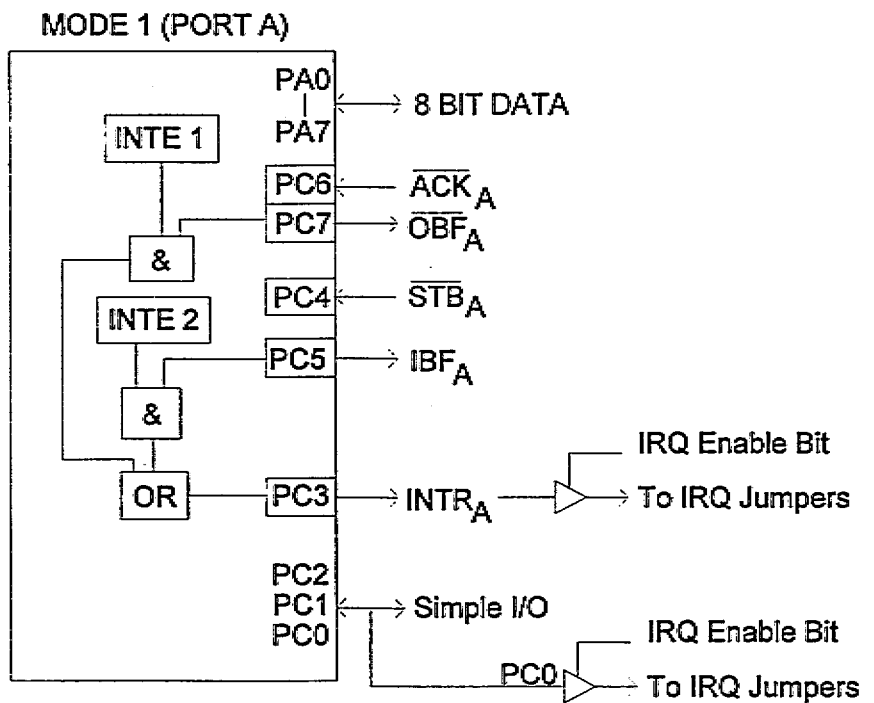


Figure 4.4: Mode 2 of an 8255

4.4.1) Mode 2 Programming

To use the 8255 PPI in mode 2 with hardware interrupt transfer:

- a) Write a byte to the control register to configure the 8255 PPI for mode 2 operation.
- b) Select an interrupt level with the interrupt jumpers and enable 8255 interrupt(s) in the PC 192A Interrupt Enable Registers (IEN0 and IEN1).
- c) With the bit set/reset operation, write a 1 to the Interrupt Enable number 1 flip-flop (INTE₁) to enable output transfer interrupts. Write a 1 to the Interrupt Enable number 2 flip-flop (INTE₂) to enable input transfer interrupts. Both input and output interrupts may be enabled at the same time.
- d) With both interrupt flip-flop enabled, the interrupt request line to the host computer is activated if the external device has a strobed data into the 8255 input latch or if the external device has read the PC 192A output data from the output latch.
- e) The host computer detects the INTR line is active. The Interrupt Service Routine (ISR) which services this interrupt determines whether it was an input or output interrupt by checking bit 5 (IBF_A) of the mode 2 status information from port C. In the IBF line is high (bit 5 is set) then it is an input interrupt, otherwise it is an output interrupt.
- f) In either case, the ISR simply reads the data from or writes to the 8255 PPI and then issues an end of interrupt command (EOI) to the interrupt controller.
- g) This generates the appropriate handshake signals from the 8255 PPI to the digital I/O connector.
- h) The cycle continues when the next interrupt is generated.

Whenever the 8255 PPI is in mode 2, the status of the handshaking lines and the interrupt signals can be obtained by reading port C. The byte read contains the following information:

Port C Mode 2 Status Information

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/OBF _A	INTE ₁	IBF _A	INTE ₂	INTR _A	C2	C1	C0

The 8255 PPI may alternatively be used in mode 2 with the data read and written by polled I/O transfer. This is done as follows:

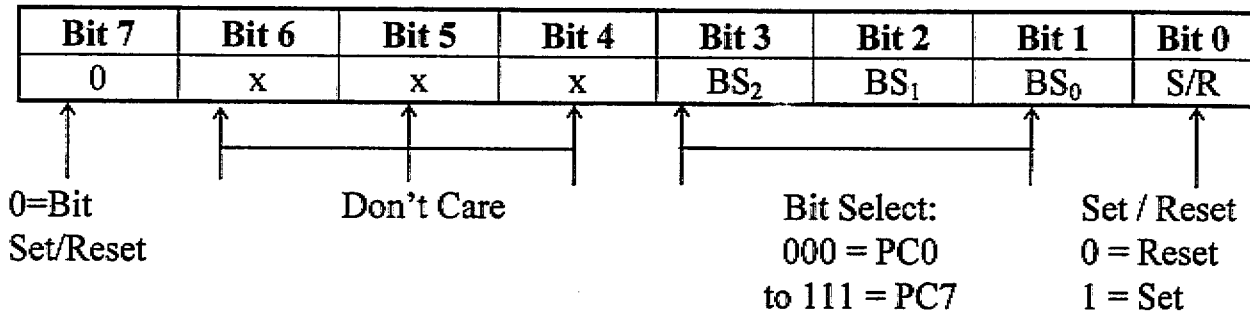
- a) Write a byte to the control register to configure the 8255 PPI for mode 2 operation.
- b) The program continually monitors both the IBFA and /OBFA line by reading port C.
- c) If port C bit corresponding to IBFA is set, this indicates that the external device has written data into the input latch. The program must therefore read the data from port A.
- d) If the port C bit corresponding to /OBFA is set, this indicates that the external device has read the data written by the program to port A. It must therefore write more data to Port A.
- e) This process can be repeated until the required amount of data has been read and written.

Interrupt to the host computer must not be enabled in the Interrupt Enable registers (IEN0 and IEN1) when data is transferred by polled I/O.

4.5) Single Bit Set/Reset

Any of the eight bits of port C can be set or reset using a single output instruction to the DIOCTRL register. When Port C is being used as status/control for port A or B, any of these bits can be set or reset just as if they were data outputs. The format of the byte to write to the DIOCTRL register to set or reset a port C bit is repeated below.

DIO0CTL Register (write only) - Bit Set/Reset Mode



4.6) Mixed Mode Programming

An 8255 PPI is not constrained to operate in one mode only. For example, Port A may operate in mode 2 and port B may then operate in either mode 1 or mode 0. For any combination, some or all of the Port C lines are used for control or status. The remaining port C lines may be used in mode 0 either as inputs or outputs.

A read operation of port C returns all the port C lines except the /ACK and /STB lines. In their place will appear the status of the Interrupt Enable flip-flops (INTE_x). This is illustrated in figures 6 to 8 above and the status information bytes which follow the figures.

A write operation to port C will affect lines programmed as mode 0 outputs. To write to any port C output programmed as a mode 1 output or to change an interrupt enable flip-flop, the Bit Set/Reset operation must be used.

Using the Bit Set/Reset command, any port C line programmed as an output (including INTR, IBF and /OBF) can be written or an interrupt enable flag set or reset. Lines programmed as inputs (including /ACK and /STB) are not affected by this command. Writing to these lines will affect the interrupt enable flags.

Chapter 5: Driver Software

Full driver software is supplied with the PC 192A package. Full details are explained in the EDR Software developers kit User Manual. A summary of what these drivers consist of are explained below.

Both DOS and Windows Languages are supported: They are:

DOS Languages:

Borland C/C++ Version 3.1 or 4.0
Microsoft C/C++ Version 6.0 or 7.0
Borland Pascal / Turbo Pascal Version 6.0 or 7.0
Microsoft QuickBasic Version 4.5

Windows Languages:

Delphi V1.00 / V2.00
Borland C/C++ 3.1 or 4.0
Microsoft C/C++ 6.0 or 7.0
Borland Pascal / Turbo Pascal Version 6.0 or 7.0
Visual Basic V1.00 thru V4.00

5.1) Board Handles

All EDR functions used above require a board handle as the first parameter. The board handle defines which board is affected by the function call. Using this method has several advantages, For example, there is no need for a 'select board' function; working with parallel boards is much easier; different applications using the EDR at the same time will not conflict with each other.

Board handle are integers obtained by calling `EDR_AllocBoardHandle` (see 7.2 of EDR Developers Toolkit). Once allocated a board handle must be initialised to the PC 192A before it can be accessed. this is achieved by calling `EDR_InitBoard` or `EDR_InitBoardType` (see 7.5 of EDR manual) with the base address or `EDR_loadConfiguration` (see section 7.8 of EDR manual).

`EDR_InitBoard` will attempt to detect the PC192A at the base address specified.

5.2) Interrupt functions

Port C0 and C3 of each 8255 PPI are connected to the IRQ line via a tri-state buffer. An ISR can be installed using the EDR driver functions to service these lines when pulses toggles the C0 and C3. Note that these lines are not latched in Mode 0. Hence the pulses must be long enough for the PC's Interrupt system to detect it.

These functions are callable from virtually any programming language. See the EDR Software Developers Kit User Manual.

5.3) Quick Function Reference

The PC 192A Enhanced 8 port 8255 PPI Board utilises the following functions calls contained in the EDR driver developers toolkit. They are:

Function Name	Description
EDR_DIOConfigurePort	Configures a digital port for a particular mode and direction. EDR only directly supports mode 0 (EDR_DIO_SIMPLE) with the driver functions. Other modes can be used but you will need to write your own support code.
EDR_DIOGetPortConfig	Gets the current configuration of the port A, B or C in any of the 8255 PPIs.
EDR_DIOLineInput	Gets the status of a single line (bit) in a digital input port. If the port is an output port then the last value written to the line (bit) is returned.
EDR_DIOLineOutput	Changes a single line (bit) in a digital output port.
EDR_DIOPortOutput	Writes a byte of data to the PC192A I/O port
EDR_DIOPortInput	Reads a byte of data from the PC192A I/O Port. If the port is an output port then the last value written to the port is returned.
EDR_HasDOReadback	Indicates if a particular board type's digital output ports can be read back or not. If the board supports readback from DO ports then doing EDR_DIOPortInput or EDR_DIOLineInput on an output port will read the last value written to the port from a board register. If the readback is not supported the EDR returns its software copy of the last value written using EDR_DIOPortOutput or EDR_DIOLineOutput.
EDR_EnableInterrupt	Enables or disables the specified interrupt on the PC 192A. Note that this just programs the board registers (ie: writing to IEN0 and IEN1 Registers) so that it will/will not generate the interrupt. If the interrupt from the is masked then interrupts from the board will be blocked. Disabling interrupts or enabling interrupts when they are already enabled may generate extra interrupts. Make sure that your ISR are prepared to handle these rogue interrupts.
EDR_InstallISR	Installs an ISR for the specified hardware interrupt request

Function Name	Description
EDR_UninstallISR	Removes an interrupt service routine that was installed with EDR_InstallISR
EDR_InstallBoardISR	Installs an ISR for a particular type of interrupt installed on the PC192A.
EDR_UninstallBoardISR	Removes an interrupt service routine that was installed with EDR_InstallBoardISR
EDR_MaskIRQ	Masks or unmask a particular IRQ level
EDR_MaskBoardIRQ	Masks or unmask a particular board interrupt
EDR_ResetInterrupt	Resets an interrupt latch on the PC192A and sends an EOI command to one of the PCs interrupt controllers on completion of the interrupt
EDR_AllocBoardHandle	Allocates a new board handle to the PC192A. If no board handles are available then a 0 is returned. This is particularly useful is multiple PC192A are present in the same.computer.
EDR_FreeBoardHandle	Releases a board handle allocated to the PC192A making it available to any other PC card
EDR_InitBoardType	Initialises a board and allocates a board handle to it
EDR_ConfigDialog	Diplays a dialog box that allows the user to manually configure the driver for the Board in the computer
EDR_SaveConfiguration	Function writes configuration information to a file for later loading with EDR_LoadConfiguration
EDR_LoadConfiguration	Loads details of the Cards configuration from the file created by EDR_SaveConfiguration
EDR_RestoreDefaults	Restores factory default configuration for a baord attached to a handle
EDR_IsBaseAddressInUse	Checks if any board initialised with EDR is using the specified I/O address
EDR_DetectBoard	Tries to determine the type of board present at a specified I/O address.
EDR_SetBoardType	Changes the board type attached to a board handle
EDR_SetIRQLevel	Set the IRQ level EDR will use for the interrupt ID specified.
EDR_NumDIOPorts	Gets the number of DIO ports a board has.
EDR_ValidDIOPortConfig	Checks the configuration of a digital port.
EDR_ValidInterruptID	Checks to see if the board supports the ID specified
EDR_ValidIRQLevel	Checks an IRQ level

Chapter 6: Testing the PC 192A

Before attempting to interface the PC 192A with your application, it is essential that you test the board first. This is done using the following procedure:

6.1) Testing the PC 192A Board

Install the PC 192A using the procedure described in the Chapter 2: Installation. Proceed as follows:

- * Switch the Computer on
- * On the DOS prompt, go to the C:\EDR\TPAS\DEMOS\ sub-directory
- * Run the DILOOP.EXE test program with parameter 300 where 300 is the base address of the PC 192A.

If an error message 'Board not found' appears on your screen then the PC 192A was not installed at that address. Try a different base address as specified in Appendix A (eg: 700h) and re-run the test S/W. If the problem persists then try increasing the wait states on the PC 192A Board and re-run test software. The board should work.

If the PC 192A is found, a message will appear on the screen: 'PC 192A Board found'. The program will walk a bit through port A and display all other ports (programmed as inputs) in Hex. You may feed any TTL signal input to the above ports.

6.2) Connecting Normally Open devices to the 8255 PPIs

When connecting switches, etc, to the Port lines (classed as inputs) of the PPIs, it is important to ensure that the inputs are set to a defined state at all times. Figure 6.2 gives an example.

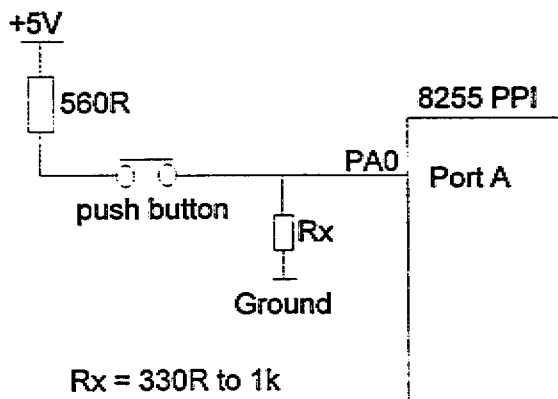


Figure 6.2: Connecting Normally Open devices to the PPI

Figure 6.2 gives an example of how to connect a push button to one of the lines of the 8255 PPI. We assume that when the Push button is closed, the Port line will go high (logic 1 = +5V). When the push button is not closed, the port line should be low. However, many Users does not connect the 'pull-down' resistor to the port line. If this is not done, the port line will be in a floating state and can hence yield either a high or a low.

Thus you must ensure that the port line is always connected which is done via a resistor network.

Chapter 7: Troubleshooting

Problem: 'Board not found' message appears on the screen when running test software.

Solution: Another I/O card might be using the same base address location as the PC 192A. Try a different base address other than the manufacturer's default base address (eg: 700h) and re-run test software DILOOP.EXE or WALKBIT.EXE found in sub directory C:\EDR\TPAS\DEMOS\. If the problem persists then try increasing the wait states on the PC 192A. If the PC 192A still does not work even after the maximum number of wait states was chosen then try a different computer with a different motherboard. If the test still fails then the PC 192A is faulty. Return the board to your distributor for repairs.

Problem: Data written to Port A, B or C (configured as Mode 0 outputs) does not set the output ports correctly.

Solution: Check the ports using the walkbit test program called WALKBIT.EXE found in EDR\TPAS\DEMOS subdirectory. Monitor the port lines of each 8255 PPI and check if the problem persists. If so, the the PPI might be faulty, replace the PPI in question with another NEC D8255AC-2 or an Intel I8255-2. You could also send the PC 192A back to your distributor for repairs.

Problem: I connected a push button to one of the port lines. When it is closed it is set to +5V (yield a logical 1) and the program reads a logical 1. However, when it is open random numbers are read by the program on port A.

Solution: When the push button is not connected, it seems that the port line is floating (not connected). You must connect a 'pulldown' resistor (experiment from 330R to 1k) to the port line in order to ensure that it is in a defined state. Also note that if a port is configured as an input then all unused lines MUST be grounded. See Section 6.2 for more details.

Warning

Any parts replaced on the PC 192A must be done by a qualified or trained technician. If you (the user) is not a trained technician then rather return the board to your distributor for repairs explaining in detail what the problem is.

If you cannot solve the problem then simply call your distributor for immediate help.

Chapter 8: Repair Service

The PC 192A is guaranteed for a period of 1 year. If the board is faulty within this period, we will gladly repair it free of charge provided that the maximum specifications was not exceeded. If any burn't tracks are seen on the PC 192A Board, warranty will be void. A repair charge will be levied in the user requires the board to be repaired.

Before sending the board to your distributor for repairs, ensure that you go through Chapter 7: TroubleShooting Hints thoroughly. If, after you have gone through this Chapter, the board still does not work, return it for repairs stating in detail what the problem is.

Our repair service centre will be available to repair our products even after the 1 year warranty. A small service fee will be levied which usually covers the cost of the components that are faulty.

Specifications

Computer Host Interface

<i>Base Address:</i>	Switchable from 0 to 1FD0h on 64 byte boundaries
<i>Bus Type:</i>	XT, AT, ISA or EISA
<i>I/O Wait States:</i>	0, 2, 4, or 8 Jumper selectable.
<i>Number of Registers:</i>	Sixty four 8-bit
<i>Word size:</i>	8 bits
<i>Word transfer Rate:</i>	10Mhz max (depends on computer and program)
<i>Interrupts:</i>	Jumper selectable from IRQ2, 3, 4, 7, 10, 11, 12, 15

Digital Inputs/Outputs

* <i>Number of lines:</i>	192 in twenty four 8-bit digital ports
* <i>Compatilty:</i>	TTL
* <i>Input Voltage:</i>	Logic Low: 0.5V to 0.8V Logic High: 2V to 5V
* <i>Output Voltage:</i>	Logic 0: 0.45V max Logic 1: 2.4V min
* <i>Output Current:</i>	Low State: 1.7mA max High State: -200 μ A min
* <i>Max Darlington drive current</i>	-4.0mA from ports types B and C only
* <i>Maximum Power per 8255</i>	1W max from all three ports per PPI

Absolute Maximum TTL Inputs

* <i>Absolute Max Input voltage:</i>	6.5V*
* <i>Absolute Min Input voltage:</i>	-0.5V*

Warning

Stresses greater than listed above may cause permanent damage to the PC 192A. This stress rating only applies to the PC 192A at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. We do not recommend exposure to absolute maximum ratings.

I/O Connector

- * *Digital I/O Connector:* 50 way male IDC
- * *Max +5V supply current at I/O connector:* 250mA from +5V typ. This also depends on the host computer power supply rating

Enviromental

- * *Operating temperature:* 0°C to 55°C
- * *Storage temperature:* -55°C to 150°C
- * *Relative humidity:* 5% to 90% non-condensing
- * *PC Board size:* 200mm x 103mm

Power Supply Requirements

- * *+5V Supply:* : 1.6A typ (excludes +5V power for User Interfacing)

Appendix A

Base Address Switch Settings

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
00	ON	ON	ON	ON	ON	ON	ON	ON	00
40	ON	ON	ON	ON	ON	ON	ON	OFF	40
80	ON	ON	ON	ON	ON	ON	OFF	ON	80
C0	ON	ON	ON	ON	ON	ON	OFF	OFF	C0
100	ON	ON	ON	ON	ON	OFF	ON	ON	100
140	ON	ON	ON	ON	ON	OFF	ON	OFF	140
180	ON	ON	ON	ON	ON	OFF	OFF	ON	180
1C0	ON	ON	ON	ON	ON	OFF	OFF	OFF	1C0
200	ON	ON	ON	ON	OFF	ON	ON	ON	200
240	ON	ON	ON	ON	OFF	ON	ON	OFF	240
280	ON	ON	ON	ON	OFF	ON	OFF	ON	280
2C0	ON	ON	ON	ON	OFF	ON	OFF	OFF	2C0
300	ON	ON	ON	ON	OFF	OFF	ON	ON	300
340	ON	ON	ON	ON	OFF	OFF	ON	OFF	340
380	ON	ON	ON	ON	OFF	OFF	OFF	ON	380
3C0	ON	ON	ON	ON	OFF	OFF	OFF	OFF	3C0
400	ON	ON	ON	OFF	ON	ON	ON	ON	400
440	ON	ON	ON	OFF	ON	ON	ON	OFF	440
480	ON	ON	ON	OFF	ON	ON	OFF	ON	480
4C0	ON	ON	ON	OFF	ON	ON	OFF	OFF	4C0
500	ON	ON	ON	OFF	ON	OFF	ON	ON	500
540	ON	ON	ON	OFF	ON	OFF	ON	OFF	540
580	ON	ON	ON	OFF	ON	OFF	OFF	ON	580
5C0	ON	ON	ON	OFF	ON	OFF	OFF	OFF	5C0
600	ON	ON	ON	OFF	OFF	ON	ON	ON	600
640	ON	ON	ON	OFF	OFF	ON	ON	OFF	640
680	ON	ON	ON	OFF	OFF	ON	OFF	ON	680
6C0	ON	ON	ON	OFF	OFF	ON	OFF	OFF	6C0
700	ON	ON	ON	OFF	OFF	OFF	ON	ON	700
740	ON	ON	ON	OFF	OFF	OFF	ON	OFF	740
780	ON	ON	ON	OFF	OFF	OFF	OFF	ON	780
7C0	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	7C0
800	ON	ON	OFF	ON	ON	ON	ON	ON	800
840	ON	ON	OFF	ON	ON	ON	ON	OFF	840
880	ON	ON	OFF	ON	ON	ON	OFF	ON	880
8C0	ON	ON	OFF	ON	ON	ON	OFF	OFF	8C0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
900	ON	ON	OFF	ON	ON	OFF	ON	ON	900
940	ON	ON	OFF	ON	ON	OFF	ON	OFF	940
980	ON	ON	OFF	ON	ON	OFF	OFF	ON	980
9C0	ON	ON	OFF	ON	ON	OFF	OFF	OFF	9C0
A00	ON	ON	OFF	ON	OFF	ON	ON	ON	A00
A40	ON	ON	OFF	ON	OFF	ON	ON	OFF	A40
A80	ON	ON	OFF	ON	OFF	ON	OFF	ON	A80
AC0	ON	ON	OFF	ON	OFF	ON	OFF	OFF	AC0
B00	ON	ON	OFF	ON	OFF	OFF	ON	ON	B00
B40	ON	ON	OFF	ON	OFF	OFF	ON	OFF	B40
B80	ON	ON	OFF	ON	OFF	OFF	OFF	ON	B80
BC0	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	BC0
C00	ON	ON	OFF	OFF	ON	ON	ON	ON	C00
C40	ON	ON	OFF	OFF	ON	ON	ON	OFF	C40
C80	ON	ON	OFF	OFF	ON	ON	OFF	ON	C80
CC0	ON	ON	OFF	OFF	ON	ON	OFF	OFF	CC0
D00	ON	ON	OFF	OFF	ON	OFF	ON	ON	D00
D40	ON	ON	OFF	OFF	ON	OFF	ON	OFF	D40
D80	ON	ON	OFF	OFF	ON	OFF	OFF	ON	D80
DC0	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	DC0
E00	ON	ON	OFF	OFF	OFF	ON	ON	ON	E00
E40	ON	ON	OFF	OFF	OFF	ON	ON	OFF	E40
E80	ON	ON	OFF	OFF	OFF	ON	OFF	ON	E80
EC0	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	EC0
F00	ON	ON	OFF	OFF	OFF	OFF	ON	ON	F00
F40	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	F40
F80	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	F80
FC0	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	FC0
1000	ON	OFF	ON	ON	ON	ON	ON	ON	1000
1040	ON	OFF	ON	ON	ON	ON	ON	OFF	1040
1080	ON	OFF	ON	ON	ON	ON	OFF	ON	1080
10C0	ON	OFF	ON	ON	ON	ON	OFF	OFF	10C0
1100	ON	OFF	ON	ON	ON	OFF	ON	ON	1100
1140	ON	OFF	ON	ON	ON	OFF	ON	OFF	1140
1180	ON	OFF	ON	ON	ON	OFF	OFF	ON	1180
11C0	ON	OFF	ON	ON	ON	OFF	OFF	OFF	11C0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
1200	ON	OFF	ON	ON	OFF	ON	ON	ON	1200
1240	ON	OFF	ON	ON	OFF	ON	ON	OFF	1240
1280	ON	OFF	ON	ON	OFF	ON	OFF	ON	1280
12C0	ON	OFF	ON	ON	OFF	ON	OFF	OFF	12C0
1300	ON	OFF	ON	ON	OFF	OFF	ON	ON	1300
1340	ON	OFF	ON	ON	OFF	OFF	ON	OFF	1340
1380	ON	OFF	ON	ON	OFF	OFF	OFF	ON	1380
13C0	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	13C0
1400	ON	OFF	ON	OFF	ON	ON	ON	ON	1400
1440	ON	OFF	ON	OFF	ON	ON	ON	OFF	1440
1480	ON	OFF	ON	OFF	ON	ON	OFF	ON	1480
14C0	ON	OFF	ON	OFF	ON	ON	OFF	OFF	14C0
1500	ON	OFF	ON	OFF	ON	OFF	ON	ON	1500
1540	ON	OFF	ON	OFF	ON	OFF	ON	OFF	1540
1580	ON	OFF	ON	OFF	ON	OFF	OFF	ON	1580
15C0	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	15C0
1600	ON	OFF	ON	OFF	OFF	ON	ON	ON	1600
1640	ON	OFF	ON	OFF	OFF	ON	ON	OFF	1640
1680	ON	OFF	ON	OFF	OFF	ON	OFF	ON	1680
16C0	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	16C0
1700	ON	OFF	ON	OFF	OFF	OFF	ON	ON	1700
1740	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	1740
1780	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	1780
17C0	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	17C0
1800	ON	OFF	OFF	ON	ON	ON	ON	ON	1800
1840	ON	OFF	OFF	ON	ON	ON	ON	OFF	1840
1880	ON	OFF	OFF	ON	ON	ON	OFF	ON	1880
18C0	ON	OFF	OFF	ON	ON	ON	OFF	OFF	18C0
1900	ON	OFF	OFF	ON	ON	OFF	ON	ON	1900
1940	ON	OFF	OFF	ON	ON	OFF	ON	OFF	1940
1980	ON	OFF	OFF	ON	ON	OFF	OFF	ON	1980
19C0	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	19C0
1A00	ON	OFF	OFF	ON	OFF	ON	ON	ON	1A00
1A40	ON	OFF	OFF	ON	OFF	ON	ON	OFF	1A40
1A80	ON	OFF	OFF	ON	OFF	ON	OFF	ON	1A80
1AC0	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	1AC0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
1B00	ON	OFF	OFF	ON	OFF	OFF	ON	ON	1B00
1B40	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	1B40
1B80	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	1B80
1BC0	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	1BC0
1C00	ON	OFF	OFF	OFF	ON	ON	ON	ON	1C00
1C40	ON	OFF	OFF	OFF	ON	ON	ON	OFF	1C40
1C80	ON	OFF	OFF	OFF	ON	ON	OFF	ON	1C80
1CC0	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	1CC0
1D00	ON	OFF	OFF	OFF	ON	OFF	ON	ON	1D00
1D40	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	1D40
1D80	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	1D80
1DC0	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	1DC0
1E00	ON	OFF	OFF	OFF	OFF	ON	ON	ON	1E00
1E40	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	1E40
1E80	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	1E80
1EC0	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	1EC0
1F00	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	1F00
1F40	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	1F40
1F80	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	1F80
1FC0	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	1FC0
2000	OFF	ON	ON	ON	ON	ON	ON	ON	2000
2040	OFF	ON	ON	ON	ON	ON	ON	OFF	2040
2080	OFF	ON	ON	ON	ON	ON	OFF	ON	2080
20C0	OFF	ON	ON	ON	ON	ON	OFF	OFF	20C0
2100	OFF	ON	ON	ON	ON	OFF	ON	ON	2100
2140	OFF	ON	ON	ON	ON	OFF	ON	OFF	2140
2180	OFF	ON	ON	ON	ON	OFF	OFF	ON	2180
21C0	OFF	ON	ON	ON	ON	OFF	OFF	OFF	21C0
2200	OFF	ON	ON	ON	OFF	ON	ON	ON	2200
2240	OFF	ON	ON	ON	OFF	ON	ON	OFF	2240
2280	OFF	ON	ON	ON	OFF	ON	OFF	ON	2280
22C0	OFF	ON	ON	ON	OFF	ON	OFF	OFF	22C0
2300	OFF	ON	ON	ON	OFF	OFF	ON	ON	2300
2340	OFF	ON	ON	ON	OFF	OFF	ON	OFF	2340
2380	OFF	ON	ON	ON	OFF	OFF	OFF	ON	2380
23C0	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	23C0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
2400	OFF	ON	ON	OFF	ON	ON	ON	ON	2400
2440	OFF	ON	ON	OFF	ON	ON	ON	OFF	2440
2480	OFF	ON	ON	OFF	ON	ON	OFF	ON	2480
24C0	OFF	ON	ON	OFF	ON	ON	OFF	OFF	24C0
2500	OFF	ON	ON	OFF	ON	OFF	ON	ON	2500
2540	OFF	ON	ON	OFF	ON	OFF	ON	OFF	2540
2580	OFF	ON	ON	OFF	ON	OFF	OFF	ON	2580
25C0	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	25C0
2600	OFF	ON	ON	OFF	OFF	ON	ON	ON	2600
2640	OFF	ON	ON	OFF	OFF	ON	ON	OFF	2640
2680	OFF	ON	ON	OFF	OFF	ON	OFF	ON	2680
26C0	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	26C0
2700	OFF	ON	ON	OFF	OFF	OFF	ON	ON	2700
2740	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	2740
2780	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	2780
27C0	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	27C0
2800	OFF	ON	OFF	ON	ON	ON	ON	ON	2800
2840	OFF	ON	OFF	ON	ON	ON	ON	OFF	2840
2880	OFF	ON	OFF	ON	ON	ON	OFF	ON	2880
28C0	OFF	ON	OFF	ON	ON	ON	OFF	OFF	28C0
2900	OFF	ON	OFF	ON	ON	OFF	ON	ON	2900
2940	OFF	ON	OFF	ON	ON	OFF	ON	OFF	2940
2980	OFF	ON	OFF	ON	ON	OFF	OFF	ON	2980
29C0	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	29C0
2A00	OFF	ON	OFF	ON	OFF	ON	ON	ON	2A00
2A40	OFF	ON	OFF	ON	OFF	ON	ON	OFF	2A40
2A80	OFF	ON	OFF	ON	OFF	ON	OFF	ON	2A80
2AC0	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	2AC0
2B00	OFF	ON	OFF	ON	OFF	OFF	ON	ON	2B00
2B40	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	2B40
2B80	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	2B80
2BC0	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	2BC0
2C00	OFF	ON	OFF	OFF	ON	ON	ON	ON	2C00
2C40	OFF	ON	OFF	OFF	ON	ON	ON	OFF	2C40
2C80	OFF	ON	OFF	OFF	ON	ON	OFF	ON	2C80
2CC0	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	2CC0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
2D00	OFF	ON	OFF	OFF	ON	OFF	ON	ON	2D00
2D40	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	2D40
2D80	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	2D80
2DC0	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	2DC0
2E00	OFF	ON	OFF	OFF	OFF	ON	ON	ON	2E00
2E40	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	2E40
2E80	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	2E80
2EC0	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	2EC0
2F00	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	2F00
2F40	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	2F40
2F80	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	2F80
2FC0	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	2FC0
3000	OFF	OFF	ON	ON	ON	ON	ON	ON	3000
3040	OFF	OFF	ON	ON	ON	ON	ON	OFF	3040
3080	OFF	OFF	ON	ON	ON	ON	OFF	ON	3080
30C0	OFF	OFF	ON	ON	ON	ON	OFF	OFF	30C0
3100	OFF	OFF	ON	ON	ON	OFF	ON	ON	3100
3140	OFF	OFF	ON	ON	ON	OFF	ON	OFF	3140
3180	OFF	OFF	ON	ON	ON	OFF	OFF	ON	3180
31C0	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	31C0
3200	OFF	OFF	ON	ON	OFF	ON	ON	ON	3200
3240	OFF	OFF	ON	ON	OFF	ON	ON	OFF	3240
3280	OFF	OFF	ON	ON	OFF	ON	OFF	ON	3280
32C0	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	32C0
3300	OFF	OFF	ON	ON	OFF	OFF	ON	ON	3300
3340	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	3340
3380	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	3380
33C0	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	33C0
3400	OFF	OFF	ON	OFF	ON	ON	ON	ON	3400
3440	OFF	OFF	ON	OFF	ON	ON	ON	OFF	3440
3480	OFF	OFF	ON	OFF	ON	ON	OFF	ON	3480
34C0	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	34C0
3500	OFF	OFF	ON	OFF	ON	OFF	ON	ON	3500
3540	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	3540
3580	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	3580
35C0	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	35C0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
3600	OFF	OFF	ON	OFF	OFF	ON	ON	ON	3600
3640	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	3640
3680	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	3680
36C0	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	36C0
3700	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	3700
3740	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	3740
3780	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	3780
37C0	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	37C0
3800	OFF	OFF	OFF	ON	ON	ON	ON	ON	3800
3840	OFF	OFF	OFF	ON	ON	ON	ON	OFF	3840
3880	OFF	OFF	OFF	ON	ON	ON	OFF	ON	3880
38C0	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	38C0
3900	OFF	OFF	OFF	ON	ON	OFF	ON	ON	3900
3940	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	3940
3980	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	3980
39C0	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	39C0
3A00	OFF	OFF	OFF	ON	OFF	ON	ON	ON	3A00
3A40	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	3A40
3A80	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	3A80
3AC0	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	3AC0
3B00	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	3B00
3B40	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	3B40
3B80	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	3B80
3BC0	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	3BC0
3C00	OFF	OFF	OFF	OFF	ON	ON	ON	ON	3C00
3C40	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	3C40
3C80	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	3C80
3CC0	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	3CC0
3D00	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	3D00
3D40	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	3D40
3D80	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	3D80
3DC0	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	3DC0
3E00	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	3E00
3E40	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	3E40
3E80	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	3E80
3EC0	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	3EC0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
3F00	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	3F00
3F40	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	3F40
3F80	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	3F80
3FC0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3FC0

Appendix B

DESIGNERS: R. CANNING

DOC NO: PC192A
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EAGLE TECHNOLOGY
TITLE: PC-192A ENHANCED I/O CARD
TOP SILK

