PC-14
dual 8255 I/O
card

User manual

PC-14 Engineering Guide

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1. The PC-14 Digital Input/Output Card

The PC-14 digital Input/Output (I/O) card provides an easy interface for digital signals to the IBM-PC or compatible. It includes 48 programmable I/O lines plus 3 counter/timers for counting events or timing the length of an event.

To provide the most programmability and the most economical solution the PC-14 is built using two 8255 Programmable Peripheral Interface (PPI) chips and an 8253 Counter/Timer circuit. The operation of these devices and the addressability and the external connections are described in the following chapters.

2. Port Addresses

The PC-14 uses one of two possible address spaces in the I/O bus of the IBM-PC. The two address spaces are 1B0-1BF and 1F0-1FF selectable by switches SW4 and SW5. If SW4 is on then addresses 1F0-1FF are used. If switch SW5 is on then addresses 1B0-1BF are used.

The following table outlines the use of each address location. For operation of the PPI see the section titled "Using the Parallel Peripheral Interface (PPI)" on page 2. For operation of the 8253 Counter/Timer see the section titled "Using the Onboard Timer (8253)" on page 6.

Port Address	Function
1B0 or 1F0	Parallel I/O 8255 Number 1 Port A
1B1 or 1F1	Parallel I/O 8255 Number 1 Port B
1B2 or 1F2	Parallel I/O 8255 Number 1 Port C
1B3 or 1F3	Parallel I/O 8255 Number 1 Control Port
1B4 or 1F4	Parallel I/O 8255 Number 2 Port A
1B5 or 1F5	Parallel I/O 8255 Number 2 Port B
1B6 or 1F6	Parallel I/O 8255 Number 2 Port C
1B7 or 1F7	Parallel I/O 8255 Number 2 Control Port
1B8 or 1F8	8253 Counter/Timer 0
1B9 or 1F9	8253 Counter/Timer 1
1BA or 1FA	8253 Counter/Timer 2
1BB or 1FB	8253 Counter/Timer Control

3. Using the Parallel Peripheral Interface (PPI)

The 8255 Programmable Peripheral Interface (PPI) is a multi purpose parallel I/O support chip. It supplies 3 parallel ports which can be programmed independently as either input or output. The 3 ports are named Port A, Port B, and Port C. Port C can be programmed as either input, output or support for Ports A and B.

The PPI supports three modes of operation; simple input or output with three ports, Strobed input or output with two ports or one port of bi-directional I/O with one port of simple I/O. The following is an explanation of the operation of these three modes. For further information on the 8255 PPI refer to Intel Microsystems Component Handbook or other manufacturers specifications.

3.1. PPI Mode 0: Simple I/O

Using the simple I/O mode the three ports can be independently programmed as input or output, and Port C can be nibble (4 bits) programmed as input or output. This is referred to as Mode 0.

3.2. PPI Mode 1: Strobed I/O

Mode 1 is the strobed I/O mode. In this mode Port C supplies the strobe signals as follows:

3.2.1. PPI Mode 1: Strobed Input

Signal	Port A	Port B
Strobe (STB)	PC4	PC2
Input Buffer Full (IBF)	PC5	PC1

PC6 and PC7 can be used as simple I/O bits

Using the input mode, STB going low will write data into the input buffer if it is empty. When the data is written the PPI will output IBF high and IBF will remain high until the PC reads the data from that port.

3.2.2. PPI Mode 1: Strobed Output

Signal	Port A	Port B
Output Buffer Full (OBF)	PC7	PC1
Acknowledge (ACK)	PC6	PC2

PC4 and PC5 can be used as simple I/O bits

Using the output mode, when data is written into the PPI by the PC the PPI will output OBF low, indicating data is ready to be read on the port. The OBF line will not go inactive until the ACK line is pulled low and returned high by external circuitry.

3.3. PPI Mode 2: Bi-Directional I/O

Signal	Port A
Output Buffer Full (OBF)	PC7
Acknowledge (ACK)	PC6
Strobe (STB)	PC4
Input Buffer Full	PC5

PC0, PC1, and PC2 can be used as simple I/O bits

When the PC writes data to the PPI in this mode the PPI sets OBF low but the data does not become available on the Port A bus until ACK is input low. The Port A bus remains in input mode unless ACK is input low. When STB is input low the PPI reads data from the Port A bus and outputs IBF high.

4. Programming the PPI

The PPI is controlled via the control port which is located at 1B3H or 1F3H for PPI number 1 and 1B7 or 1F7 for PPI number 2 depending on the position of SW4 and SW5.

The tables on pages 4 and 5 show the bit definitions for the PPI control ports in two modes depending on the state of D_7. The table on page 4 shows the definitions for the control port when bit $D_7 = 1$ (Mode definitions). The table on page 5 shows the bit definitions when bit $D_7 = 0$ (Set/Reset Format).

The mode definition byte allows the setting of all three port modes with one command.

The Set/Reset Format allows the setting or resetting of any single bit on port C that is in output mode.

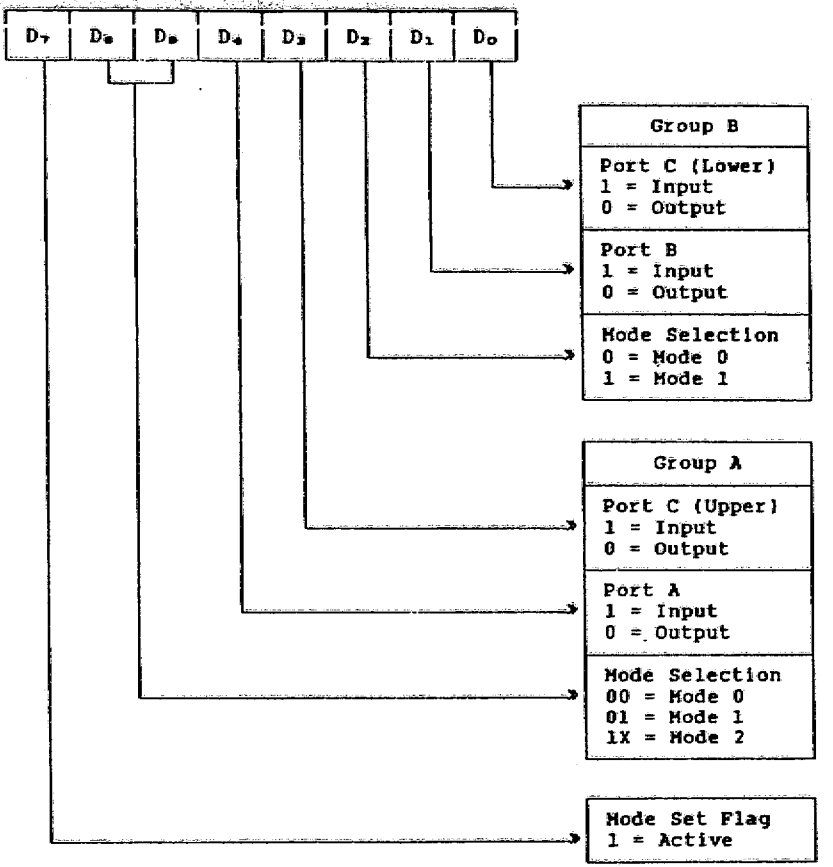


Figure 1. PPI Mode Register Bit Definitions

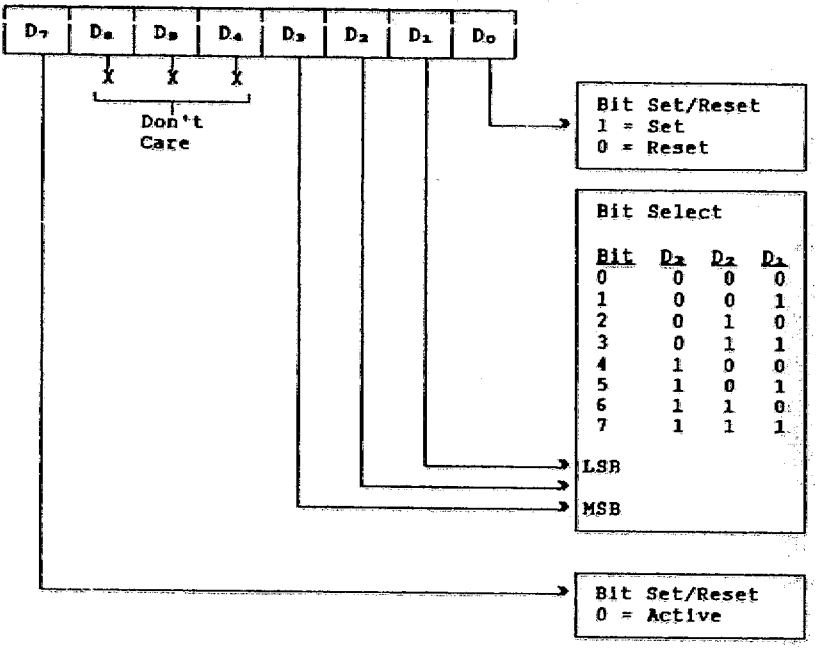


Figure 2. PPI Control Port Definitions (Bit Set/Reset Format)

5. Using the Onboard Timer (8253)

The PC-14 includes an on board 8253 Counter/Timer circuit that is useful for the the following applications:

* Programmable Rate Generator
* Digital One Shot
* Event Counter
* Binary Rate Multiplier

The 8253 is a programmable interval Counter/Timer. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports by the system software.

Each timer has two inputs and one output. The inputs are named; CLK IN and GATE. The output is named CLK OUT.

The GATE input "gates" the CLK IN signal. When GATE is High clock pulses are allowed in to the timer. When GATE is input Low no inputs are allowed in to the timer.

The inputs to the 8253 have two possible sources; an external connection or the CPU system clock from the IBM-PC bus divided by 2. On a standard PC with a system clock speed of 4.77 MHZ this frequency is 2.38633 MHZ.

Note: The clock inputs of the 8253 timer are rated at 2.6 MHZ therefor the timer cannot be used with internal clocking in a system with a system clock speed of greater than 5.2 MHZ which includes most "turbo" models.

For external connections and switch settings see the appendices.

6. Programming The Onboard Timer (8253)

The 8253 has four I/O ports. The first three are timer specific for loading/reading the counter values and the last is a full chip control port.

The operation of each control port bit is diagrammed in the figure on page 14 .

The following sections describe the operation of the timer control port.

6.1. Counter Selection Bits

There are four sections of the control port each with its own function. The first section is the "Select Counter" or "SC" section. These two bits define the counter that this control word is to effect.

6.2. Read/Load Mode Selection Bits

The next two bits define the operation of the specific timer read/load port. Each timer has a sixteen bit counter that can be read or loaded one byte at a time. The "RL" bits control the operation of the reading or loading order of the counters. When RL1 = 1 and RL0 = 1, the next operation should be to read or load two bytes into the selected register's data port. Either byte can be loaded by itself using one of the other modes.

The latching mode when selected (RL1 = 0, RL0 = 0) takes the current counter contents and writes them to a latch that can be read on a subsequent read operation. This allows the counter to be read one byte at a time while the timer is running.

Note: A Read/Load command must be completed by reading or loading data into or from the appropriate timer's data port. If a two byte operation is selected, both bytes must be transferred before any other commands can be given.

6.3. 8253 Modes of Operation

The 8253 has six modes of operation. The six modes are; Mode 0: Interrupt on terminal count, Mode 1: Programmable One-Shot, Mode 2: Rate generator, Mode 3: Square wave generator, Mode 4: Software triggered strobe, and Mode 5: Hardware Triggered Strobe.

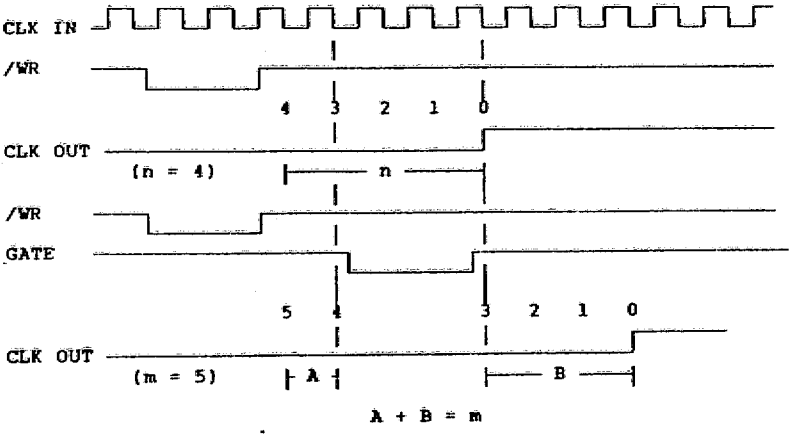
The operation of each mode is described in the following sections.

Note: In the mode descriptions the Trigger input is the same as the GATE input.

6.3.1. Mode 0: Interrupt on Terminal Count

This mode initially sets Clock Out low and starts the counter counting clock pulses from Clock In after the counter has been loaded with the second byte. Once terminal count is reached the output of the timer goes high until the counter is loaded with a new value.

This mode is useful for counting items. If a sensor is connected to the CLK IN line the CLK OUT line will go High when a programmed number of items is counted.

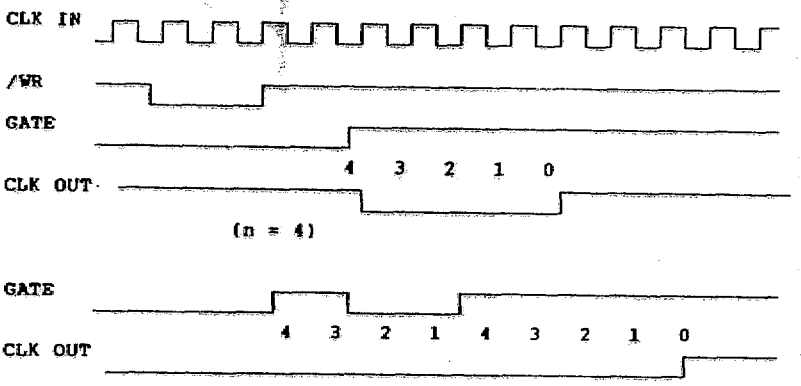


6.3.2. Mode 1: Programmable One-Shot

The CLK OUT line will go Low on the count following the rising edge of the GATE input.

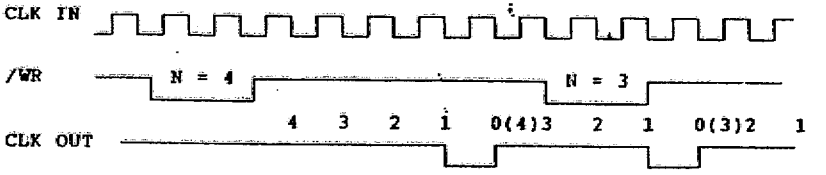
CLK OUT will go High on the terminal count. If a new count value is loaded while the output is Low it will not effect the duration of the one-shot pulse until the next trigger. The current count can be read at any time without effecting the one-shot pulse.

The one-shot is retriggerable. If a trigger comes while a one-shot pulse is being counted, the count will be started over.



6.3.3. Mode 2: Rate Generator

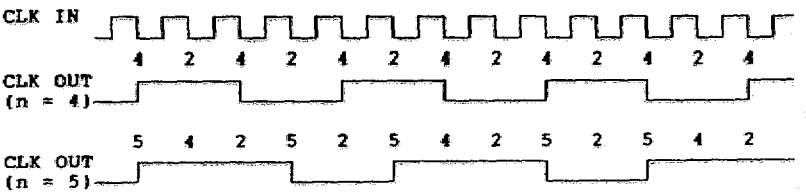
This mode is a divide by N counter. Once the counter is loaded the counter begins to count down until terminal count when the output is set low for one period of the input clock and the counter is automatically reloaded and the count is started again.



6.3.4. Mode 3: Square Wave Generator

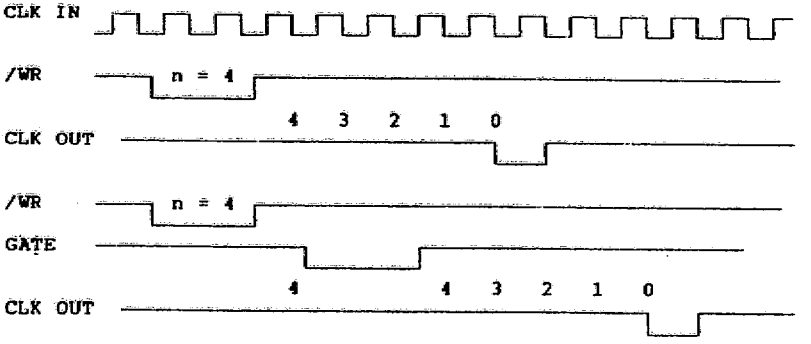
This mode is similar to mode 2 except that the output remains High until one half of the count has been completed (for even numbers) and go Low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the the output is changed and the counter is reloaded with the same count or a new one that has been loaded since the last terminal count.

If the count is odd and the output is High, the first clock pulse (after the count is loaded) decrements the count by 1 and other clock pulses decrement the count by two. After timeout, the output goes Low and the full count is reloaded. The first clock pulse following reload decrements the counter by 3 and following pulses decrement the counter by 2. Then the process is repeated. Therefore if the count is odd, the output will be high for (N + 1) / 2 pulses and Low for (N - 1) / 2 pulses.



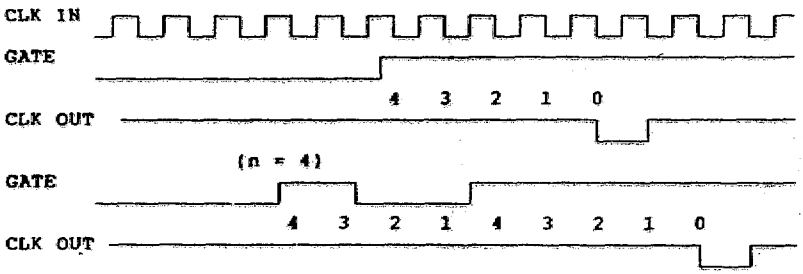
6.3.5. Mode 4: Software Triggered Strobe

After the mode is set the output will be high. When the count is loaded the count will begin. When terminal count is reached, the output will go low for one clock period.



6.3.6. Mode 5: Hardware Triggered Strobe

The counter will start counting after the rising edge of the trigger input and will go Low for one clock period when the terminal count is reached. The counter is retriggerable the same as in mode 1.



6.4. Binary or Binary Coded Decimal (BCD) Counters

The last bit, bit 0, controls the type of counters used. If this bit is 0, the counters count in binary (four bits count up to 16). If this bit is 1, the counters are Binary Coded Decimal (BCD). In the BCD mode a four bit counter will only count up to 10 before incrementing the next four bit counter.

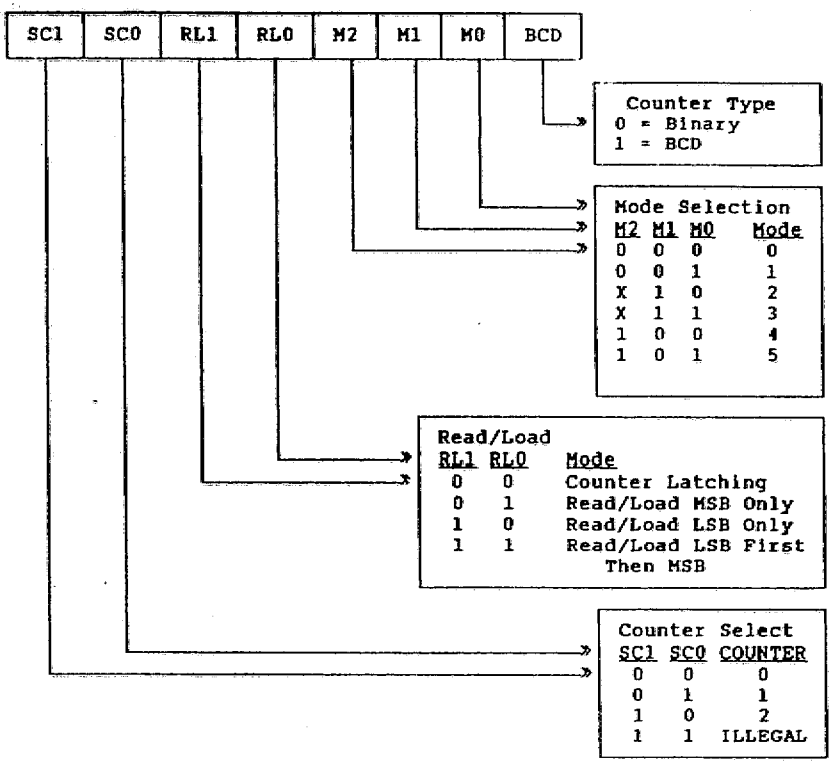


Figure 3. Timer Control Port Bit Definitions

7. The PC-14 Software

The PC-14 board is shipped complete with a test software package. The diskette contains two files; "IO8255.BAS" and "IO8255-2.BAS". Both files are BASIC programs.

Both programs set up all of the timers to output a square waves (Mode 3). Timer 0 is a divide by 2 counter, timer 1 is a divide by 50 counter and timer 2 is a divide by 100 counter.

The 8255's are set up in IO8255.BAS to output all of the bits high and then all of the bits low continuously.

In IO8255-2.BAS the 8255's output binary numbers from 0 to 255 continuously.

The provided software is meant to provide a means of easily testing the board and also to provide software examples for programming techniques.

Appendix A. PC-14 External Connections

The external connectors on the PC-14 are 2-40 pin dual row pin connectors. These connectors were chosen due to the high number of connections to be made and the ease of cable making for interconnection to the outside world. The connections are as follows:

CN1 (Port 1)				CN2 (Port 2)			
Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	GND	21	PC6	1	GND	21	PC7
2	GND	22	PC7	2	GND	22	PC6
3	N/C	23	PC4	3	N/C	23	PC5
4	PA3	24	PC5	4	N/C	24	PC4
5	PA1	25	PC1	5	N/C	25	PC0
6	PA2	26	PC0	6	N/C	26	PC1
7	CLKIN_0	27	PB7	7	N/C	27	PC2
8	PA0	28	PC2	8	N/C	28	PB7
9	GATE_0	29	PB6	9	N/C	29	PC3
10	CLKOUT_0	30	PC3	10	N/C	30	PB6
11	CLKOUT_2	31	PB5	11	N/C	31	PB0
12	CLKIN_2	32	PB0	12	N/C	32	PB5
13	CLKIN_1	33	PB4	13	PA0	33	PB1
14	GATE_2	34	PB1	14	PA1	34	PB4
15	CLKOUT_1	35	PB3	15	PA2	35	PB2
16	GATE_1	36	PB2	16	PA3	36	PB3
17	PA5	37	+5V	17	PA4	37	+5V
18	PA4	38	-5V	18	PA5	38	-5V
19	PA7	39	+12V	19	PA6	39	+12V
20	PA6	40	-12V	20	PA7	40	-12V

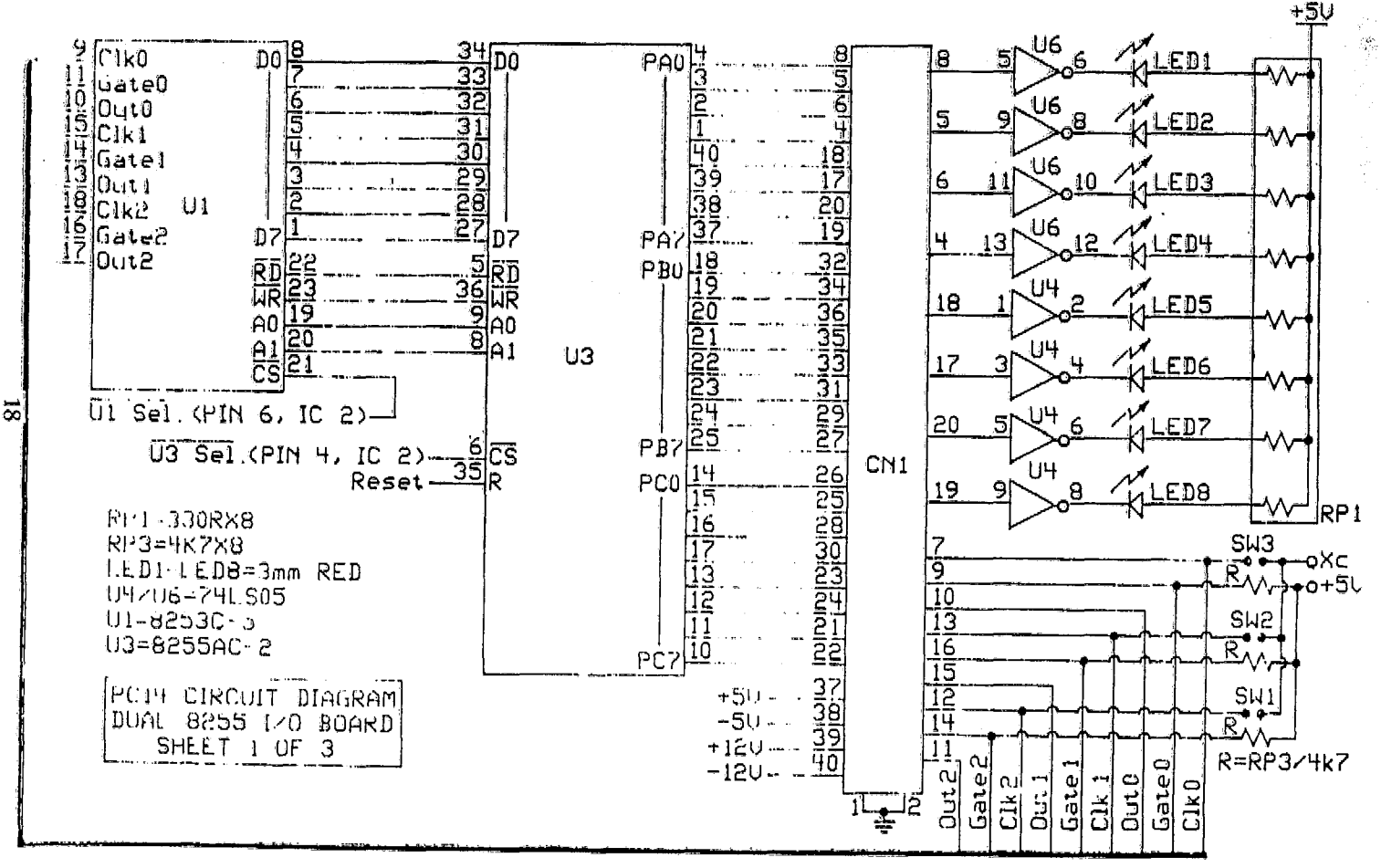
Appendix B. PC-14 Switch Settings

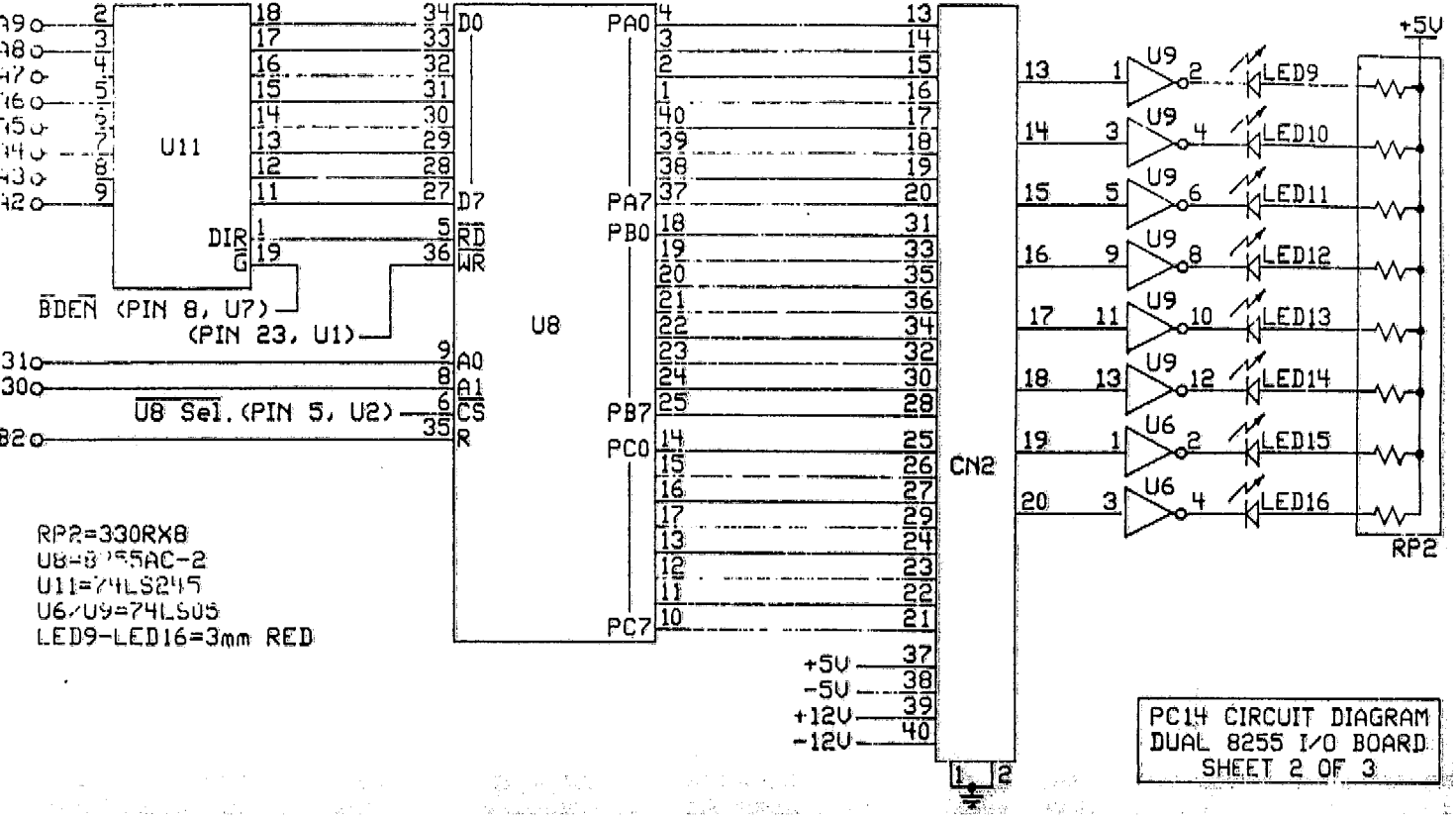
The PC-14 has one switch block that has 8 switches. Only the first five are used. The switches are defined as follows:

Switch	ON	OFF
SW3	Counter 0 Internal Clock (2.3 MHZ)	Counter 0 External Clock
SW2	Counter 1 Internal Clock (2.3 MHZ)	Counter 1 External Clock
SW1	Counter 2 Internal Clock (2.3 MHZ)	Counter 2 External Clock

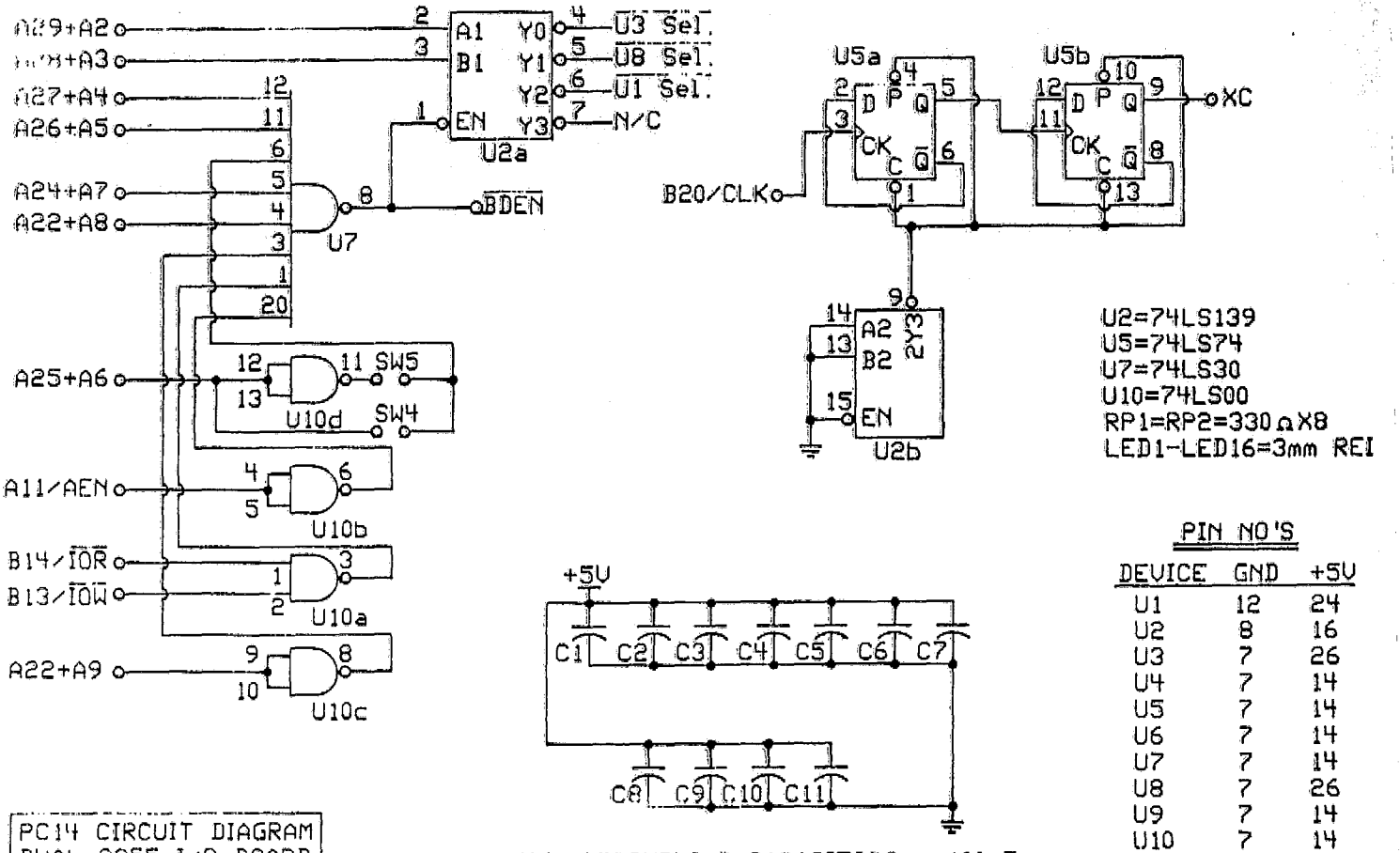
SW4 OFF and SW5 on — Select Addresses 1B0-1BF
SW4 ON and SW5 off — Select Addresses 1F0-1FF

SW6-SW8 Not Used


Clk0
Gate0
Out0
Clk1
Gate1
Out1
Clk2
Gate2
Out2
U1
D0
D7
RD
WR
A0
A1
CS
U1 Sel.(PIN 6, IC 2)
U3
U3 Sel.(PIN 4, IC 2)
Reset
PA0
PA7
PB0
PB7
PC0
PC7
+5V
-5V
+12V
-12V
CN1
U6
U4
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
RP1
SW3
SW2
SW1
R
XC
+5V
R=RP3/4k7
RP1-330RX8
RP3=4K7X8
LED1-LED8=3mm RED
U4/U6=74LS05
U1-8253C-5
U3=8255AC-2
PC14 CIRCUIT DIAGRAM
DUAL 8255 I/O BOARD
SHEET 1 OF 3



PC14 CIRCUIT DIAGRAM
DUAL 8255 I/O BOARD
SHEET 2 OF 3



PC14 CIRCUIT DIAGRAM
DUAL 8255 I/O BOARD
SHEET 3 OF 3

PIN NO'S

DEVICE	GND	+5V
U1	12	24
U2	8	16
U3	7	26
U4	7	14
U5	7	14
U6	7	14
U7	7	14
U8	7	26
U9	7	14
U10	7	14
U11	10	20

PARTS LIST - PC-14 DUAL 8255 I/O CARD

Integrated circuits:

IC1	8253C-5
IC2	74LS139
IC3	8255AC-5
IC4	74LS05
IC5	74LS74
IC6	74LS05
IC7	74LS30
IC8	8255AC-5
IC9	74LS05
IC10	74LS00
IC11	74LS245

Resistors:

RP1/RP2	330 ohm D.I.L. (16-pin)
RP3	4K7 D.I.L. (16-pin)

Capacitors:

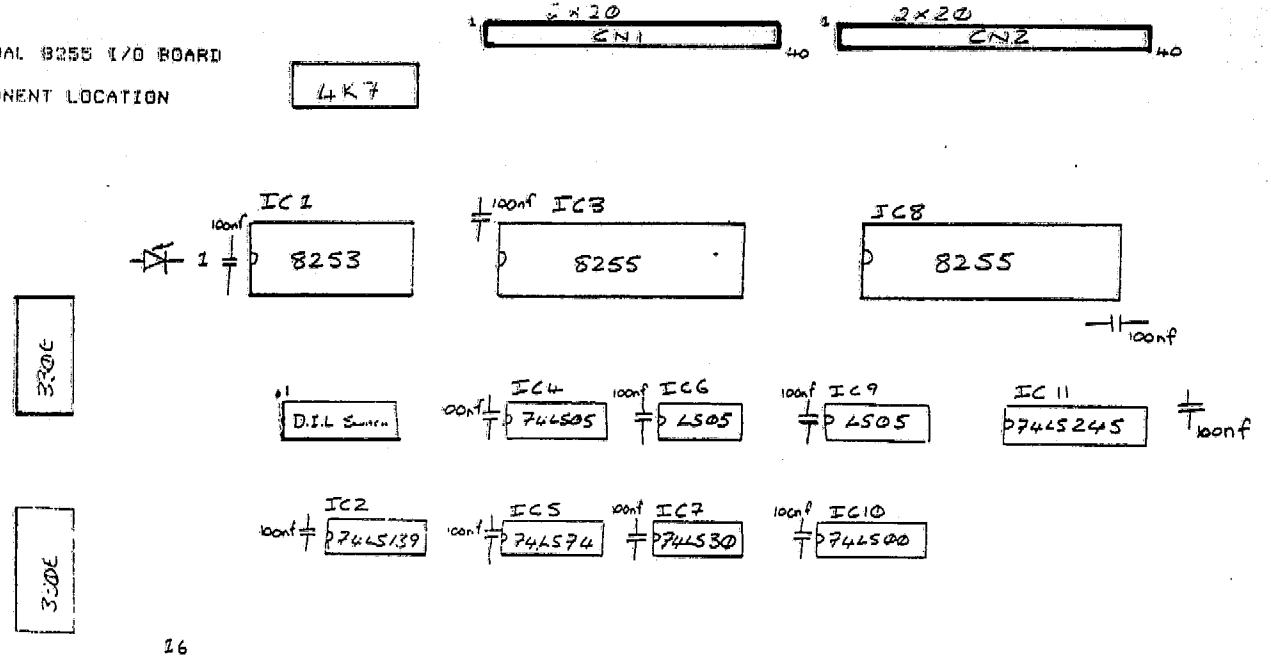
C1/C11	100nF ceramic

LEDs:

LED1/LED16	3mm red

Z80 DUAL 8255 I/O BOARD

COMPONENT LOCATION



16

MULTIADDRESS PC-14

To avoid conflict between other expansion cards and the PC-14, a new version of the PC-14 has been introduced. Base addresses can be selected between 010H and 3F0H, by setting the DIP switches to suit before installing the card.

There are also two jumpers, W1 and W2, to be set on the new PC-14. When using a PC with a clock speed of less than 8MHz, W1 is in and W2 is out. This will give a clock speed to the 8253 of the PC clock speed divided by 4.

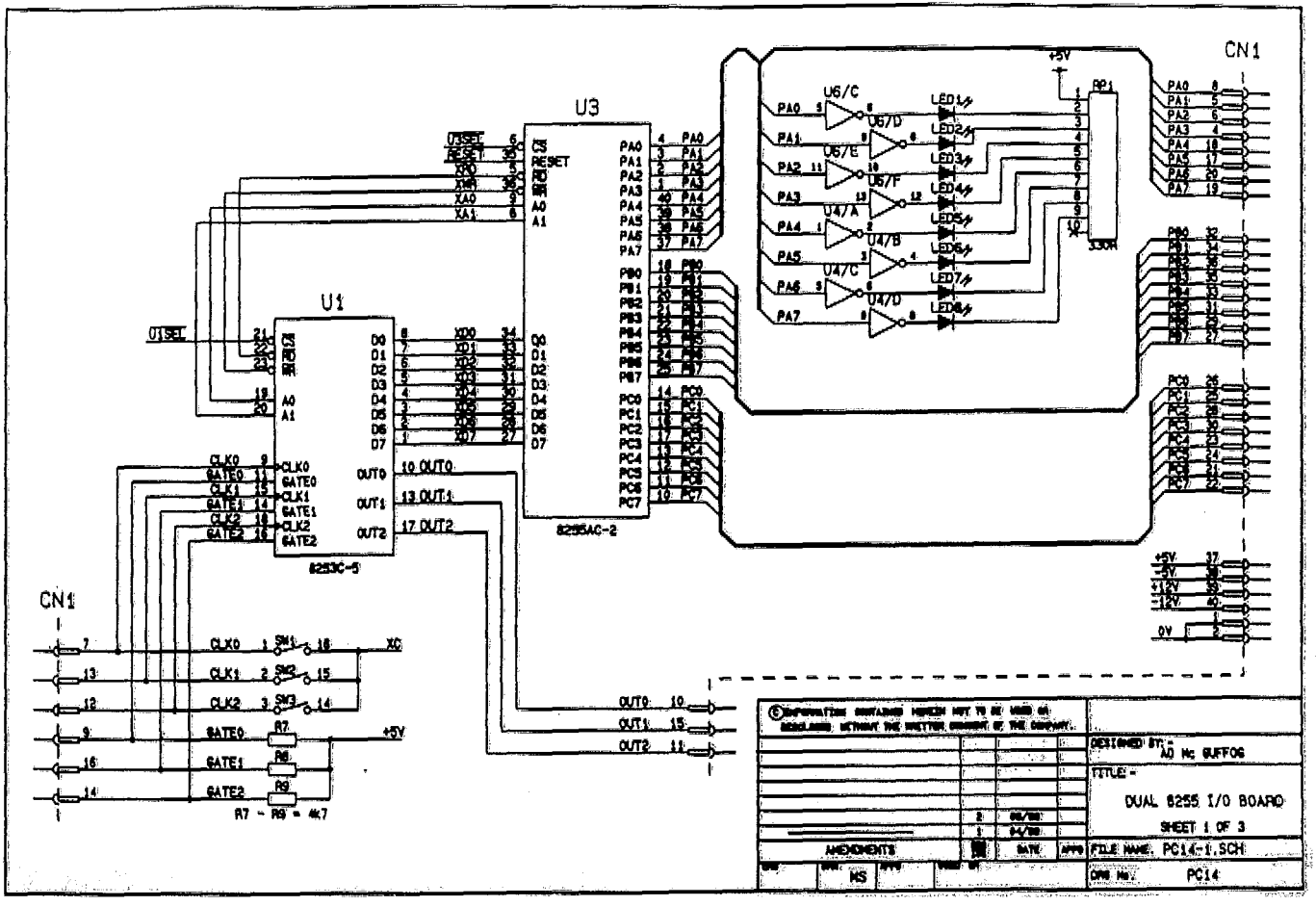
If you are using a PC with a greater than 8MHz clock speed, W1 should be out and W2 in. The clock to the 8253 will then be the PC clock divided by 64.

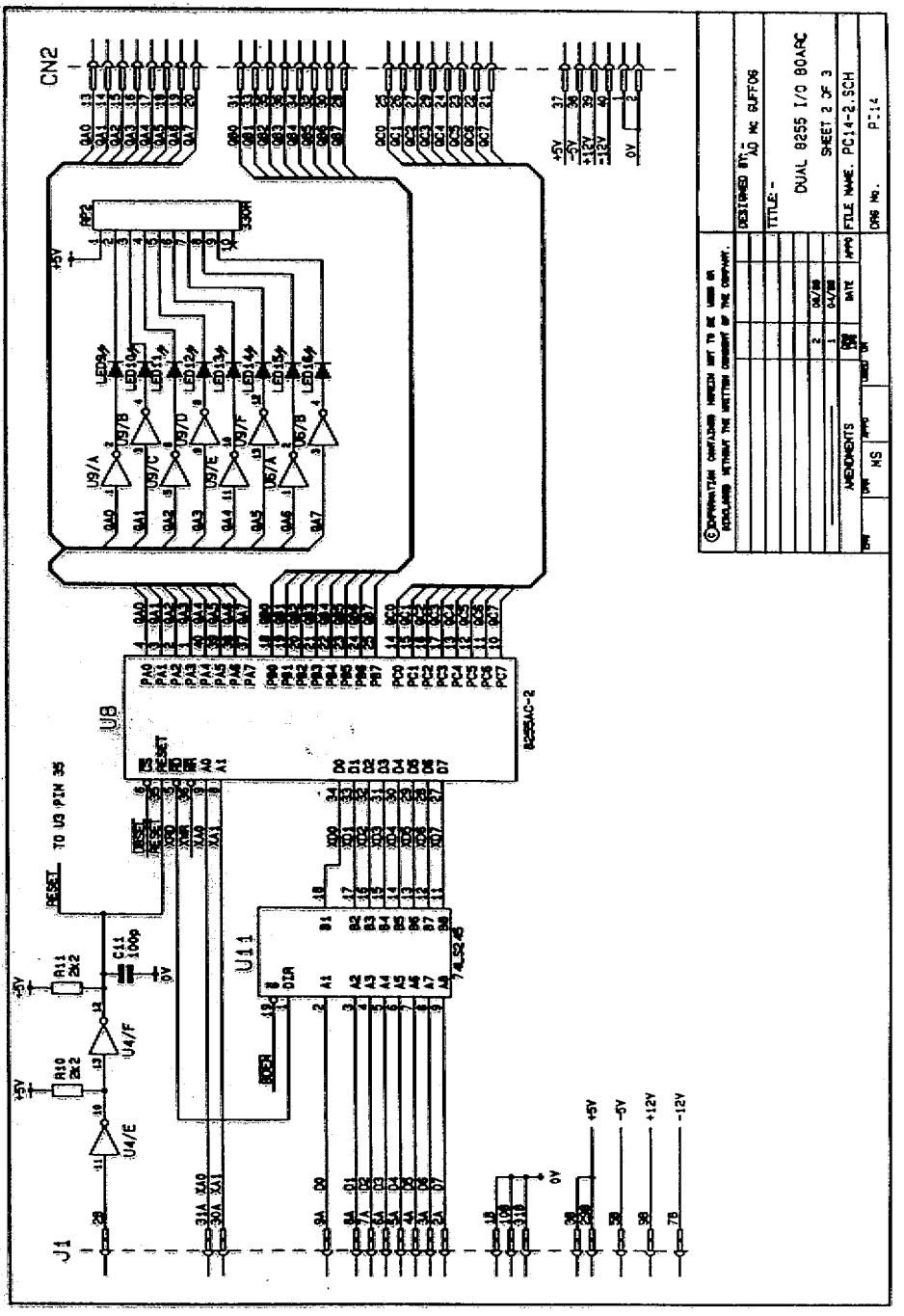
Base address switch settings and circuit diagrams for the new PC-14 follow this page.

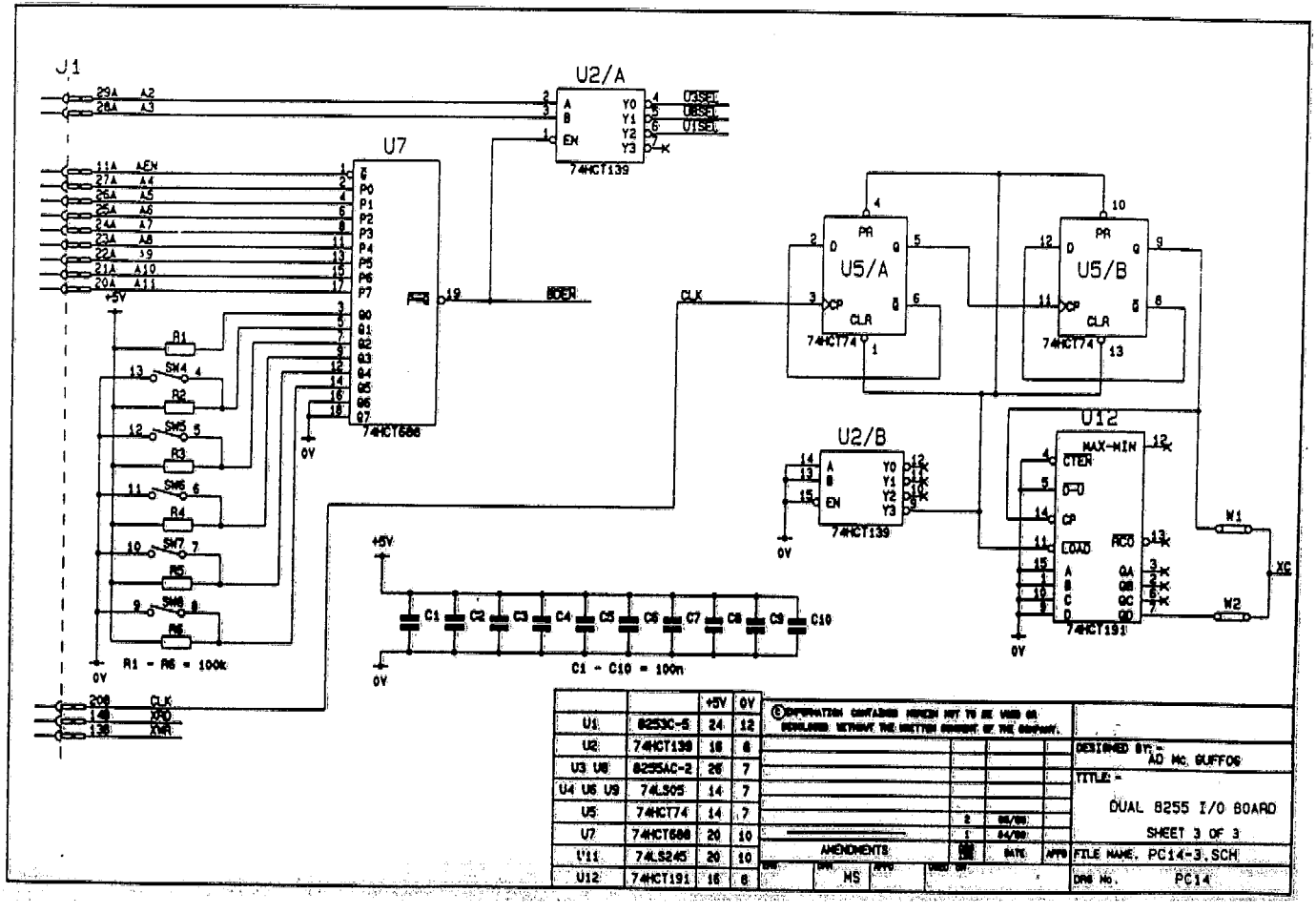
PC-14 switch settings

New switch settings for base address are as follows :

Base address	SW4	SW5	SW6	SW7	SW8
010H	On	On	On	On	On
030H	Off	On	On	On	On
050H	On	Off	On	On	On
070H	Off	Off	On	On	On
090H	On	On	Off	On	On
0B0H	Off	On	Off	On	On
0D0H	On	Off	Off	On	On
0F0H	Off	Off	Off	On	On
110H	On	On	On	Off	On
130H	Off	On	On	Off	On
150H	On	Off	On	Off	On
170H	Off	Off	On	Off	On
190H	On	On	Off	Off	On
1B0H	Off	On	Off	Off	On
1D0H	On	Off	Off	Off	On
1F0H	Off	Off	Off	Off	On
210H	On	On	On	On	Off
230H	Off	On	On	On	Off
250H	On	Off	On	On	Off
270H	Off	Off	On	On	Off
290H	On	On	Off	On	Off
2B0H	Off	On	Off	On	Off
2D0H	On	Off	Off	On	Off
2F0H	Off	Off	Off	On	Off
310H	On	On	On	Off	Off
330H	Off	On	On	Off	Off
350H	On	Off	On	Off	Off
370H	Off	Off	On	Off	Off
390H	On	On	Off	Off	Off
3B0H	Off	On	Off	Off	Off
3D0H	On	Off	Off	Off	Off
3F0H	Off	Off	Off	Off	Off


U3
8255AC-2
U1
8253C-5
CN1
CN1
RP1
330R
U6/C
U6/D
U6/E
U6/F
U4/A
U4/B
U4/C
U4/D
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
+5V
0V
-5V
+12V
-12V
R7 - R9 = 4k7
DUAL 8255 I/O BOARD
SHEET 1 OF 3
PC14-1.SCH
PC14


CN2
U8
U11
U4/E
U4/F
J1
TO U3 PIN 35
DUAL 8255 I/O BOARD
SHEET 2 OF 3
FILE NAME: PC14-2.SCH
DRG No. P:14



		+5V	0V
U1	8253C-5	24	12
U2	74HCT139	16	8
U3 U8	8255AC-2	26	7
U4 U6 U9	74LS05	14	7
U5	74HCT74	14	7
U7	74HCT688	20	10
U11	74LS245	20	10
U12	74HCT191	16	8

AMENDMENTS			DATE	APP'D
	2		06/88	
	1		04/88	

DESIGNED BY:- AD Mc GUFFOG

TITLE:- DUAL 8255 I/O BOARD

SHEET 3 OF 3

FILE NAME. PC14-3.SCH

DRG No. PC14

DRN MS