User manual for

PC-126

High Performance Analog I/O Boards for IBM PC, PC/XT, PC/AT, PS/2 Model 25 and 30 and compatible Computer Systems.

Third edition

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PC-126 Quick Start

As supplied by the factory, your PC-126 is configured such that it is ready to run in virtually all PC, PC/XT, PC/AT, PS/2 and compatible computers.

Only if you have other engineering cards, or some LAN and tape backup systems installed will you need to reconfigure the PC-126. Reconfiguring the PC-126 is discused in chapter 3 of the "User Manual"

Assuming you haven't changed any of the factory installed jumpers on the PC-126 and have a PC with a graphics adapter (Hercules, CGA, EGA, VGA etc), you can get started quickly:

If you have changed the PC-126 DIP switch settings, don't despair; default settings are described in chapter 3 of the user manual.

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i. Install the PC-126 in your computer. (Chapter 3 provides brief instructions on this, but if you are not sure, it is better to get someone who is qualified to do this).

ii. Connect up a voltage source to analog input channel 0. (You can also loop the analog outputs back to the inputs). The pin-out of the PC-126 connector is shown in figure 4.1 of the user manual.

Note

Remember not to apply more than +-12 V to the PC-126 analog inputs, and to ground unused inputs.

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iii) Power up your computer and wait for the DOS prompt. Insert the supplied PC 30 driver disk and type: A: <enter>
Install a: c:

The program files will then be installed on your harddisk in the PC30 subdirectory.

iv) Go to the PC30\WAVEVIEW subdir and type: WV <enter>

v) Waveview will then start up and display a message relating to your computers extended / expanded memory, etc. Press any key to clear the message.

v) Go to the Card Type function in the Card Menu to check if the PC 126 was detected. If no PC 126 Board was found, you need to reconfigure the PC 126. See chapter 3 of the User Manual.

vi) Press F7. WaveView will then sample 10000 samples at 10kHz and display the results. That's it; your PC 126 is up and running!

vii) To sample other channels, change the sampling frequency, etc, use the AD in Menu. WaveView also allows you to store or plot data, perform FFTs, set the DACs, set the digital I/O lines, etc. Use WaveView comprehensive Help Menu for more details.

NOTE: Previous users of PC126 boards should note that on revision III boards, the power supply outputs on the IDC connector are ±12V (125mA max) not ±15V (0.5mA max) as was previously the case.

Table of Contents

Preface

This manual is written for users of the PC-126 and PC-126A series of analog I/O boards. It provides all information necessary to successfully program and operate all boards in the series.

The companion manual to this, "User Manual for PC-30 Driver Software", describes the use of the supplied driver software.

This manual assumes:

- That you have a basic knowledge of electronic circuitry and measurement techniques.
- That you are familiar with the host PC which you are using.
- That you are capable of writing your own programs.

The manual contains the following sections.

Chapter 1 - Introduction.

- Chapter 1 contains an overview of the PC-126[1] series of boards.

Chapter 2 - Architecture.

- Chapter 2 discusses the basic operation of the PC-126 board.

Chapter 3 - Configuration.

- Chapter 3 discusses the selection of various board parameters and the configuration of the board for various operating requirements.

Chapter 4 - Interconnection.

- Chapter 4 describes the connection of the PC-126 series of boards to the host computer and to user inputs.

Chapter 5 - Register structure.

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[1] For the rest of the manual, PC-126 will be used to refer to the PC-126 and PC-126A. Where information is specific to a particular board, this will be stated in the text.

- Chapter 5 describes the register structure of the PC-126 series of boards.

Chapter 6 - Programming guide.

- Chapter 6 provides a tutorial style guide to programming the PC-126. Information is provided as to where in the driver software to obtain examples of the topics discussed.

Chapter 7 - Calibration.

- Chapter 7 describes the procedures and equipment required to calibrate the PC-126 series of boards. Calibration software included with the PC-126 is also described.

Appendix A - Hardware Specifications.

- Appendix A provides complete electrical specifications for the PC-126 series of boards.

Appendix B - PC-126 Differences Compatibility.

- Appendix B discusses the compatibility of the PC-126 to various other PC-30 series boards.

Appendix C - PC-126 Component Layout.

- Appendix C contains layout diagrams of the PC-126.

Appendix D - Problem Determination guide.

- Appendix D contains information which may help you if you are experiencing problems with your PC-126.

Chapter 1

Introduction

1.1. Overview

The PC-126 and PC-126A series of boards are full size, low cost, high accuracy analog and digital I/O boards for the IBM PC, PC/XT, PC/AT, PS/2 model 25, PS/2 model 30 and compatible series of computers..

- PC-126. The PC-126 forms the basis of the range, and features 16 analog input channels with 50 KHz throughput, two 12 bit D/A outputs, 8 digital input lines and 8 digital output lines. The PC-126 is specifically designed to operate in laptop style host PCs. In addition to its small size, the PC-126 draws power only from the host PC's +5 V power supply.

- PC-126A. The PC-126A has similar features to the PC-126, but does not have D/A outputs, and draws power from the host PC's +12 and -12 V power rails. It is a low cost board, intended for use in desktop systems.

1.2. Features

The PC-126 can be plugged into any of the fully bussed slots in a PC/XT/AT, PS/2 model 25 or 30 or compatible computer.

1.2.1. A/D subsystem

The A/D subsystem's major component is a monolithic analog to digital converter, which accepts analog voltage inputs from sensors, such as pressure transducers and thermocouples, and converts them into 12 bit digital codes.

This code is transmitted to the host processor, which processes it according to the software in use at the time.

The A/D section allows for 16 single-ended inputs, and can be configured for unipolar (input range of 0 to 10V) or bipolar (input range of +/-10V) operation. Resolution is 12 bits. For unipolar inputs, the output code is straight binary, and for bipolar, offset binary.

The A/D may be operated in either single conversion or continuous conversion mode. In single conversion mode the board performs a single conversion on the selected input channel and stops on completion of this conversion. In continuous conversion mode conversions are performed at a set rate. This rate is set by programming the PC-30's internal timer or an external clock source.

A/D conversions may be monitored by either polled I/O or by interrupts. In polled I/O mode the software continuously polls the board's status register to check for completion of the current A/D conversion. In interrupt mode, the board automatically generates a hardware interrupt on completion of each conversion.

Key specifications

- A/D resolution: 12 Bits
- Nonlinearity: Less than +/-0.75 LSB
- A/D full scale input ranges: 0 to +10V and -10 to +10V switch selectable.
- Number of A/D inputs: 16 single ended.
- A/D throughput rate: 50 KHz.

1.2.2. D/A Subsystem

The D/A subsystem consists of two 12-bit D/A converters, DAC0 and DAC1. The D/A subsystem is not present on the PC-126A. Digital outputs are received from the host processor and converted to an analog voltage output as required by the application in hand. The two DACs are independent of one another, and can operate at a throughput of up to 50KHz. Output ranges are independently configurable as 0- +5V unipolar, or as +/-5V bipolar.

Key specifications: DAC0 and DAC1

- D/A resolution: 12 Bits
- D/A nonlinearity: Within 0.01% FSR
- Full scale output ranges: 0 to +5V, -5V to +5V.
- D/A throughput rate: 50 KHz.

1.2.3. Digital I/O subsystem

The digital I/O subsystem is an interface for the transfer of digital data from and to the PC bus to and from one or more peripheral devices connected to the PC-126. There is a single eight-bit digital input port, and a single eight-bit digital output port. The output port provides high power drivers, suitable for directly driving solid-state relay modules etc.

1.2.4. Interface logic

The PC-126 is accessed via I/O operations performed by the host processor. Of the 12 bit address received by the board, the most significant 8 bits select the board, and the least significant 4 bits select the register to be accessed.

The PC-126 occupies 16 byte locations: four byte locations for the A/D subsystem, four for the D/A subsystem, two for the digital I/O subsystem, four for the counter/timer system, and two for control and manufacturing test functions. The base address of the PC-126 can be switch selected in the range 200 to 7E0 (hex).

The PC-126 operates from the +5V line of the PC bus.

1.3. Software support

Software support for the PC-126 is available in a variety of forms :

1.3.1. PC-126 software support pack

The PC-126 software support pack provides two packages; the PC-30 driver software, and Status-30. This is supplied with each PC-126 sold.

1.3.1.1 Driver software

This consists of a set of real time device drivers for use with the PC-126 boards. These device drivers are written in C, and are callable from most compiled languages, including the following :

- Microsoft C.
- Microsoft FORTRAN.
- Microsoft QuickBasic.
- Borland C.
- Turbo Pascal versions 4 and 5.

The driver software allows programmers to control the PC-126 via high level function calls, so allowing users to write custom software without understanding the low level operation of the PC-126. The driver package provides access to all PC-126 capabilities, including interrupts. Also included with the driver package is complete source code, in C, for the entire driver package. This allows advanced users to modify existing code, rather than having to start writing low level code from scratch.

1.3.1.2 Status-30

Status-30 is an application program, which combines the features of an oscilloscope, spectrum analyzer and data logger in one package. Now in release 2, Status features a graphical interface, pull-down menus, and extensive on-line help. The program can be controlled either by a mouse or from the keyboard, and has sophisticated zoom, pan, and cursor measurement capabilities.

Status's data analysis capabilities not only include FFT (Fast Fourier Transforms), but also include Chirp-Z transforms. Chirp-Z transforms can provide more than 60 times better frequency resolution than conventional FFTs. For example, sampling at 50KHz, Status-30 can provide frequency resolution of 0.2 Hz with a record length of only 4096 samples.

Waveforms and signal spectrums can be plotted to a variety of plotters. In addition, Status-30 can store data in a variety of formats, compatible with most spreadsheet and graphing programs, as well as special purpose programs such as MathCad and Hypersignal.

1.3.2. IoCalc

IoCalc is a spreadsheet program, with the ability to acquire, process and output data to and from analog and digital I/O devices in real-time. Not just an add-on for a spreadsheet program designed for business applications, IoCalc is a custom written real-time program, optimized for engineering and scientific users. Under OS/2, IoCalc provides full multi-tasking operation, allied with powerful inter-task communication capabilities.

Data is acquired directly into spreadsheet cells, processed, and in turn sent to output devices direct from spreadsheet cells.

The entire spreadsheet, or part of it, can be updated at fixed intervals, with timing resolution down to 10 milliseconds. Any section of the spreadsheet can also be logged to disk or printer at fixed intervals.

IoCalc can be used to implement virtually any process that can be represented mathematically. Sample spreadsheets supplied with IoCalc include : Control loops (PID and 'Bang-bang'), intelligent data loggers, digital filters, multi-channel multimeters, thermocouple compensation and oscillators.

1.3.2.1 Features

- True real-time, multi-tasking data processing
- Familiar user interface
- Can be used to implement control loops, data loggers, digital filters and more
- Menu driven, with context sensitive help.
- Either DOS or OS/2 protected mode operation.

1.3.2.2 Applications

- Process control
- Data logging
- Monitoring
- Automatic test
- Smart instrumentation
- Laboratory data collection
- Virtual instruments

1.4. Throughput

The throughput of the PC-126 series of boards is dependent on several factors, principally the performance of the host PC. The PC-126 transfers data by program transfer :

1.4.1. Program transfer.

When program transfer techniques are used (polled I/O or interrupts), the maximum possible throughput is limited by the processing power of the CPU in the host PC, and the efficiency of the software in use. In general, throughput of greater than 50 KHz is very seldom achieved.

Note that the software drivers for the PC-126, although efficient, are written as general purpose, "idiot proof" routines. Custom assembly language routines can easily be written which will outperform these.

1.5. Getting Started

If you want to get started quickly and have not changed any of the factory installed switches on the PC-126, here's what to do:

i. Install the PC-126 in your computer. (Chapter 3 provides brief instructions on this, but if you are not sure, it is better to get someone who is qualified to do this).

ii. Connect up a voltage source to any (or all) of the input channels. (You can also loop the analog outputs back to the inputs). The pin-out of the PC-126 connector is shown in figure 4.1 later in the manual.

iii. Run the DIAG.EXE program on the Calibration disk. This program will execute the PC-126 diagnostics routine, and should print out the following message:

    PC-30 Driver Version 1.05
    PC-30 diagnostics report the following:

    PC-126 found, operating correctly.

iv. If the "found" message is displayed, then the PC-126 is installed correctly. If the DIAG program displays some other message, then you probably need to reconfigure the board. This is discussed in chapter 3 of this manual.

1.6. Accessories

In order to assist in applying the PC-126, several accessories are available. Only a brief description is given here. Consult your dealer for full details.

1.6.1. PC-81

The PC-81 is an input expander board. Multiple PC-81s may be used to expand the input channel capability of the PC-126 to more than 65000 channels. Each PC-81 has 64 screw terminal inputs.

1.6.2. PC-22

The PC-22 is a Euro-card format single channel signal conditioning module. It provides programmable gain, and filtering functions.

1.6.3. PC-68

The PC-68 is a Euro-card format four channel strain gage signal conditioning board. It provides four independent channels with user programmable excitation, differential inputs, and a high performance instrumentation amplifier. The PC-68 can also be used simply as a four channel ultra-high performance instrumentation amplifier board.

Chapter 2

Architecture

This chapter describes the architecture of the PC-126 series of boards. The block diagram in figure 2.1 highlights the major elements contained on the board, and their interrelationship. There are four major subsections. These are the following:

2.1. D/A Subsystem

The D/A subsystem contains two 12-bit D/A converters as well as their associated circuitry, including buffer registers. In order to transfer data written to the buffer register to the D/A, and hence to the analog output, a D/A clock pulse must be generated via the clock system, described below.

2.2. A/D Subsystem

The A/D subsystem contains several separate components:

- The input multiplexer. The multiplexer selects one of sixteen single ended input channels. This channel is selected by a channel address, obtained from the Control/Channel register.

- The sample and hold unit. The sample and hold unit holds the selected input channel steady for the duration of the A/D converter's conversion process.

- The A/D converter performs the actual A/D conversion. An A/D conversion is begun by an A/D strobe. This is generated by the timing and control section, described later.

Data may be transferred from A/D either by polled I/O or interupts.

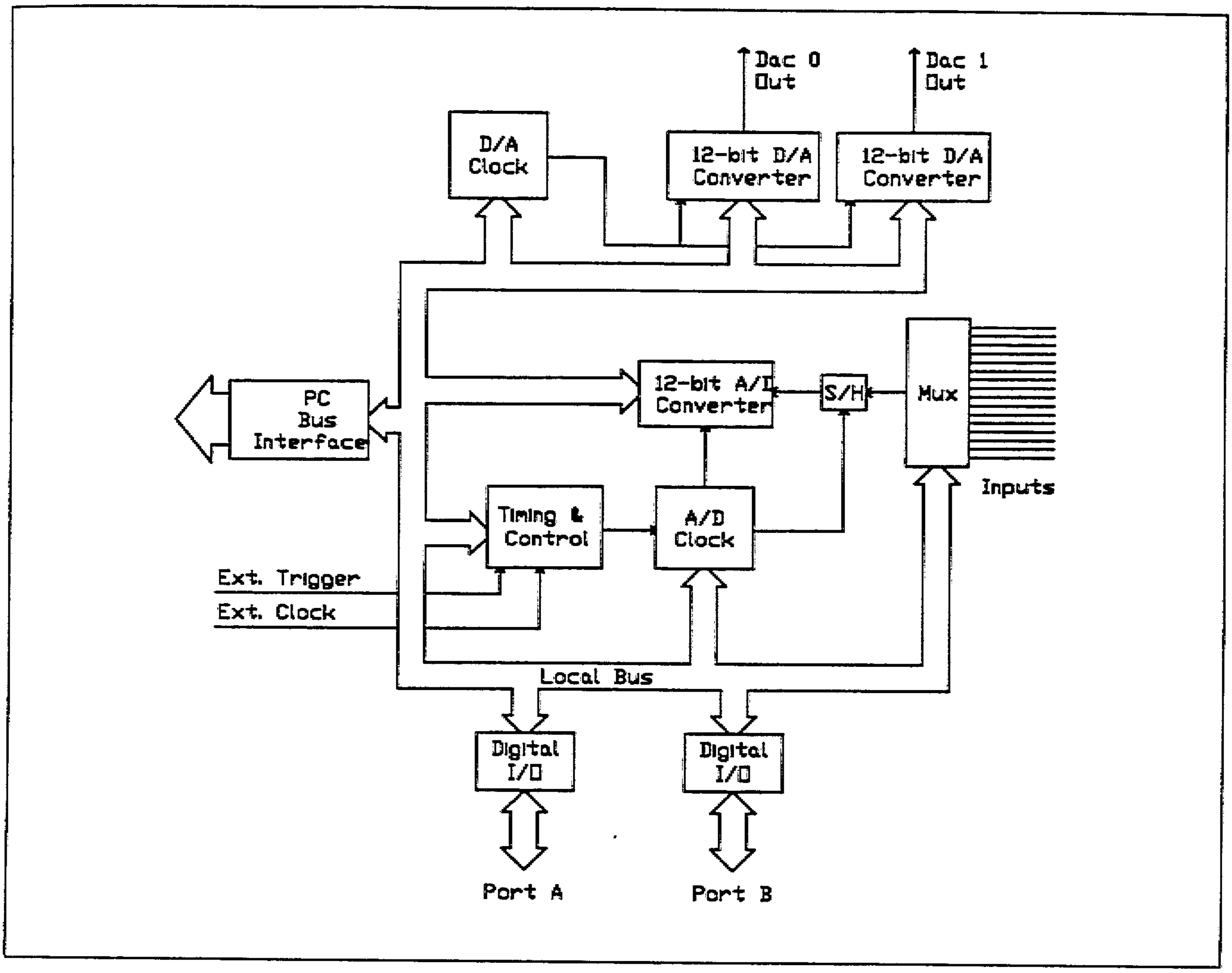

Figure 2.1.

2.3. Bus interface.

The bus interface is responsible for two functions:

i. The decoding of the board's base address. The board's base address is set by switches.

ii. The generation of interrupts. Interrupts can be generated at the end of each A/D conversion. The interrupt level is factory preset to 5.

2.4. Timing and control

The timing and control subsection is responsible for the generation of A/D and D/A strobes. A/D strobes cause the A/D converter to begin a conversion. D/A strobes cause the contents of the D/A buffer registers to be transferred to the analog outputs. A simplified block diagram of this section is shown in figure 2.2.

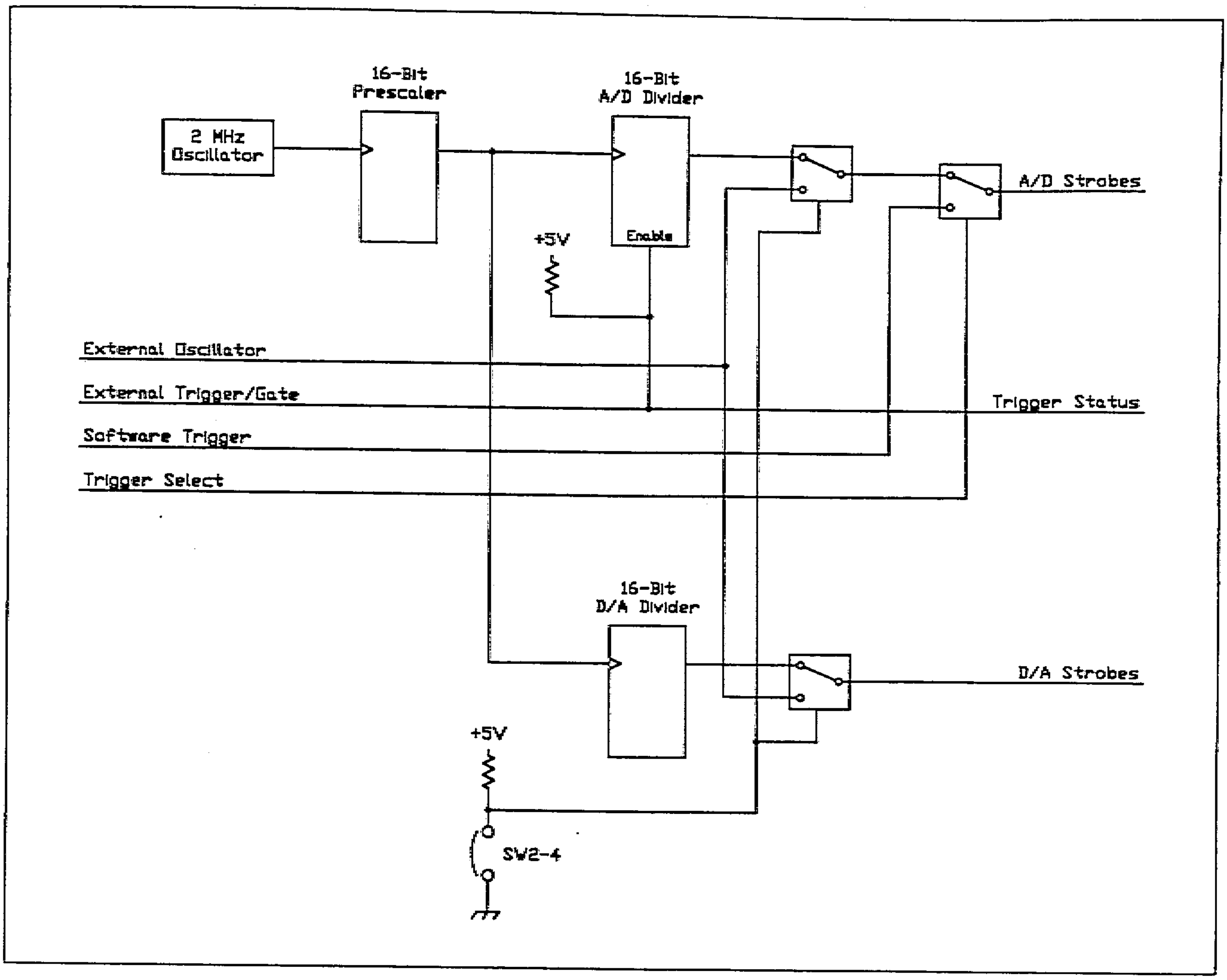

Figure 2.2.

A/D strobes may be selected under program control to be either hardware or software strobes.

i. Software strobes. Software strobes are generated by a write operation to a control register. They hence allow a single conversion to be started under program control.

ii. Hardware strobes. The source of hardware strobes is the internal clock. This is derived from a 2 MHz crystal controlled oscillator. This signal is then divided down by a programmable ratio.

The timing and control section contains three major subsections:

2.4.1. Clock Prescaler.

The 2 MHz signal from the board's master oscillator is used to drive the clock prescaler. This is a 16 bit counter, the output from which drives the A/D clock divider and the D/A clock divider.

2.4.2. A/D Clock divider.

The A/D clock divider divides the signal from the prescaler by a programmable ratio. No A/D strobes are generated unless the divider is enabled, so allowing the start of a set continuous conversion to be synchronized to the trigger input. Note that this divider is active only for an internally generated clock signal.

2.4.3. Clock selection multiplexer.

The Clock selection multiplexer determines whether the A/D strobe signal is derived from the hardware clock (which may be either derived from the internal clock, or from the external input) or from the software clock. The software clock is generated by a write operation to a control register, and hence allows a single conversion to be started under program control.

2.4.4. D/A clock divider.

The D/A clock divider performs a similar function to the A/D divider, but generates strobes to the D/A converter. The input to the D/A clock divider is the output from the prescaler. Note that unlike the A/D clock system, there is no direct provision for software strobes; when a program wishes to update the outputs of the D/A converters, a hardware strobe *must* be generated via the D/A clock divider, or from an external signal.

2.5. A/D operations.

2.5.1. Sampling data

A/D operations proceed as follows:

i. The board is initialized. This comprises the following steps:

   a) The appropriate clock mode is selected, and the clock divider programmed.

   b) The A/D buffer and the trigger system are reset.

   c) The channel to be converted is written to the channel register.

ii. The system is then enabled, either by a trigger command, or by an external signal.

iii. As soon as conversions are enabled, A/D conversions start. These conversions occur at the rate set by either the external clock or the internal clock and the value programmed into the clock divider.

iv. Conversions continue until the board is disabled. There are two methods of transferring data from the A/D to memory. These are the following:

2.5.2. Simple Polled I/O.

Polled I/O is the simplest possible method of data transfer. It proceeds as follows:

i. The program continuously waits for a conversion cycle to complete.

ii. The data from the A/D conversion is then read, and stored in the PC's memory by the program.

iii. This process repeats until however many samples are required have been read.

2.5.3. Interrupt driven I/O.

Interrupt driven I/O allows data acquisition to occur in the background. It proceeds as follows:

i. The board is configured to generate interrupts when each A/D conversion completes, and the address of an Interrupt Service Routine (ISR) is programmed into the PC's hardware.

ii. When an interrupt occurs, whatever program is running is interrupted, and the interrupt service routine begins to run. The ISR then reads the data from the A/D conversion, and stores it in the PC's memory.

iii. This process repeats until however many samples are required have been read.

2.6. D/A operations.

2.6.1. Generating output waveforms

D/A operations proceed as follows:

i. The board is initialized. This comprises the following steps:

   a) The appropriate clock mode is selected, and the clock divider programmed.

   b) The trigger system is reset.

   c) The first data point is then written to the D/A converter's buffer.

ii. The system is then enabled, either by a trigger command, or by an external signal.

iii. As soon as conversions are enabled, D/A conversions start. These conversions occur at the rate set by either the external clock or the internal clock and the value programmed into the clock divider.

iv. The program continuously waits for a conversion cycle to complete, by monitoring the PC-126's D/A ready status bit.

v. As soon as the ready bit is set, the next data point is written to the D/A buffer registers.

vi. Conversions continue until the board is disabled.

2.7. Digital I/O.

The digital I/O section of the PC-126 consists of two 8-bit ports (port A and B). Port A is an 8-bit input port, and port B an 8-bit output port.

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Chapter 3

Configuring the board

3.1. Introduction

The PC-126 boards can be configured in many different ways to suit each user's individual requirements. This configuration is set by the position of the two DIP-switch blocks on the board. Each set of switches controls a specific aspect of the operation of the board. These are as follows :

i. Bus interface. The base address of the board and the interrupt level used by the board can be set. As supplied by the factory, the base address is set to 700H, and the interrupt level to 5. This allows operation in a standard PC/XT/AT which contains only conventional boards (multifunction boards, disk controller boards, display boards etc), but may require modification if exotic boards (other scientific boards, certain backup systems etc) are installed.

ii. D/A operation. The output range of all D/A converters may be selected independently. As supplied by the factory, all D/A outputs are set for bipolar output, -5 to +5 volts. In addition, the D/A converters can be set for either internal or external clocks.

iii. A/D operation. The input range of the A/D may be set, by switch, for uni- or bipolar operation, for input voltage ranges 0 - +10V or +/-5V.

3.2. Changing the Configuration

The switches may be located either from the diagram in appendix C, or from the labels on the PC-126 board itself. Switch block 1 (SW1) is the eight way switch block, and switch block 2 (SW2) is the four way block.

In order to change the switches settings, follow the procedure below :

i. Switch off the computer.

ii. Remove the board.

iii. Change the required switches settings.

iv. Replace the board in the PC.

v. Power up, and run a program (such as DIAG), which executes the PC-126 diagnostics routines.

Base Address (hex)	Switch				
	SW1-1	SW1-2	SW1-3	SW1-4	SW1-5
200	On	On	On	On	On
220	On	On	On	On	Off
240	On	On	On	Off	On
260	On	On	On	Off	Off
280	On	On	Off	On	On
2A0	On	On	Off	On	Off
2C0	On	On	Off	Off	On
2E0	On	On	Off	Off	Off
300	On	Off	On	On	On
320	On	Off	On	On	Off
340	On	Off	On	Off	On
360	On	Off	On	Off	Off
380	On	Off	Off	On	On
3A0	On	Off	Off	On	Off
3C0	On	Off	Off	Off	On
3E0	On	Off	Off	Off	Off
600	Off	On	On	On	On
620	Off	On	On	On	Off
640	Off	On	On	Off	On
660	Off	On	On	Off	Off
680	Off	On	Off	On	On
6A0	Off	On	Off	On	Off
6C0	Off	On	Off	Off	On
6E0	Off	On	Off	Off	Off
700	Off	Off	On	On	On
720	Off	Off	On	On	Off
740	Off	Off	On	Off	On
760	Off	Off	On	Off	Off
780	Off	Off	Off	On	On
7A0	Off	Off	Off	On	Off
7C0	Off	Off	Off	Off	On
7E0	Off	Off	Off	Off	Off

Table 3.1. PC-126 Base address settings.

3.3. Bus Interface Configuration.

3.3.1. Base address

The base address setting is controlled by switches 1 through 5 of switch block 1 (SW1-1 to SW1-5). As supplied by the factory, the address is set to 700H. The board occupies 16 consecutive locations. Table 3.1 shows the switch selections for the PC-126.

3.3.2. Interrupt level.

3.3.2.1 Switch setting

The PC-126 interrupt level may be set to 3, 5 or 7, under the control of switches 6, 7 and 8 of switch block 1 (SW1-6 to SW1-8). The factory default setting for level 5. Table 3.2 below shows the settings.

Interrupt level	Switches		
	SW1-6	SW1-7	SW1-8
3	Off	Off	On
5	Off	On	Off
7	On	Off	Off

Table 3.2. Interrupt level switch settings.

Warning
Only one interrupt level may be installed at any one time. Selecting more than one interrupt level may cause permanent damage to your PC-126.

3.3.2.2 Selection of interrupt level

In a standard PC, interrupts are allocated as follows :

level 3	Used by COM2: (if installed)
level 4	Used by COM1: (if installed)
level 5	Used by fixed disks (XT and AT)
level 7	Used by LPT1: (if installed)

An interrupt level which is not already used must be selected. Level 5 is the factory default. Note that unless the interrupts are specifically enabled by software, the interrupt output from the board is tri-stated (does not have any effect on the PC bus).

3.4. Clock selection.

The clock source for both the A/D and D/A converters may be selected to be either (refer to figure 2.2) :

i. Internal clock. If internal clock mode is selected, the A/D converter is clocked by the output Clock selection multiplexer, as discussed in section 2.4.3. This output is either the output of the A/D clock divider, or software strobes, as selected by the STBC bit. When internal clock mode is selected, the D/A converter is clocked by the D/A clock divider.

ii. External clock. If external clock mode is selected, then both the A/D and D/A converters are clocked from the external oscillator input, on the PC-126's external connector. The external oscillator input is a TTL input, and is positive edge sensitive.

Clock source selection is performed via switch 4 of switch block 2 (SW2-4), as shown in table 3.3, below.

Trigger Source	Switch Setting SW2-4
Internal	On
External	Off

Table 3.3. PC-126 clock source selection.

Note : The clock selection switch, SW2-4, controls the clock source of BOTH the A/D and the D/A converters. The clock source for these cannot be selected independently.

3.5. D/A switch selections.

The two D/A converters may be switched for either monopolar (0 to 5V) or bipolar (-5 to +5V) output ranges. The D/A switches are switches 1 and 2 of switch block 2 (the 4-way switch block). Setting are as shown in table 3.4 and 3.5, below :

DAC0 Output Range	Switch Setting
	SW2-1
0 - 5V -5 - +5 V	Off On

Table 3.4. DAC 0 output range.

DAC1 Output Range	Switch Setting
	SW2-2
0 - 5V -5 - +5 V	Off On

Table 3.5. DAC 1 output range.

3.6. A/D configuration.

3.6.1. A/D voltage range switch settings

The A/D may be configured for input range. This is controlled by switch 3 of switch block 3 (SW2-3). The A/D switch settings for the PC-126 are shown in table 3.6 below.

A/D Input Range	Switch Setting
	SW2-3
0 - 10V -10 - +10 V	On Off

Table 3.6. PC-126 A/D input range.

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Chapter 4

Interconnections

4.1. Introduction

The PC-126 plugs into IBM PC/XT/AT or compatible expansion slots at connector P1. All boards in the family connect to the user's circuitry at connector J1. This chapter describes these two connectors.

4.2. Connections to the IBM backplane.

PC-126 boards can be plugged into any slot of the IBM backplane, with the exception of the J8 slot of the XT. This particular slot requires the -CARDSLCT signal, which is not used on other slots. All communication to and from the host processor is carried out via this connector.

4.3. User connection.

4.3.1. PC-126

The PC-126 is connected to the user interface via a 50 way IDC connector. This connector accommodates the following signals :

- 16 single ended lines of analog input.
- 2 lines of analog output.
- 8 digital input lines.
- 8 digital output lines.
- External trigger and oscillator.

J1 also provides + and -12V power supply, with limited current output.

Ch 0	1	2	Ch 8
Ch 1	3	4	Ch 9
Ch 2	5	6	Ch 10
Ch 3	7	8	Ch 11
Ch 4	9	10	Ch 12
Ch 5	11	12	Ch 13
Ch 6	13	14	Ch 14
Ch 7	15	16	Ch 15
Analog Ground	17	18	nc
+12V Out	19	20	-12V Out
Power Ground	21	22	DAC0 Output
DAC0 Ground	23	24	DAC1 Output
DAC1 Ground	25	26	Digital Ground
Digital Ground	27	28	Dig. Input Line 0
Dig. Input Line 1	29	30	Dig. Input Line 2
Dig. Input Line 3	31	32	Digital Ground
Dig. Input Line 4	33	34	Dig. Input Line 5
Dig. Input Line 6	35	36	Dig. Input Line 7
Digital Ground	37	38	Dig. Out. Line 0
Dig. Out. Line 1	39	40	Dig. Out. Line 2
Dig. Out. Line 3	41	42	Digital Ground
Dig. Out. Line 4	43	44	Dig. Out. Line 5
Dig. Out. Line 6	45	46	Dig. Out. Line 7
Digital Ground	47	48	Digital Ground
External Trigger	49	50	Ext. Oscillator

Figure 4.1. PC-126 connector, as seen from the rear of the PC.

Figure 4.1. shows these connections, together with their pin assignments. Do not make use of any numbers on the PC-126 board.

4.3.2. Signal definitions.

i. CH0 - CH15. These are the analog input lines. Note that no more than +- 10V must be applied to these pins.

ii. ANALOG GROUND. One analog ground line is provided. The analog input lines are measured relative to AGND.

iii. DAC0 OUTPUT. This is the analog output line for DAC0.

iv. DAC0 GROUND. This is the analog return line for DAC0. It is internally connected to analog ground.

v. DAC1 OUTPUT. This is the analog output line for DAC1.

vi. DAC1 GROUND. This is the analog return line for DAC1.

vii. +12V. This line provides a +12V Power supply to the user's interface. Maximum permissible current draw is 125mA. On REV III boards it is protected with a 125mA pico fuse against overloads and shorts. Note that on the REV II boards this line was +15V.

viii. -12V. This line provides a -12V Power supply to the user's interface. Maximum permissible current draw is 125mA. On the REV III boards it is protected with a 125mA pico fuse against overloads and shorts. Note that on the REV II boards this line was -15V.

ix. POWER GROUND. This is the return line for the +12V and -12V supplies. It is internally connected to analog ground.

x. Digital Input Lines 0 - 7. This is the digital input port.

xi. Digital Output Lines 0 - 7. This is the digital output port. The digital output lines have high power (24 mA) drive capability, suitable for directly driving most solid-state relays.

xii. DIGITAL GROUND. This is the return line for the digital input and output lines. It should be connected to the ground of any digital equipment connected to the PC-126. It is internally connected to analog ground.

xiii. External Trigger. When the external trigger line is a logical high, the A/D clock divider is active, and A/D clock pulses are produced. When this line is a logical low, the A/D clock divider is low, and no A/D clock pulses are produced. Note that this has no effect on either software strobes or the external oscillator. The external trigger input is TTL compatible, with a 4K7 pull-up, and so may be driven either from totem-pole or open collector TTL gates. This line may also be read under software control.

xiv. External Oscillator. The external oscillator provides conversion strobes to both the A/D and D/A converters, if switch SW2-4 is in the OFF position. If SW2-4 is on, then this signal has no effect. The external trigger input is TTL compatible. Conversions are performed on positive edges.

4.4. Analog I/O

4.4.1. Recommended analog input schemes.

Analog signals are input into the PC-126 as single ended inputs. Single ended inputs are shown diagrammatically in figure 4.2.

Analog inputs are limited to a voltage of between -10 and + 10 V.

Warning:
Overloading any analog input may cause other input channels to become inaccurate or noisy.

4.4.2. Analog output

The analog output lines are referenced the analog ground line. The analog output lines may be switched to give either monopolar or bipolar outputs.

4.4.3. Connection guidelines.

The PC-126 is a very high performance I/O subsystem, and was designed to have lower input noise levels than any similar analog I/O board currently available. Its performance may however be severely affected by incorrect connection techniques. This especially true of noise levels.

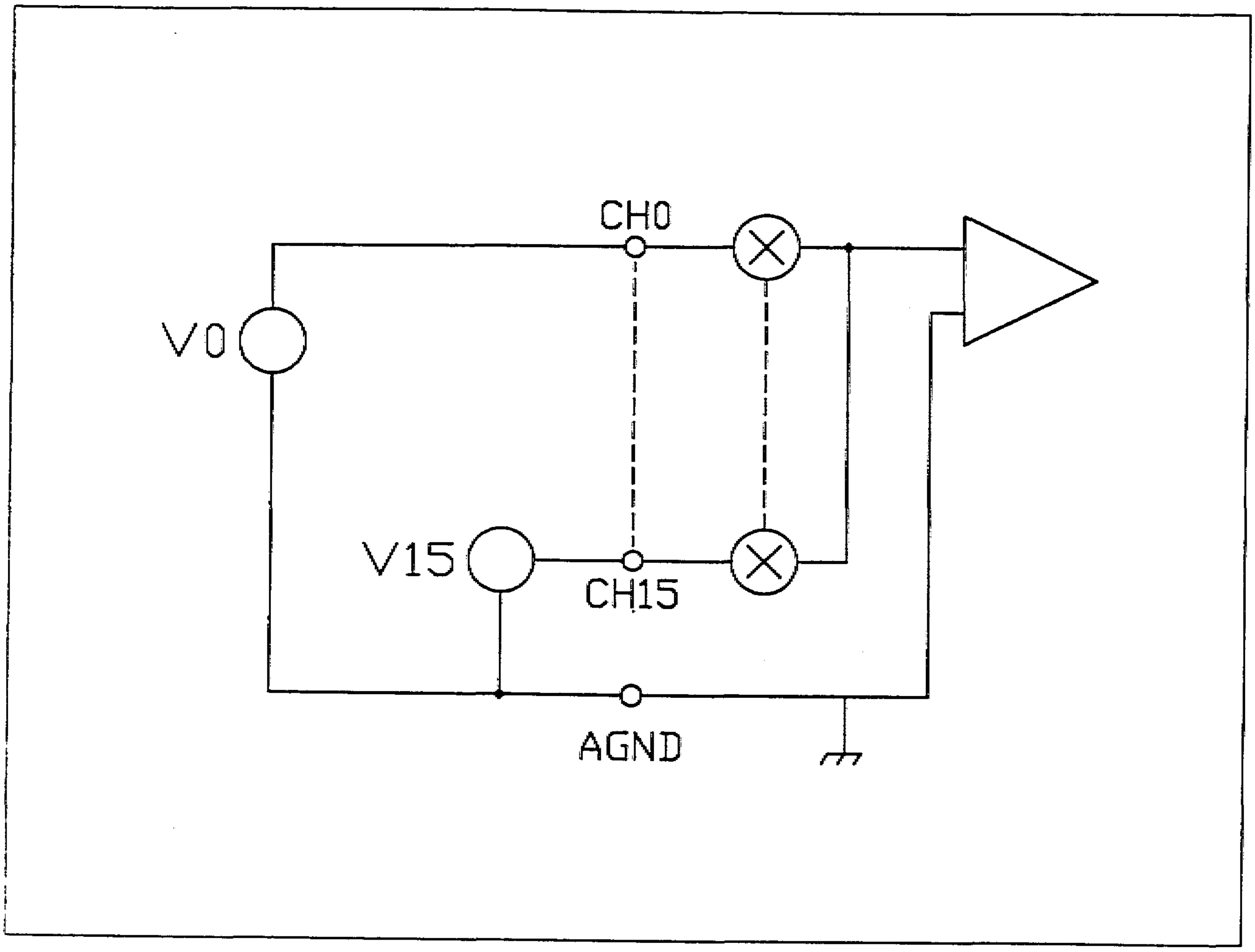

Figure 4.2. Single ended analog inputs.

4.4.3.1 Shielded input lines.

Wherever possible, leads should be shielded. Optimally, each input line should be individually shielded. The shield should be tied to analog ground at the instrument end of the connection only.

4.4.3.2 Input voltages.

To maintain stated accuracy, all inputs to the PC-126 must be within +- 10 V.

4.4.3.3 Source Impedance.

To maintain stated accuracy, all devices connected to the analog inputs of the PC-126 must have a source impedance of less than 1 KOhm.

4.5. Digital I/O.

The digital I/O lines are referenced to digital ground, as are the external trigger and oscillator lines. Note that the digital output lines are always active, and that no other digital output should be connected to them

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Chapter 5

Register structure

5.1. Introduction

At the lowest level, the PC-126 can be programmed using I/O input and output instructions. This chapter contains the information required to do this. Although not difficult, this is time consuming, and requires detailed knowledge of the PC-126, as well as the operation of the host PC and its operating system. In order to simplify this process, a set of device drivers is available for use with the board. The use of these allows access to all board functions. These drivers are described in the "User Manual for PC-30 Driver Software" manual.

The next chapter discusses various programming techniques and tips.

5.2. Register structure.

The PC-126 uses 16 consecutive address locations in I/O space. The layout of these registers is shown in figure 5.1. Note that certain addresses have different read and write register functions.

Note also that the addresses above are given as offsets from the base address of the board. This base address is switch selected as described in chapter 3.

Each register will now be described in detail.

Warning
You should not write to, or read from, unused registers. All unused registers are reserved for manufacturing test, or for future developments.

Offset From Base	Register Name	
	Read	Write
0	A/D Low Byte (ADDATL)	—
1	A/D Data/Status(ADDSR)	—
2	Control/Channel (ADCCR)	
3	Mode/Status Register (ADMDE)	
4	—	Prescaler (PRESCALER)
5	—	A/D Divider (DIVIDER)
6	—	D/A Divider (USR_CNT)
7	—	Counter Control(TMRCTR)
8	Digital Input (DIOP0)	—
9	—	Digital Output (DIOP1)
10	—	
11	—	
12	—	DAC0 Low Byte (DADATL0)
13	—	DAC0 High Byte (DADATH0)
14	—	DAC1 Low Byte (DADATL1)
15	—	DAC1 High Byte (DADATH1)

Figure 5.1. PC-126 Register Structure.

5.2.1. ADDATL - A/D data low byte (offset 0) (read only)

On completion of an A/D conversion, the A/D converter loads this register with digital data. To retrieve converted data, the user must perform a read operation to ADDATL. Bit 0 is the LSB. The layout of this register is shown in figure 5.2

Data should not be read from this register unless the A/D done bit in the ADMDE register is set.

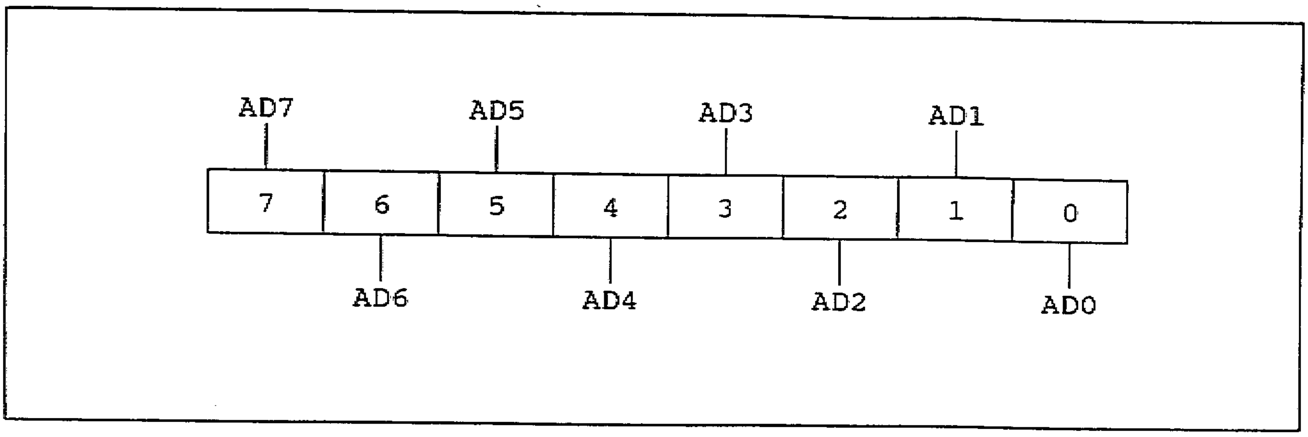

Figure 5.2. A/D data register (low byte).

Bits 7-0 - A/D data (AD)

These bits are the low byte of the 12-bit code which is returned from an A/D conversion.

5.2.2. ADDSR - A/D data/status register (offset 1)

The ADDSR contains the high nibble of the A/D result, and contains the current A/D's status information. The bit functions of the ADDSR are shown in figure 5.3.

Data should not be read from this register unless the A/D done bit in the ADMDE register is set.

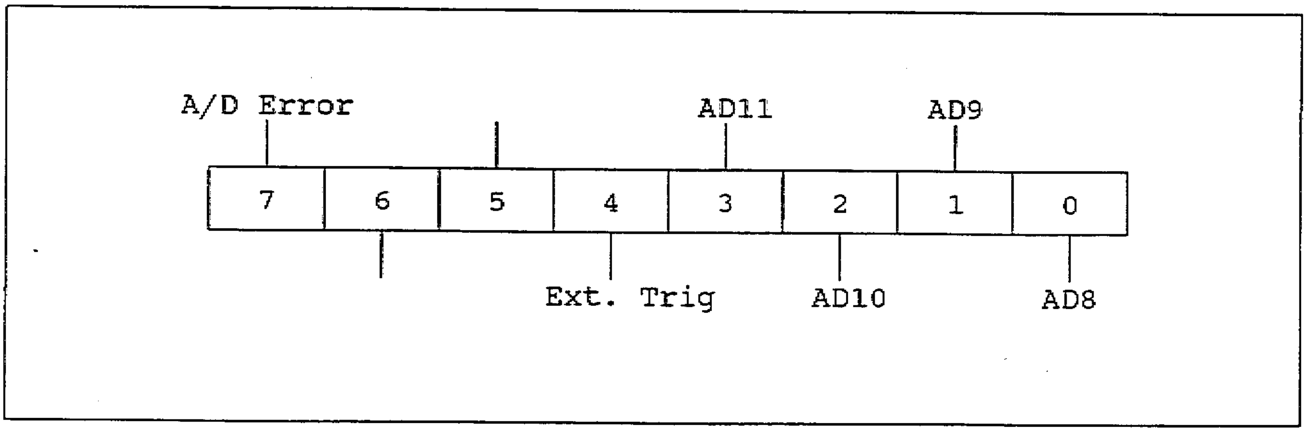

Figure 5.3. A/D data/status register.

Bit 7 - A/D error

Set when an error occurs during an A/D conversion. Such conditions can result from two causes:

either the current conversion has been completed while data from the previous conversion has not been completely read (ADDATL low byte not read), which is a data overflow error, or an attempt has been made to initiate a new conversion while the current conversion is still in progress, which is a trigger error.

Bit 7 is cleared by any write to the ADMDE register.

This bit is identical to the A/D error bit in the ADMDE register.

Bit 6 - Reserved

The result of reading this bit is undefined.

Bit 5 - Reserved

The result of reading this bit is undefined.

Bit 4 - Ext. Trig

This bit reflects the status of the external trigger pin. It is identical to the bit in the ADMDE register.

Bits 3-0 - A/D data (AD)

The four higher bits of 12-bit data from an A/D conversion.

5.2.3. ADCCR - A/D Control/channel register (offset 2)

The ADCCR contains channel address bits, A/D clock control bits as well as DMA and interrupt enable bits. The bit functions of the ADCCR are shown in figure 5.4.

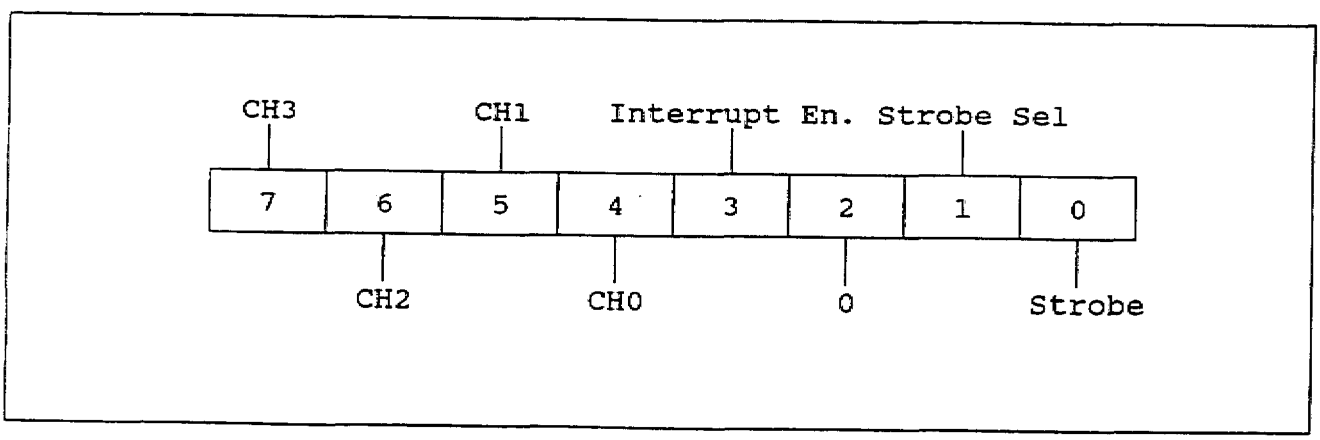

Figure 5.4. A/D control/channel register.

Bits 7-4 - Channel (CH)

These bits specify a four bit channel address. This channel is the channel which will be converted on the next A/D strobe.

Bit 3 - Interrupt enable

If the interrupt enable bit is set, then interrupts will be generated at the end of each A/D conversion.

This bit is controlled by the program in use. All interrupts are disabled when this bit is cleared. Bit 3 is cleared on power up.

Note
When interrupts are disabled, the PC-126 electronically disconnects the interrupt line from the Pc's bus.

Bit 2 - Reserved.

This bit is reserved, and should always be set to 0.

Bit 1 - Strobe Select (STBC).

This bit controls the source of A/D strobes to the A/D converter. If it is set, then software strobes are used. Software strobes are generated by toggling the SSTB bit (bit 0). If the STBC bit is cleared, then A/D clock pulses are used to start A/D conversion cycles. A/D clock pulses are generated from the A/D clock prescaler/divider combination.

Bit 0 - Strobe (SSTB).

Bit 0 of the ADCCR is the software strobe bit. If the STBC bit is set, then a software strobe is generated by taking the strobe bit high, then low. If the STBC bit is low, then the SSTB bit is ignored.

Warning
Whenever you change the state of the STBC bit, the SSTB bit must be 0 (cleared). If the SSTB bit is not clear, spurious A/D conversion cycles may be generated.

5.2.4. ADMDE - A/D mode register (offset 3)

The ADMDE register contains A/D mode selection bits, and status information. The bit functions of the ADMDE register are shown in figure 5.5.

Note
The value 92 (hex) must be written to this register prior to any other activity.

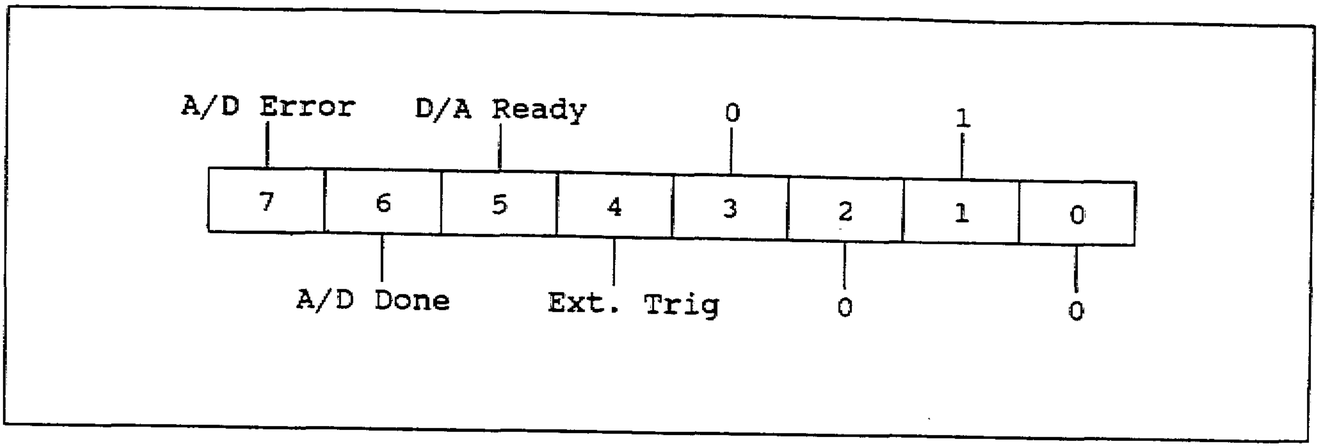

Figure 5.5. A/D mode register.

Bit 7 - A/D error

Set when an error occurs during an A/D conversion. Such conditions can result from two causes: either the current conversion has been completed while data from the previous conversion has not been completely read (ADDATL low byte not read), which is a data overflow error, or an attempt has been made to initiate a new conversion while the current conversion is still in progress, which is a trigger error.

Bit 7 is cleared by any write to the ADMDE register.

This bit is identical to the A/D error bit in the ADDSR register.

Bit 6 - A/D done

Set by the A/D converter to indicate that A/D data is available. If bit 3 of the ADCCR is set (interrupts are enabled), then an interrupt will be generated when bit 6 is set.

Bit 6 is cleared by a read of the ADDATL.

Data should not be read from the ADDSR or ADDATL registers unless this bit is set.

Bit 5 - D/A ready

This bit is set when the buffer register of the D/A converters are empty. The buffer registers are emptied when a D/A clock occurs, transferring the contents of the buffer register to the D/A outputs. The D/A ready bit is cleared by a write to any D/A register.

Bit 4 - Ext. Trig

This bit reflects the status of the external trigger pin. It is identical to the bit in the ADDSR register.

Bit 3 - Reserved (0)

For compatibility with future products, you must write a 0 to this bit. The results of reading this bit are undefined.

Bit 2 - Reserved (0)

For compatibility with future products, you must write a 0 to this bit. The results of reading this bit are undefined.

Bit 1 - Reserved (1)

For compatibility with future products, you must write a 1 to this bit. The results of reading this bit are undefined.

Bit 0 - Reserved (0)

For compatibility with future products, you must write a 0 to this bit. The results of reading this bit are undefined.

5.2.5. PRESCALER - Clock prescaler register (offset 4)

The register is used to program the Clock prescaler. Before it can be used, the counter must be configured by writing the appropriate mode setting byte to the counter control register, TMRCTR, described later. The counter can be configured either as a binary or BCD counter. Binary mode is almost always used.

The counter can be configured into several operating modes, as discussed in the description of the TMCTR register. Default mode setting is mode 2.

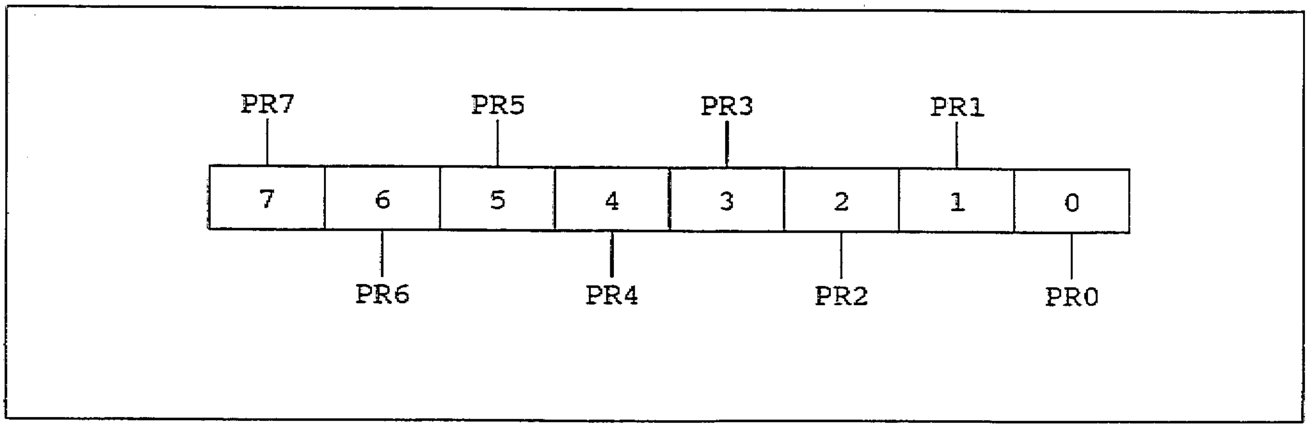

Figure 5.6. Prescaler register.

The input to the prescaler is always the PC's bus clock divided by four.

This register is register 0 (counter 0) of the 8254 on the PC-126 board. The bit layout of the prescaler is shown in figure 5.6.

Bits 7-0 - Prescaler data (PR)

The prescaler register can be configured to write either the high byte of the counter, the low byte of the counter, or both bytes in sequence. The normal configuration is to write both bytes. In this case the LSB is written first, then the MSB.

Note
It is important to always write two bytes to the counter if it is configured for 16-bit operation. Failing to do this can result in invalid data.

5.2.6. DIVIDER - A/D clock divider register (offset 5)

The divider register is used to program the A/D clock divider. Before it can be used, the counter must be configured by writing the appropriate mode setting byte to the counter control register, TMRCTR, described later. The counter can be configured either as a binary or BCD counter. Binary mode is almost always used.

The counter can be configured into several operating modes, as discussed in the description of the TMCTR register. Default mode setting is mode 2.

The input to the clock divider is always the output from the clock prescaler.

This register is register 1 (counter 1) of the 8254 on the PC-126 board. The bit layout of the divider is shown in figure 5.7.

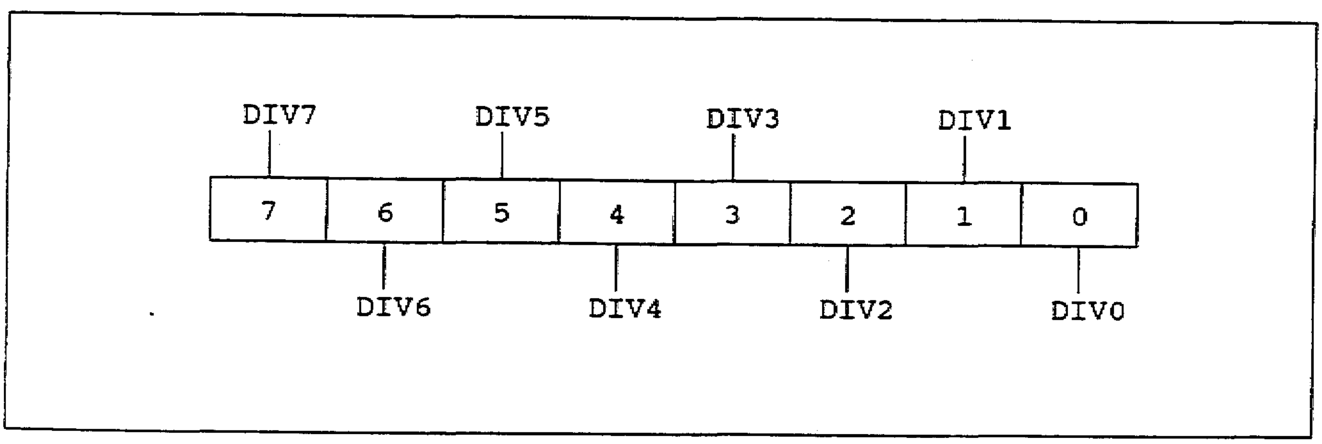

Figure 5.7. A/D clock divider register.

Bits 7-0 - A/D clock divider data (DIV)

The clock divider register can be configured to write either the high byte of the counter, the low byte of the counter, or both bytes in sequence. The normal configuration is to write both bytes. In this case the LSB is written first, then the MSB.

Note:
It is important to always write two bytes to the counter if it is configured for 16-bit operation. Failing to do this can result in invalid data.

5.2.7. USR_CNT - D/A clock divider register (offset 6)

The divider register is used to program the D/A clock divider. Before it can be used, the counter must be configured by writing the appropriate mode setting byte to the counter control register, TMRCTR, described later. The counter can be configured either as a binary or BCD counter. Binary mode is almost always used.

The counter can be configured into several operating modes, as discussed in the description of the TMCTR register. Default mode setting is mode 2.

The input to the clock divider is always the output from the clock prescaler.

This register is register 2 (counter 2) of the 8254 on the PC-126 board. The bit layout of the divider is shown in figure 5.8.

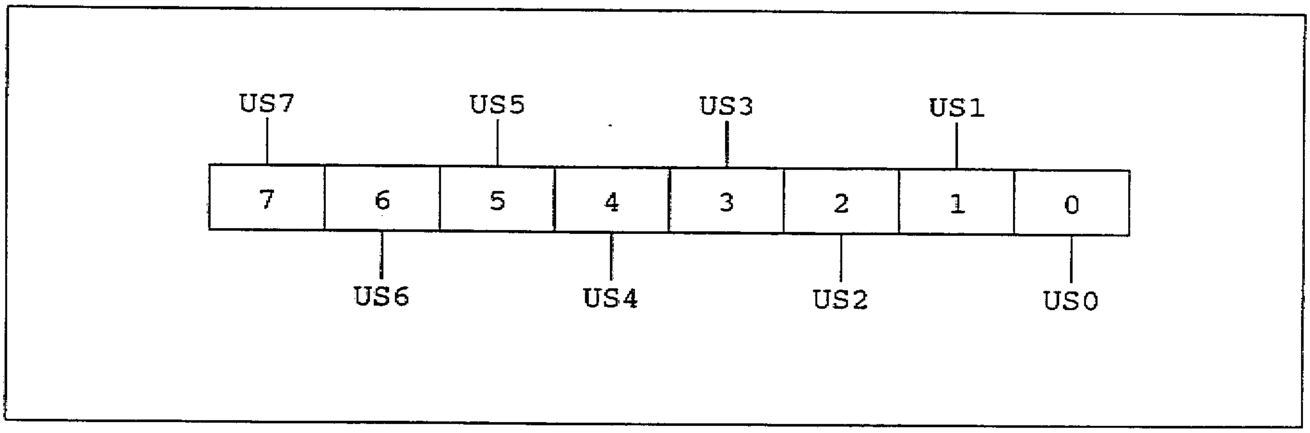

Figure 5.8. D/A divider register.

Bits 7-0 - D/A divider data (US)

The D/A divider register can be configured to write either the high byte of the counter, the low byte of the counter, or both bytes in sequence. The normal configuration is to write both bytes. In this case the LSB is written first, then the MSB.

Note:
It is important to always write two bytes to the counter if it is configured for 16-bit operation. Failing to do this can result in invalid data.

5.2.8. TMRCTR - Timer control register (offset 7)

The timer control register is used to configure the three 16-bit counters on the PC-126 board. It is register 3 (Mode word) of the 8254 on the board. If you intend to program the 8254 extensively, you should obtain a copy of the data sheet for an 8254 type counter/timer.

The register layout is shown in figure 5.9.

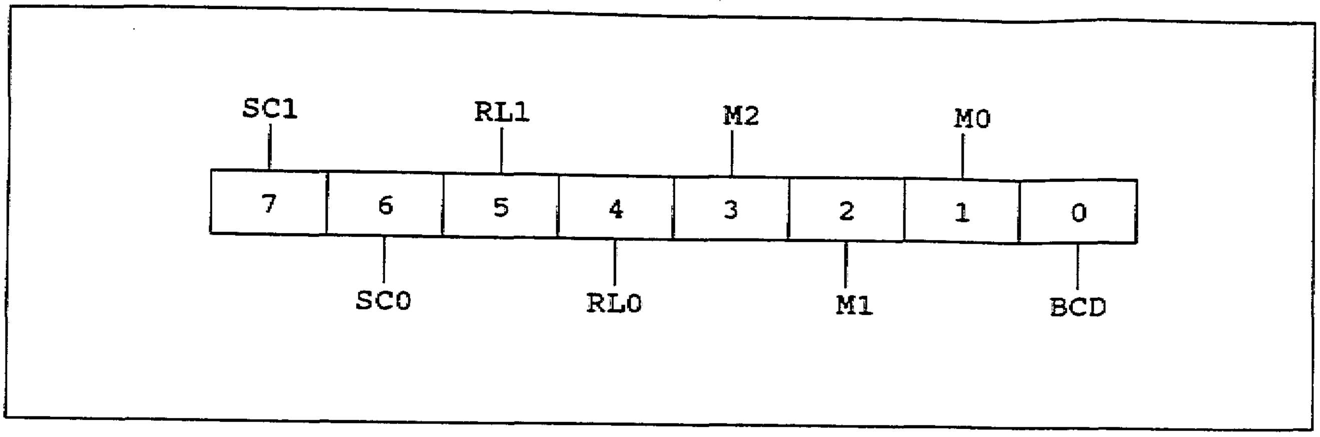

Figure 5.9. Timer controller register.

Bit 7-6 - Select Counter (SC)

These two bits are used to select the counter to be configured. They function as follows:

SC1	SC0	Function
0	0	Select counter 0 (A/D clock prescaler). The rest of the information in the byte written is used to configure the prescaler.
0	1	Select counter 1 (A/D clock divider). The rest of the information in the byte written is used to configure the divider.
1	0	Select counter 2 (User configured counter/timer). The rest of the information in the byte written is used to configure the user counter.
1	1	Reserved; do not use.

Bits 5-4 - Read/load (RL)

Bits 4 and 5 are used to configure how the counter is read and written. The meaning of the various bit combinations is as follows:

RL1	RL0	Function
0	0	Counter latch. The selected counter is latched. This is used to read the contents of a counter while the counter in question's clock is active. If you intend to use this function you should consult the 8254 data sheet for full details.
0	1	Write LSB only. All write operations will write only the LSB (least significant byte) of the selected counter.
1	0	Write MSB only. All write operations will write only the MSB (most significant byte) of the selected counter.
1	1	Write LSB/MSB. Both the LSB and MSB of the counter are written. The LSB is written first, then the MSB. Note that both bytes must always be written. Writing only one byte will cause unpredictable results.

Bits 3-1 - Mode (M)

The counters can be programmed into various modes, as described below. The normal mode of operation for all the counters is mode 2.

Mode bits (M2 M1 M0)	Mode description
000	Mode 0, interrupt on terminal count. After the mode byte is written, the output is low. Once a count value is written, the output remains low until the counter counts down to 0. The output then goes high, and remains high until a new count or mode is written to the counter. The gate input of the counter disables counting when low.
001	Mode 1, programmable one shot. Any rising edge on the clock input to the counter causes the output of the counter to go low for the number of clock cycles programmed into the counter. This mode can be used to generate a pulse of programmable length to external circuitry on each A/D conversion.
010	Mode 2, rate generator. The output of

	the counter goes low for one clock period in every N clocks, where N is the number programmed into the counter. This is the normal mode for the A/D prescaler and clock divider. The gate input of the counter disables counting when low.
011	Mode 3, square wave generator. The output of the counter goes low for N/2 clocks in every N, where N is the number programmed into the counter. The counter hence generates square waves. The gate input of the counter disables counting when low. Note that the minimum value of N is 4.
100	Mode 4, software triggered strobe. After the mode byte or a count value is written, the output is high. The output remains high until the counter counts down to 0. The output then goes low for one clock period. The gate input of the counter disables counting when low.
101	Mode 5, hardware triggered strobe. After the mode byte or a count value is written, the output is high. The counter begins counting down after a rising edge on the gate input. When the count reaches 0, the output goes low for one clock period.

Bit 0 - BCD

If this bit is 0, the counter is configured as a binary counter. If it is 1, the counter is configured as a BCD counter. Note that in either case the counter is a down counter.

5.2.9. DIOP0 - Digital Input port (offset 8)

This register is the digital input port. The layout of the DIOP0 register is shown in figure 5.10.

Bits 7-0 digital Input port (DA)

These bits reflect the digital value on the PC-126's digital input port.

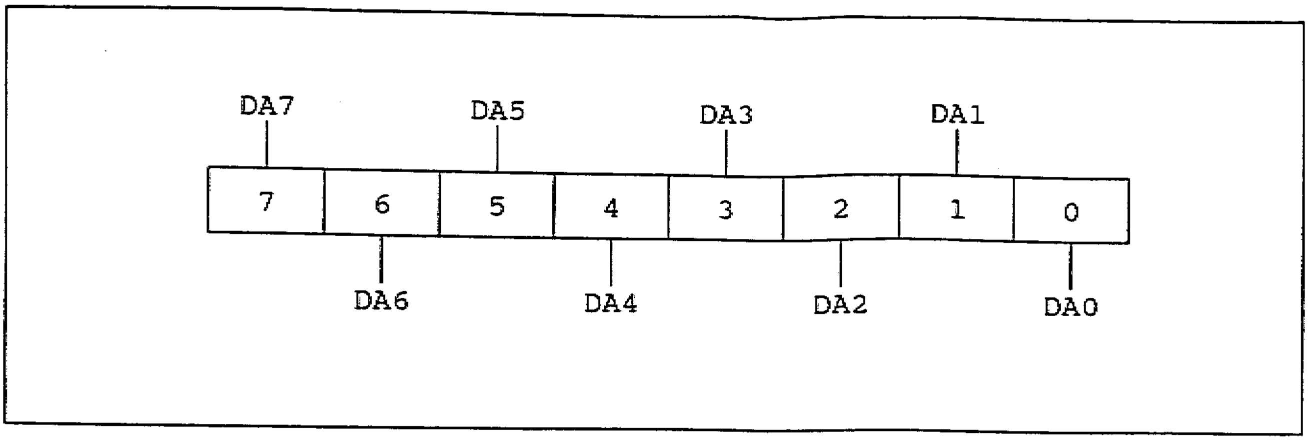

Figure 5.10. Digital input port register.

5.2.10. DIOP1 - Digital Output port (offset 9)

This register is the digital output port. Values written to this register are transferred to the PC-126's digital output lines. The layout of this register is shown in figure 5.11.

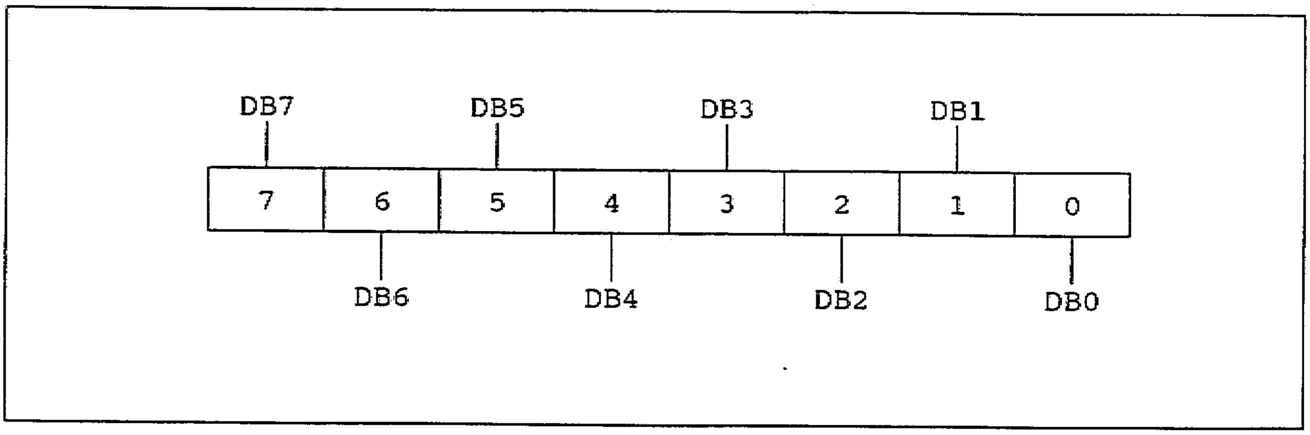

Figure 5.11. Digital output port register.

Bits 7-0 digital Output port (DB)

These bits are the value written to the PC-126's digital outputs.

5.2.11. DADATL0 - DAC0 register (low byte) (offset 12)

This register is used to hold the eight lower bits of the 12-bit code loaded into DAC0 by software for D/A conversions. Data is left justified. Figure 5.14 shows the register layout. Data is transferred to the output when a D/A clock occurs, as discussed in section 2.6.

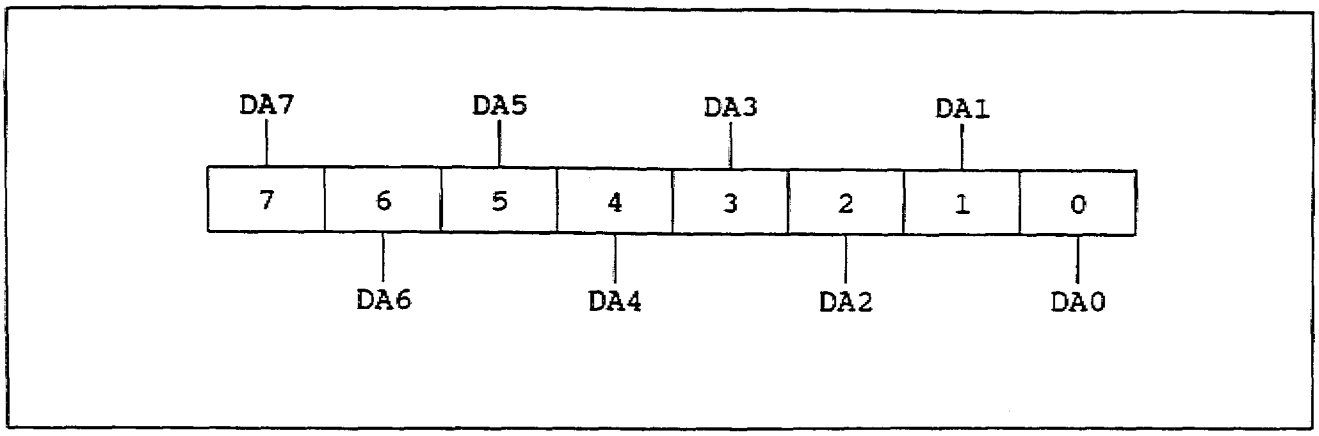

Figure 5.14. DAC0 low byte data register.

Bits 7-0 - DAC0 data (DA)

These bits are the LSB of DAC0 data.

5.2.12. DADATH0 - DAC0 register high byte (offset 13)

DADATH0 high byte holds the four higher bits of the software-loaded 12-bit code for D/A conversion. Bit 3 is the MSB. Data is left justified. Note that changes to this register are not reflected in the output until a D/A clock occurs. The layout of this register is shown in figure 5.15.

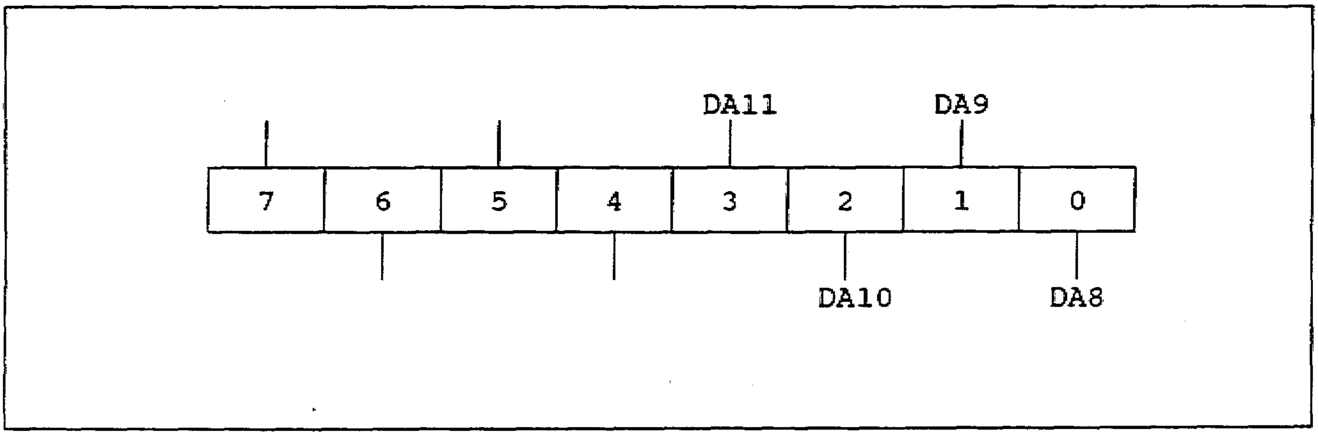

Figure 5.15. DAC0 high byte data register.

Bits 3-0 - DAC0 data (DA)

These four bits are the MSB of the DAC0 data.

Bits 7-4 - Reserved

A value of 0 should be written to these bits.

5.2.13. DADATL1 - DAC1 register (low byte) (offset 14)

This register is used to hold the eight lower bits of the 12-bit code loaded into DAC1 by software for D/A conversions. Data is left justified. Figure 5.16 shows the register layout. Data is transferred to the output when a D/A clock occurs.

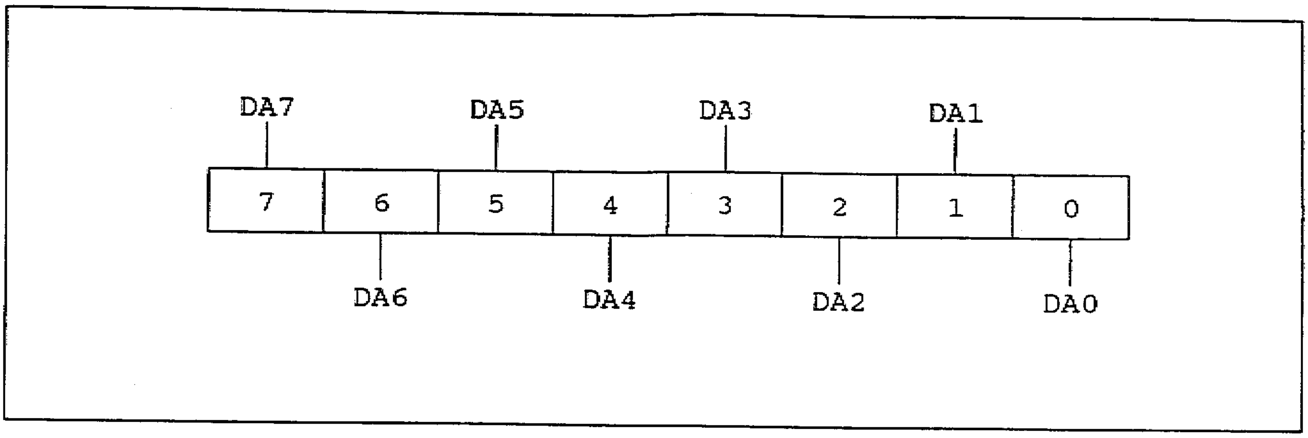

Figure 5.16. DAC1 low byte data register.

Bits 7-0 - DAC1 data (DA)

These bits are the LSB of DAC1 data.

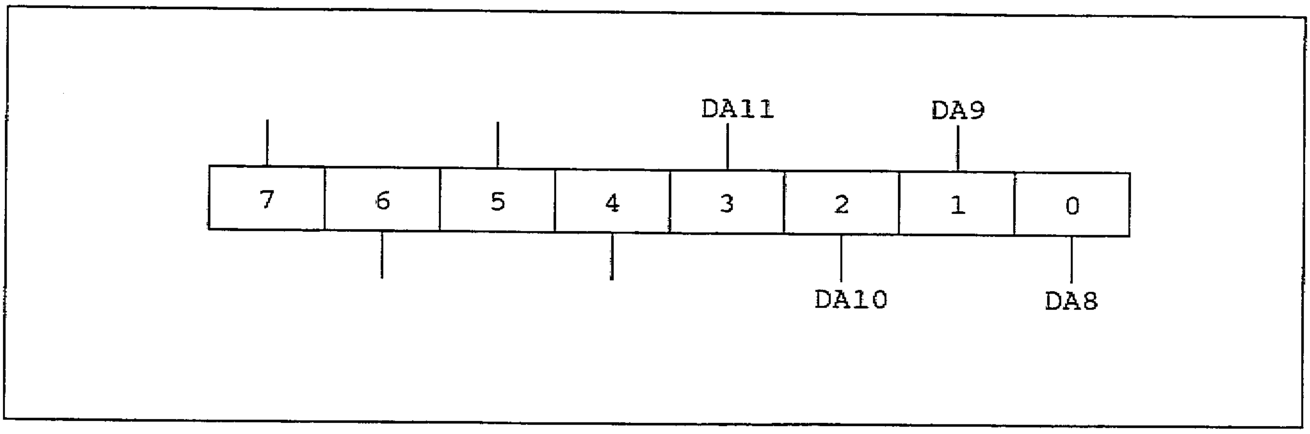

Figure 5.17. DAC1 high byte data register.

5.2.14. DADATH1 - DAC1 register high byte (offset 15)

DADATH1 high byte holds the four higher bits of the software-loaded 12-bit code for D/A conversion. Bit 7 is the MSB. Data is left justified. Note that changes to this register are not reflected in the output until a D/A clock occurs. The layout of this register is shown in figure 5.17.

Bits 3-0 - DAC1 data (DA)

These four bits are the MSB of the DAC1 data.

Bits 7-4 - Reserved

A value of 0 should be written to these bits.

Chapter 6

Programming Guide

This chapter gives a "How To" guide to programming the PC-126. In order to make best use of the contents of this chapter, you should be familiar with the contents of the previous chapter.

Driver software for the PC-126 is available, and where possible you should make use of this software, rather than write your own. However, if you do decide to write your own low-level code, we strongly recommend that you study the source code for the drivers. This code is found in the \SOURCE directory of the driver diskette supplied with the driver software package. When you study this code however, bear in mind that the code is written to support all both the all the PC-30 variants, and all PC-126 variants, including boards not described in this manual.

Where possible, in the following guide there are references to where you can find example code showing how to perform various functions.

6.1. Converting from binary to analog values

Analog data from the A/D converter is always in the form of complementary binary code while data to the D/A converters is offset binary. Analog voltages may be calculated from the digital codes most easily as follows:

6.1.1. A/D converter codes

i. For the 0 to +10V range :

Voltage = (Digital code XOR 800h)(10)/4096

ii. For the -10 to +10V range :

Voltage = ((Digital code XOR 800h) - 2048)(10)/2048

6.1.2. DAC0 and DAC1 converter codes

DAC0 and DAC1 are 12 bit converters. Conversion is as follows :

i. For the 0 to +5V range :

$$\text{Voltage} = (\text{Digital code})(5)/4096$$

ii. For the -5 to +5V range :

$$\text{Voltage} = (\text{Digital code} - 2048)(5)/2048$$

Note:
The above formulas all assume that the PC-126 is calibrated as described in chapter 7. If you do not use the recommended calibration procedure, these formulas may not apply.

6.2. Initialization

In order to initialize the PC-126, the following steps should be performed. The function Init, supplied with the PC-126 driver software, performs this function. This sequence should be followed prior to attempting any function.

i. Write 92(hex) to the A/D mode register (ADMDE).

ii. Write 34(hex) to the counter control register (TMRCTR). This sets the mode of the A/D clock prescaler to 2.

iii. Write 30(hex) to the counter control register (TMRCTR). This sets the mode of the A/D clock divider to 2.

iv. Write B6(hex) to the counter control register (TMRCTR). This sets the mode of the uncommitted counter/timer to 3.

v. Write 02(hex) to the A/D control/channel register (ADCCR). This disables DMA and interrupts, and sets the A/D for software strobes.

vi. Wait at least 100 uS.

vii. Read the high and low byte of the A/D data register.

The PC-126 is then ready for operation.

6.3. Clearing the A/D subsystem

Before using the A/D subsystem, it is important to wait for any current A/D conversion to complete, and to clear any information in the A/D data registers. The sequence below performs this function. The function Clean, supplied with the PC-126 driver software, performs this function. This sequence should be followed prior to attempting any A/D input function.

i. Write 92(hex) to the A/D mode register (ADMDE).

ii. Write 02(hex) to the A/D control/channel register (ADCCR). This disables interrupts, and sets the A/D for software strobes.

iii. Read the high and low byte of the A/D data register.

iv. Wait at least 100 uS, or until the done bit is set.

v. Read the high and low byte of the A/D data register.

6.4. Writing to the D/A converters

In order to write to the D/A converters, the following sequence should be followed.

i. Convert the required voltage to a digital code.

ii. Write this code to the appropriate D/A registers.

iii. Generate a D/A strobe. In order to generate a D/A strobe, assuming that the board is configured for internal clocking, follow the sequence below :

a) Set the D/A clock divider to mode 0. This is done by writing B0(hex) to the TMRCTR register.

b) Write FEFE(hex) to the D/A clock divider. This is done by writing FE(hex) to the USR_CNT register twice.

c) Set the D/A clock divider to mode 1. This is done by writing B2(hex) to the TMRCTR register.

d) Write FEFE(hex) to the D/A clock divider. This is done by writing FE(hex) to the USR_CNT register twice.

e) Set the D/A clock divider to mode 0. This is done by writing B0(hex) to the TMRCTR register.

f) Write FEFE(hex) to the D/A clock divider. This is done by writing FE(hex) to the USR_CNT register twice.

g) This sequence of operations guarantees that a valid D/A clock will be generated, regardless of the initial mode of the D/A clock divider, or the setting of the clock prescaler.

The procedures Da_out and Gen_126_da_clk (in the file PC30S.C) show how to perform the above functions.

6.5. Digital I/O

Digital I/O is performed simply by reading or writing the required digital values to the appropriate registers.

6.6. Obtaining a single A/D reading

To obtain a single A/D reading under program control, proceed as follows:

i. Clear the A/D subsystem as described above.

ii. Write a byte containing the address of the channel you wish to convert, with the STBC bit set, and all other bits cleared, to the ADCCR.

iii. Write the same byte, but with the SSTB bit set as well as the STBC bit, to the ADCCR.

iv. Write the same byte, but with the SSTB bit cleared, to the ADCCR.

v. Wait for the Done bit in the ADDSR to be set.

vi. Read the result from the ADDSR and the ADDATL registers.

6.7. Setting the sample rate

Assuming that the PC-126 is initialized as described above, setting the sampling rate is simple:

i. Decide on values for the clock prescaler and divider. For example, to sample at 10KHz, you could set the prescaler to 20, and the divider to 10 (or vice-versa). Remember that the maximum value for either the prescaler or the divider is FFFF(hex). Also remember that the prescaler value is common to both the A/D and the D/A clocks.

ii. Write the LSB of the prescaler value to the PRESCALER register, then the MSB.

iii. To set the A/D sampling rate, write the LSB of the divider value to the DIVIDER register, then the MSB. To set the D/A sampling rate, write the LSB of the divider value to the USR_CNT register, then the MSB.

The sampling rate is then set. The procedures Ad_prescaler, Da_clock and Ad_clock (in the file PC30S.C) show how to perform the above functions.

6.8. Detecting the end of conversion

When you want to obtain a sequence of samples, detecting when A/D conversions end is very important. For the PC-126, all that is required is to monitor the Done bit in the ADMDE register.

6.9. Obtaining a series of A/D conversions by polled I/O

Polled I/O is by far the simplest way to obtain a sequence of samples. The procedure is as follows:

i. Set the sampling rate, as described above.

ii. Load the channel to be converted into the channel register.

iii. Set the STBC bit in the ADCCR to 0. This enables A/D strobes.

iv. Wait for the A/D conversion to complete. As soon as it is, read the A/D result into memory. How to detect the end of an A/D conversion is discussed above.

v. Repeat step iv until you have collected as many samples as you require.

vi. When the sampling procedure is complete, set the STBC bit to 1.

The procedures S_chan (for single channel operation) and Mb_chan (for multi-channel operations), in the file PC30S.C show how the driver software performs this function.

6.10. Interrupts

Interrupt based I/O allows the PC's CPU to perform other tasks while the PC-126 acquires data. It is however limited to low speed applications. Throughput of about 10KHz is typical. Note that if you intend to write your own interrupt based routines, that you must have a thorough understanding of both the PC and the operating system in use. A complete description of interrupt handlers is well beyond the scope of this manual. However, the basic procedure is described below:

i. Set the sampling rate, as described above.

ii. Load the channel to be converted into the channel register.

iii. Set the PC's interrupt vector to the address of your interrupt handling procedure. This procedure must read in the results of the A/D conversion, as well as halt operations when sufficient samples have been obtained. Remember also that the interrupt handler must send an EOI (end of interrupt) command to the interrupt controller.

iv. Set the interrupt enable bit in the ADCCR to 1. This enables the PC-126 interrupts.

v. Set the STBC bit in the ADCCR to 0. This enables A/D strobes. The program can then continue with other work.

vi. As soon as an A/D conversion completes, control is passed to the interrupt handling procedure. This continues until the interrupt handler disables interrupts.

vii. When the sampling procedure is complete, set the STBC bit to 1, and the interrupt enable bit to 0.

The procedures Mi_chan, Int_chk and Int_close in the file PC30S.C show how the driver software performs this function.

6.11. Generating waveforms from the D/A converters

Waveform generation can easily be done by the PC-126. The procedure is as follows:

i. Set the D/A clock rate, as described above.

ii. Load the first data value into one (or both) D/A converter data registers.

iii. Wait for the D/A ready bit in the ADMDE register to be set.

iv. Write the next data value to the D/A converters(s).

v. Repeat steps iii and iv until the entire waveform has been generated.

The procedure wfm_chan, in the file PC30S.C shows how the driver software performs this function.

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Chapter 7

Calibration

7.1. Introduction

This chapter contains information on the calibration procedures for the A/D subsystem on the PC-126 series of boards.

These procedures should be performed at six month intervals, or whenever the input or output range switches are changed.

NOTE
Allow the host PC and the board to warm up for at least one hour before calibration.

7.2. A/D calibration

A/D calibration is performed by adjusting three trimpots, R5 and R8. These trimpots are easily located from the board layout shown in appendix C, or the labels on the PC-126 board itself.

7.2.1. Requirements

i. Calibration is done on channel 1. The recommended connector wiring is shown in figure 7.1.

ii. Calibration is performed with the board switched into its intended operating mode.

iii. All cables should be as short as possible.

7.2.2. Equipment required

i. Precision voltage source. Range +10 to -10 V, absolute accuracy better than 0.005%,

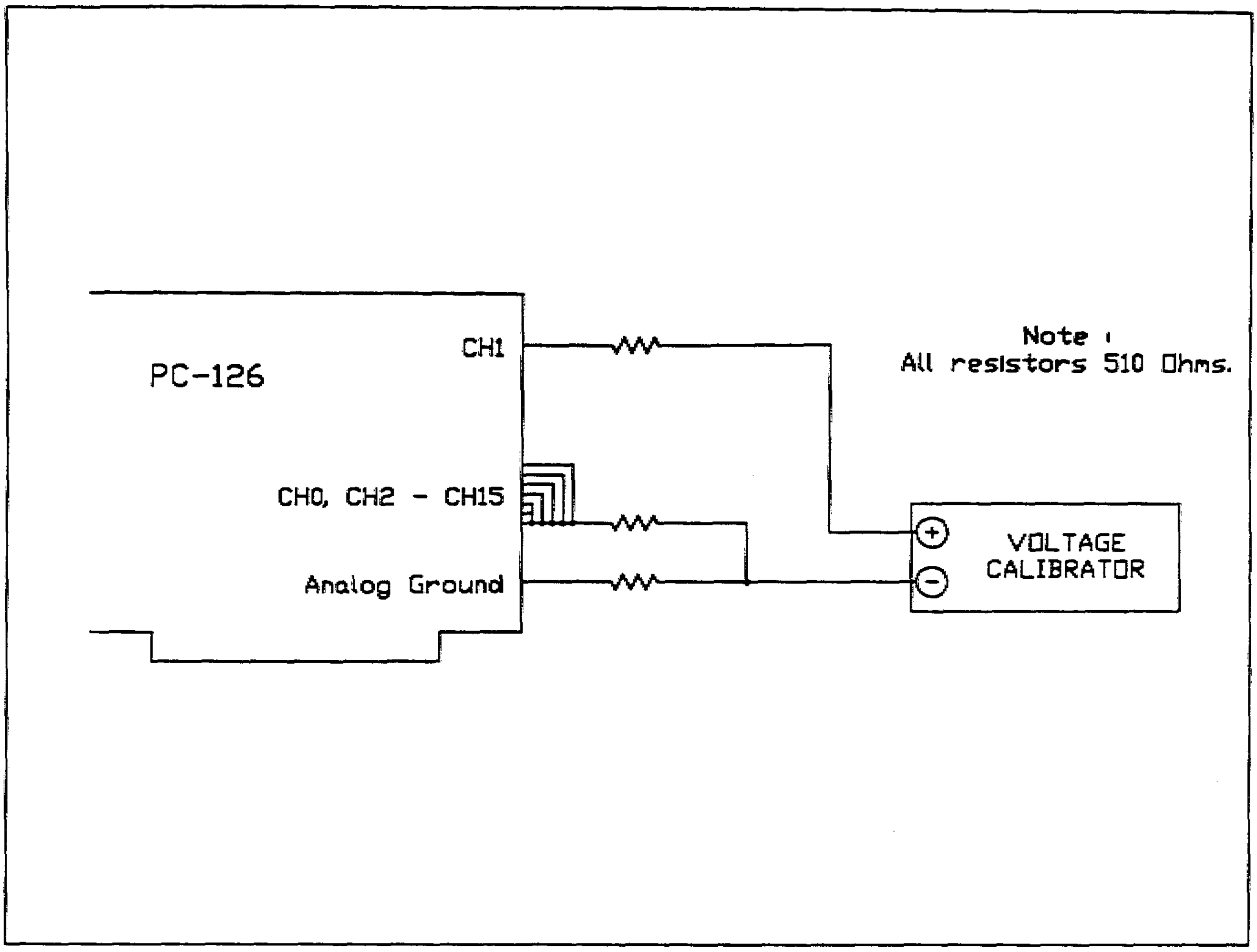

Figure 7.1. A/D calibration connections.

resolution 100 nV or better.

7.2.3. Procedure

7.2.3.1 Unipolar mode

i. Apply (-FS + 1/2 LSB) to channel 1. This is 1.20 mV for the 10 V range. Adjust R5 (A/D offset potentiometer) for an output code which flickers evenly between 000H and 001H.

ii. Apply (+ FS - 3/2 LSB) to channel 1. This is 9.9963 V for the 10 V range. Adjust R8 (gain potentiometer) for an output code which flickers evenly between FFEH and FFFH.

iii. Repeat the above two steps until no further adjustment is required.

7.2.3.2 Bipolar mode

i. Apply (-FS + 1/2 LSB) to channel 1. This is -9.9976V for the -10 to 10V range. Adjust

R5 (A/D offset potentiometer) for an output code which flickers evenly between 000H and 001H.

ii. Apply (+ FS - 3/2 LSB) to channel 1. This is +9.9927V for the -10 to 10V range. Adjust R8 (gain potentiometer) for an output code which flickers evenly between FFEH and FFFH.

iii. Repeat the above two steps until no further adjustment is required.

7.3. A/D calibration Software

The program CAL30.EXE, supplied on the distribution disk, automates the above procedure. Note that for correct operation, the setup information supplied in the first menu must be correct.

7.4. DAC0 and DAC1 calibration

No calibration of either DAC0 or DAC1 is required. Both converters are laser trimmed prior to delivery.

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Appendix A

Hardware Specifications

I. Analog Input

1. Number of Input Channels

16 single-ended

2. Resolution

12-bit, 1 in 4096

3. Total System Accuracy

+- 1.5 LSB

4. Differential Nonlinearity

+- 1 LSB max.

5. Quantization Uncertainty

+-1/2 LSB

6. Input Ranges

0 to +10V, -10 to +10V

7. Input Bias Current

+- 200 nA max

8. Gain Drift

+ - 60 ppm per degree C.

9. Offset Drift

+ - 60 ppm per degree C.

10. Input Impedance

10G/20 pF Off Chan typ.

10G/100 pF On Chan typ.

11. Offset Voltage

+ - 5 LSB, adjustable to zero.

12. Gain Accuracy

+ - 5 LSB, adjustable to zero.

13. Monotonicity

0 to 70 degree C

14. Data acquisition rate

50 KHz max

II. Internal Clock

1. Frequency

2 MHz, crystal controlled

2. Internal clock prescaler

16-bit

3. External clock

TTL compatible

4. External Trigger

TTL compatible, readable via software.

III. A/D clock

1. Clock Source

Internal or external

2. Internal Clock Divider

16-bit

IV. Analog Output

1. Number of Channels

2

2. Resolution

Two 12-bit

3. Relative Accuracy

+ - 1 LSB

4. Differential Nonlinearity

+ - 0.9 LSB

5. Quantization Uncertainty

+ -1/2 LSB

6. Output Ranges

-5 to +5 V, 0 to +5V

7. Offset Error

+ -6 LSB (max)

8. Gain Error

+ -8 LSB (max)

9. Gain Drift

+ - 30 ppm per degree C

10. Offset Drift

+ - 30 ppm per degree C

11. Throughput

50 KHz max.

12. DC Output Impedance

0.5 Ohm (typ)

13. Monotonicity

0 to 70 degree C

V. D/A clock

1. Clock Source

Internal or external

2. Internal Clock Divider

16-bit

VI. Digital I/O

1. Number of Lines

16 in 2 ports (8 input, 8 output)

2. Compatibility

TTL

3. Output Low Voltage

0.5V (I_{sink} = 24 mA)

4. Output High Voltage

3.3V (I_{source} = 2.4 mA)

VII. I/O Connector

50 way IDC connector. User supplied mating connector (3M type 3425-6050) required.

VIII. Environmental

1. Operating Temperature

0 to 70 degrees C

2. Storage Temperature

-55 to 150 degrees C

3. Relative Humidity

5% to 95% noncondensing

IX. PC Interface

1. Base Address

Switch selectable.

2. Number of registers

16 8-bit registers.

3. Interrupts

On end of conversion, software controlled.

X. Power

1. +5V

190mA (min) 212mA (typ) 225mA (max) [without load]

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Appendix B

PC-126 Compatibility

This appendix discusses the compatibility of the PC-126 with the other "30-series" series boards (PC-26, PC-30, PC-39, PC-30B, PC-30C, PC-30D, PC-30DS and PC-30PG).

I. PC-26/PC-30

1. Analog inputs

The analog inputs of the PC-30 had an input impedance of 22K. The PC-126 has an industry standard input impedance of 10G/20pF (off channel) and 10G/100pF (on channel). Series resistors are used to provide fault protection.

NOTE:
Because of the 22K pull down resistors used on the PC-26/PC-30, unused PC-26/PC-30 inputs could be left open. THIS IS NOT POSSIBLE ON THE PC-126. All unused PC-126 analog inputs must be grounded.

2. Interrupt system modifications.

The PC-126's interrupt system has improved relative to the PC-26/PC-30. The effect of these changes is as follows :

i. The PC-26/PC-30 deactivates its interrupt line approximately 10 uS after initiating an interrupt. If the host PC does not respond to the interrupt within this time, then the interrupt is lost. This means that when PC-26/PC-30 interrupts are used, all other interrupts (including the PC's clock) have to be disabled, regardless of the PC-26/PC-30's sampling frequency.

ii. The PC-126 keeps its interrupt line active indefinitely. This means the PC-126 cannot miss interrupts (unless of course an interrupt service routine takes up all the processing time from one PC-126 sample to the next). Hence it is no longer necessary to disable all other interrupts unless the PC-126 is operating at a high enough sample rate that the processing power of the PC becomes too little to handle the PC-126 as well as other interrupts.

iii. This change is invisible to PC-26/PC-30 applications programs which are well behaved. Note however that the missing of interrupts served as a "safety valve" for programs which set the PC-26/PC-30's sampling rate to higher than what the program could process. In that case interrupts which could not be handled were simply lost. As the PC-126 cannot lose interrupts, such programs will now hang up, spending all processing time on interrupts, and never responding to user inputs. Early versions of the PC-26/PC-30 demo program (which allowed the user to set almost any sample rate) suffer from this problem.

3. Data format

The PC-126 makes use of 2's-complement coding, whereas the other PC-30 series boards use offset binary. All that is required is to invert the MSB of ALL A/D data in order to convert between formats.

II. PC-39, PC-30B, PC-30C, PC-30D, PC-30DS, PC-30PG

1. Data format

The PC-126 makes use of 2's-complement coding, whereas the other PC-30 series boards use offset binary. All that is required is to invert the MSB of ALL A/D data in order to convert between formats.

2. Status bit locations

The status bits found in the upper four bits of the ADDSR register of the other PC-30 series boards are now found in the upper four bits of the ADMDE register. Bit positions are identical.

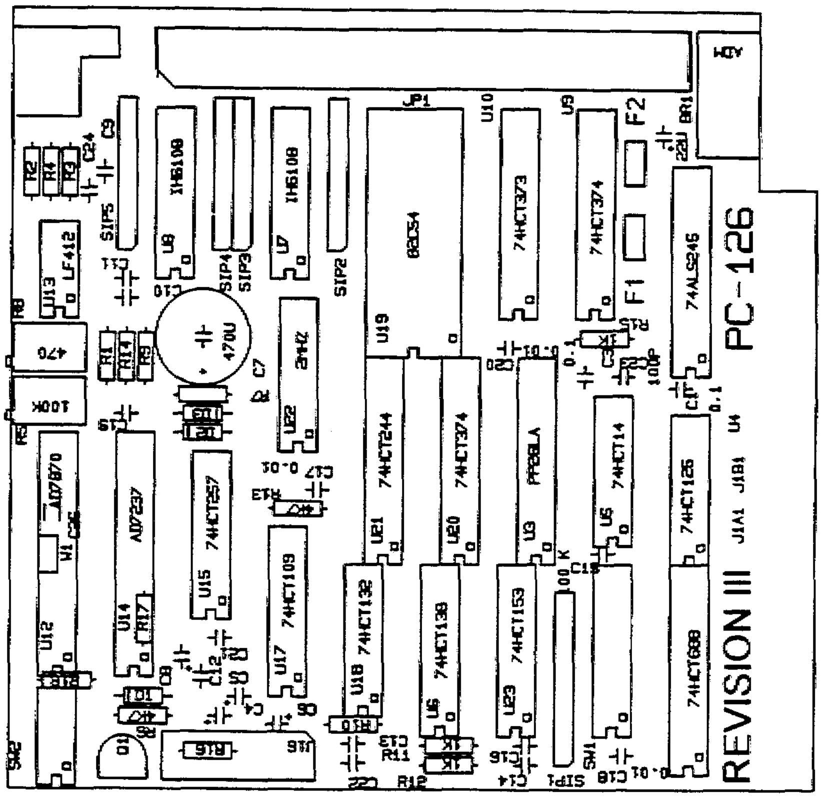
III. PC-126 Revision II

Current revision PC-126 series boards have power supply outputs of +-12V. On revision II boards. this was +-15V.

Appendix C

Layout Diagram

The following page shows the layout diagram of the PC-126.


PC-126
REVISION III

Appendix D

Problem Determination Guide

I. Introduction

If you are experiencing problems, first check the following :

i. Remove the PC-126, and check that all ICs are firmly seated in their sockets, that there is no obvious damage to any components, and that the edge connector fingers on the PC-126 are clean.

ii. Check that the PC-126 is jumpered correctly for your application.

iii. Replace the PC-126, and check that it seats firmly in the host PC's mother-board. Also check that no components are touching an adjacent board.

iv. Check that the cable is securely plugged into the PC-126.

II. The diagnostics function.

The PC-126 contains a very comprehensive diagnostics program. All of the supplied demo programs as well as the calibration program use this, and can be used to diagnose malfunctions on the PC-126. In fact, the only PC-126 malfunctions which it will not detect are the following :

i. Damaged input multiplexer.

ii. Damaged D/A output amplifier.

iii. Damaged digital input or output lines.

III. Common problems

1. PC-126 diagnostics report board not found.

This is typically as a result of incorrect switch settings.

2. A/D output code all zeros or all ones.

This is typically as a result of floating inputs, or an overload.

If you have exceeded the maximum input voltage (+/- 12 V), you may have damaged the input multiplexers. If so, return the board to your dealer for repair.

3. A/D reading are noisy.

This may be as a result of one or more of several reasons:

i. Long leads.

ii. An electrically noisy environment

iii. Overloads on other input channels. Note also that if an input channels is overloaded it may saturate in such a way as to give a reading which appears to be in the normal range, but is very noisy.

iv. Excessive source resistance. The source resistance of the devices connected to the inputs of a PC-126 should not be greater than 10 KOhm.

4. The first reading in a series is inaccurate.

This is normally as a result of an overload on another input, or long leads, or a very high source impedance.

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