

ZT532VXI Specifications

Arbitrary Waveform Generator

16-bit, 400 MS/s, 4 Ch



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Outputs

Channels	4
Low pass Filters	10 MHz, 5-pole Gaussian or Bypass
DAC Digital Filter Bandwidth	-1dB: DC to 65 MHz -3dB: DC to 75 MHz
Analog Bandwidth	>100 MHz measured at 10–90% transition time (Bypass)
Slew Rate	> 500 V/μs (Bypass)
Rise/Fall Time	< 20 ns for 10 Vstep into 50Ω (Bypass) < 4 ns for 2 Vstep into 50Ω (Bypass)
Full-Scale Range	20 mVpp to 20 Vpp into high impedance 10 mVpp to 10 Vpp into 50Ω

Range Accuracy

Range	Accuracy
≤ 19 Vpp into high impedance	±(0.5% + 10 mV)
> 19 Vpp into high impedance	±2%

Range Drift ±50 ppm of Full-Scale per °C

DC Offset Range 0 to ±5V into 50Ω
0 to ±10V into high impedance

Zero DC Offset ±5 mV into high impedance

Offset Accuracy

Offset	Accuracy
offset ≤ 9.5 Vpp into high impedance	±10 mV
offset > 9.5 Vpp into high impedance	±2.5%

Output Limit |V_{amp}+V_{offset}| ≤ 5V into 50Ω
|V_{amp}+V_{offset}| ≤ 10V into high impedance

Note: Output limited by VXI ±12V power supplies.

Maximum Positive Voltage: V_{+12v} - 1.8V

Maximum Negative Voltage: V_{-12v} + 1.8V

Output Impedance 50Ω ± 1%

Connectors BNC

Digital-to-Analog Converter (DAC)

Resolution 16 Bits (0.0015% of Full-Scale)

Record Length 512 kSamples/channel
2 MSamples/channel (Option 1)

Channel Skew < 100 ps difference between channel pairs 1–2 or 3–4
< 300 ps difference between channel pairs 1–3, 1–4, 2–3, or 2–4

Internal DAC Clock

Function Internal DAC Clock generated by Phase Locked Loop

Synchronization All channels pairs have synchronous clock rates

Data Clock Rates 1 kSamples/s to 160 MSamples/s

DAC Clock Rate 1 kSamples/s to 400 MSamples/s

DAC Clock Interpolator 1X, 2X, 4X, or 8X

Clock Resolution 1 kS/s to 10 MS/s: 1, 2.5, 5 steps
10 MS/s to 50 MS/s: 5 MS/s steps
50 MS/s to 100 MS/s: 10 MS/s steps
100 MS/s to 160 MS/s: 20 MS/s steps
Other clock rates programmable, contact factory for details

Clock Reference Internal TCXO, VXIbus Backplane

Internal TCXO ±2.5ppm accuracy

Spectral Purity

	Harmonic	Non Harmonic
+10 dBm Output	≤ -35 dBc	≤ -50 dBc
+20 dBm Output	≤ -30 dBc	≤ -45 dBc

The spectral display graphs on the following page illustrate the purity:

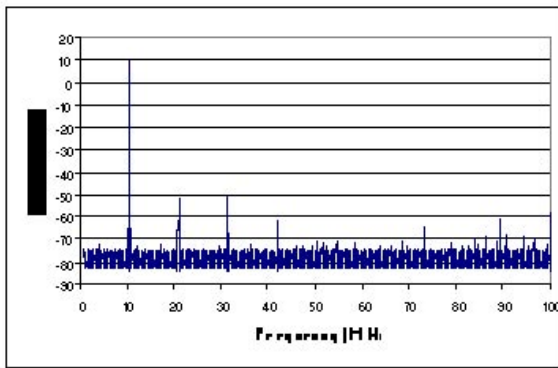


Figure 32: 10.5 MHz at +10 dBm

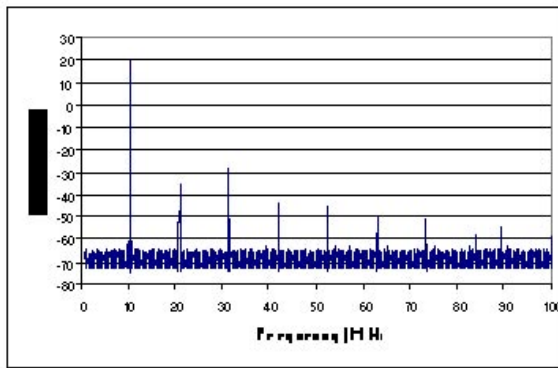


Figure 33: 10.5 MHz at +20 dBm

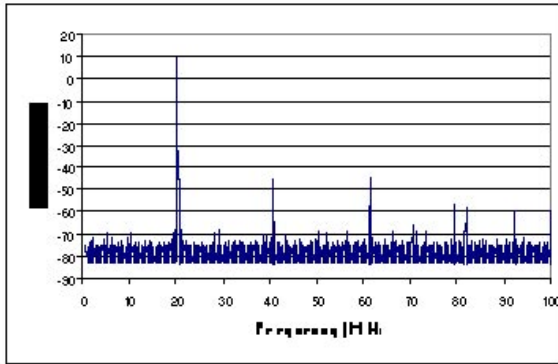


Figure 34: 20.5 MHz at +10 dBm

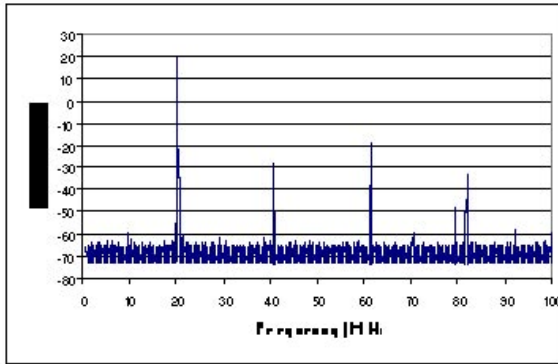


Figure 35: 20.5 MHz at +20 dBm

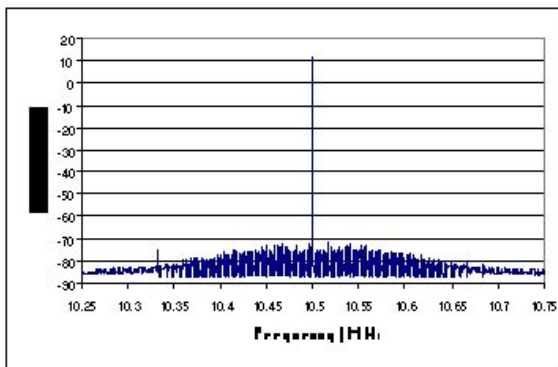


Figure 36: 10.5 MHz at +10 dBm

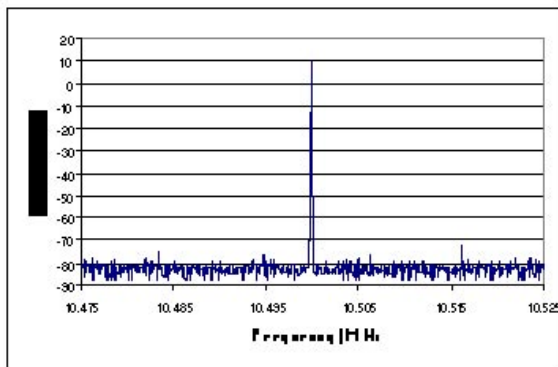


Figure 37: 10.5 MHz at +10 dBm

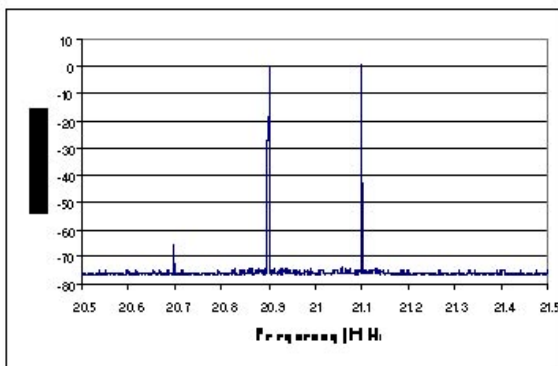


Figure 38: 21 MHz at 0 dBm

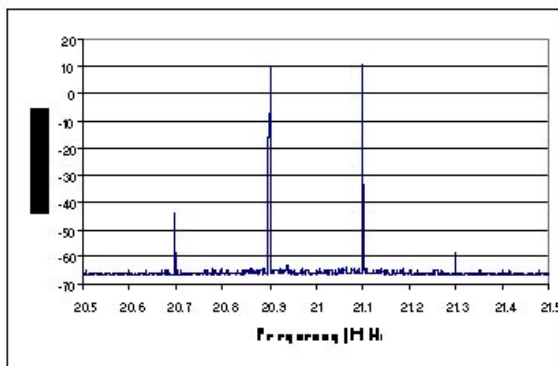


Figure 39: 21 MHz at +10 dBm

External DAC Clock

Function

External DAC Clock bypasses Phase Locked Loop

Synchronization	All four channels synchronized to external clock
Data Clock Rates	1–160 MSamples/s
DAC Clock Rates	1–160 MSamples/s
Maximum Input	$\pm 5V$, no damage
Input Signal Level	500 mVpp to 1 Vpp, sine or square wave
Input Impedance	AC coupled, $50\Omega \pm 2\%$
Connector	BNC

Digital Outputs

Channels	64 (8 bits share connector pins with Sync Outputs)
Time Resolution	6.25 ns to 1 ms (160 MHz to 1 kHz)
Functions	Programmable Pattern Generator
Signal Range	TTL Compatible
Output Loading	± 24 mA Drive Capability
Connectors	Two High-Density 50-Pin Connectors (4 pins on each connector)
Maximum Output Rate	160 Mbits/s or 80 MHz

Sync Outputs

Channels	8 (share connector pins with 8 Digital Output bits)
Time Resolution	6.25 ns to 1 ms (160 MHz to 1 kHz)
Functions	Automatic Waveform Markers or Sync Pulses
Polarity	Programmable high or low pulses
Timing	Programmable location and width (in Data Clock samples)
Repetition	Each segment marker can be programmed independently
Signal Range	TTL Compatible
Output Loading	± 24 mA Drive Capability

Connectors	Two High-Density 50-Pin Connectors (4 pins on each connector)
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Trigger

Trigger Source	External BNC, External 50-pin Connectors, External Arm, ECLTRG0–7, TTLTRG0–7, Software
Trigger Edge	Rising or Falling
Trigger Output	ECLTRG0–1, TTLTRG0–7
Trigger Latency	< (14 DAC Clock Periods + 30 ns)
Trigger Detection Jitter	$\pm\frac{1}{2}$ DAC Clock Period
Trigger Delay	Programmable delay after trigger event before start of waveform
Minimum Delay	0 + Trigger Latency
Maximum Delay	655 seconds + Trigger Latency
Trigger Time Stamp	100 ns resolution, 1 second period

External BNC Trigger Input

Maximum Input	$\pm 5V$, no damage
Threshold Level	$\pm 1V$
Threshold Resolution	0.5 mV
Input Impedance	$50\Omega \pm 2\%$
Connector	BNC

External 50-Pin Trigger Inputs

Maximum Input	0V to 5V, no damage
Nominal Level	TTL Compatible
Input Impedance	10 k Ω
Connector	High-Density 50-Pin Connectors

Arm

Function	Arm to qualify trigger event
Source	External Arm, ECLTRG0–1, TTLTRG0–7, External BNC Trigger, External 50-pin Connectors, Software
Polarity	Positive or Negative

External Arm Input

Maximum Input	0V to 5V, no damage
Nominal Level	TTL Compatible
Input Impedance	1 k Ω pull up to +5V
Connector	BNC

Waveform Sequencing

Sequencing	Channels 1–2 and 3–4 have independent sequencers for modes, waveform sizes and segmentation, but share a common clock.
Sequencing Modes	Normal: output when initiated Triggered: output upon trigger event Qualified-Triggered Segment: output upon trigger event when armed Gated: output when arm active
Waveform Size	8 Samples to 512 k/Samples 8 Samples to 2 M/Samples (Option 1)
Segmentation	1 to 65536 Segments (2M Samples to 8 Samples)
Segment Size	512 kSamples to 8 Samples 2 MSamples to 8 Samples (Option 1)
Sequencing	Continuous Waveform Switching (per Sequence Table)
Sequence Table	Sequence of 1 to 65535 Segment Numbers (with looping)
Segment Repeat	A segment is repeated up to 65536 times before advancing to the next segment in the sequence.
Segment Advance	End of Segment or immediately after Trigger/Gate Event.
Sequence Looping	Infinite, Continuous Sequence

Differential Waveform Synthesis Mode

Analog Waveforms	Differential analog outputs on channel pairs (1–2 or 3–4) Waveform compliment automatically generated for pairs
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Internal Waveform Library

DC

Amplitude $\pm 100\%$ of Maximum Range

Sine

Frequency 2 mHz to 79.9999 MHz

Initial Phase 0 to 360°

Square

Frequency 2 mHz to 80 MHz

Duty Cycle 50%

Initial Phase 0 to 360°

Triangle

Frequency 2 mHz to 10 MHz

Initial Phase 0 to 360°

Sinc: $\sin(x)/x$

Frequency 2 mHz to 10 MHz

Initial Phase 0 to 360°

Pulse

Frequency 2 mHz to 10 MHz

Pulse Width (1 Data Clock cycle) to (Period – 1 Data Clock cycle)

Rise/Fall Time (1 Data Clock cycle) to (Period – 2 Data Clock cycles)

Initial Delay 0 to (Period – 2 Data Clock cycles)

Polarity Normal or Inverted

Ramp

Frequency	2 mHz to 10 MHz
Initial Phase	0 to 360°

Noise

Period	1 μ s to 500s
Noise Type	Uniform White

Multi-Tone

Frequencies	100 Hz to 79.9999 MHz
Minimum Tone Resolution	100 Hz
Number of Tones	1 to 100

AM

Modulation Frequency	1 Hz to 1 MHz
Percent Modulation	0 to 100 percent

FM

Modulation Frequency	1 Hz to 1 MHz
Frequency Deviation	1 Hz to 1 MHz

Digital Patterns

Types	Constant, Up-count, Down-count, Shift Left, Shift Right
Count Parameters	Initial Count, End Count, Step Size
Shift Parameter	Number of Bits

Arbitrary Waveforms

Custom	Sample-by-Sample Synthesis
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Data Interface

VXIbus Connection	Standard P1 and P2 interface
Command Interface	A16 SCPI message-based
Interrupt Operation	Programmable Interrupter, Level 1–7
Data Interface	32 Mbytes, A32 register-based
Manufacturer ID	3712 (E80 ₁₆)
Model Code	532 (214 ₁₆)

VXIbus P2 Trigger and Clock Pin Usage

Pin A1	VXI ECLTRG0	(ECL level bidirectional)
Pin A3	VXI ECLTRG1	(ECL level bidirectional)
Pin A23	VXI TTLTRG0	(TTL level bidirectional)
Pin A24	VXI TTLTRG2	(TTL level bidirectional)
Pin A26	VXI TTLTRG4	(TTL level bidirectional)
Pin A27	VXI TTLTRG6	(TTL level bidirectional)
Pin C1	VXI CLK 10+	(ECL level input)
Pin C2	VXI CLK 10-	(ECL level input)
Pin C23	VXI TTLTRG1	(TTL level bidirectional)
Pin C24	VXI TTLTRG3	(TTL level bidirectional)
Pin C26	VXI TTLTRG5	(TTL level bidirectional)
Pin C27	VXI TTLTRG7	(TTL level bidirectional)

LED Status Indicators

READY Unit has passed power-up self-diagnostics

Toggles when unit has an error pending in the error queue

VXI VXI access occurring or VXIbus MODID asserted

OUT Unit has at least one output on

BUSY Unit is internally busy generating a waveform

Instrument Setup Storage

Reset Non-volatile storage of default instrument setup configuration

Save & Recall Non-volatile storage of 20 instrument setup configurations

Analog Settings Bandwidth, range, offset, output enable, load impedance, idle voltage

Record Settings	Clock rate, clock source, interpolation, waveform size
Sequence Settings	Mode, looping, repeat count
Waveform Settings	Non-arbitrary waveform type, differential mode, auto selection
Sync Settings	source, start, stop, polarity, output enable, idle pattern
Trigger Settings	Source, level, edge, delay, output enable, hold off
Arm Settings	Source, polarity

Physical

Physical Size	Single-wide C-Size VXIbus
Weight	3 lbs.

Power

Cooling	45W maximum cooling required
Power Consumption	45W typical total power required

Voltage	DC Current	Dynamic Current
+24V	0.0A	0.0A
+12V	0.7A	0.3A
+5V	5.4A	0.5A
-24V	0.0A	0.0A
-12V	0.7A	0.3A
-5.2V	0.2A	0.1A
-2V	0.1A	0.1A

Temperature Range

Operating	0 to 40 °C Ambient
Storage	-40 to +75 °C
Calibration Range	20 to 30 °C Ambient, after a 20-minute warm-up period, to meet all calibration specification accuracies

Relative Humidity

Operating or Storage	0 to 95%, non-condensing, up to +40 °C
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Altitude

Operating Up to 15,000 feet

Storage Up to 50,000 feet