

ZT530PCI & PXI Specifications

Arbitrary Waveform Generator

16-bit, 400 MS/s, 2 Ch



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Outputs

Channels	2
Low pass Filters	10 MHz, 5-pole Gaussian or Bypass
DAC Digital Filter	-1dB: DC to 65 MHz
Bandwidth	-3dB: DC to 75 MHz
Analog Bandwidth	>100 MHz measured at 10–90% transition time (Bypass)
Slew Rate	> 500 V/ μ s (Bypass)
Rise/Fall Time	< 20 ns for 10 Vstep into 50 Ω (Bypass) < 4 ns for 2 Vstep into 50 Ω (Bypass)
Full-Scale Range	20 mVpp to 20 Vpp into high impedance 10 mVpp to 10 Vpp into 50 Ω
Output Current	\pm 100 mA maximum

Range Accuracy

Range	Accuracy
≤ 19 Vpp into high impedance	$\pm(0.5\% + 10 \text{ mV})$
> 19 Vpp into high impedance	$\pm 2\%$

Range Drift < ± 50 ppm of Full-Scale per $^{\circ}\text{C}$

DC Offset Range 0 to $\pm 5\text{V}$ into 50 Ω
0 to $\pm 10\text{V}$ into high impedance

Zero DC Offset < ± 5 mV into high impedance

Offset Accuracy

Offset	Accuracy
$ \text{offset} \leq 9.5\text{V}$ into high impedance	$\pm 10 \text{ mV}$
$ \text{offset} > 9.5\text{V}$ into high impedance	$\pm 2.5\%$

Output Limit $|\text{V}_{\text{amp}} + \text{V}_{\text{offset}}| \leq 5\text{V}$ into 50 Ω
 $|\text{V}_{\text{amp}} + \text{V}_{\text{offset}}| \leq 10\text{V}$ into high impedance

Note: Output limited by PXI $\pm 12\text{V}$ power supplies.

Maximum Positive Voltage: $V_{+12\text{v}} - 1.8\text{V}$

Maximum Negative Voltage: $V_{-12\text{v}} + 1.8\text{V}$

Output Impedance 50Ω ± 1%

Connectors SMB

Digital-to-Analog Converter (DAC)

Resolution 16 Bits (0.0015% of Full-Scale)

Record Length 512 kSamples/channel (ZT530-00)
2 MSamples/channel (ZT530-01)

Channel Skew < 200 ps difference between channels at full bandwidth

Internal DAC Clock

Function Internal DAC Clock generated by Phase Locked Loop

Synchronization Channels synchronous at same clock rates

Data Clock Rates 1 kSamples/s to 160 MSamples/s

DAC Clock Rate 1 kSamples/s to 400 MSamples/s

DAC Clock Interpolator 1X, 2X, 4X, or 8X

Clock Resolution 1 kS/s to 10 MS/s: 1, 2.5, 5 steps
10 MS/s to 50 MS/s: 5 MS/s steps
50 MS/s to 100 MS/s: 10 MS/s steps
100 MS/s to 160 MS/s: 20 MS/s steps
Other clock rates programmable, contact factory for details

Clock Reference Internal TCXO, PXIbus Backplane

Internal TCXO ±2.5ppm accuracy

Spectral Purity

	Harmonic	Non Harmonic
+10 dBm Output	-35 dBc	-50 dBc
+20 dBm Output	-30 dBc	-45 dBc

The following spectral display graphs illustrate the spectral purity:

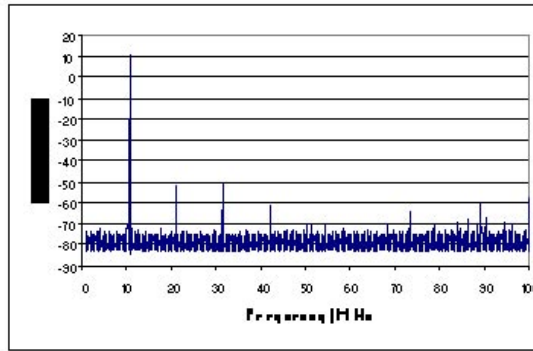


Figure 36: 10.5 MHz at +10 dBm

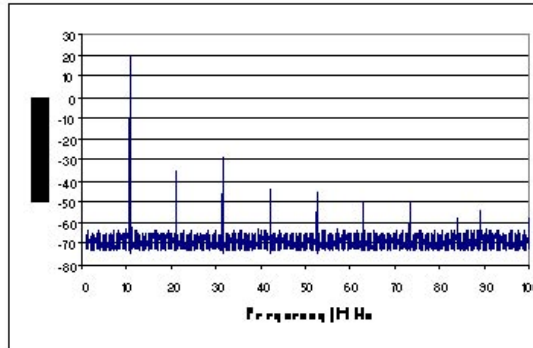


Figure 37: 10.5 MHz at +20 dBm

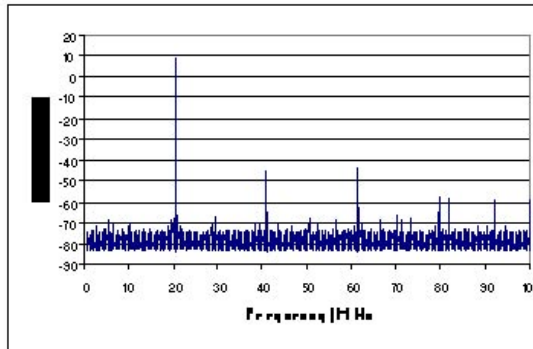


Figure 38: 20.5 MHz at +10 dBm

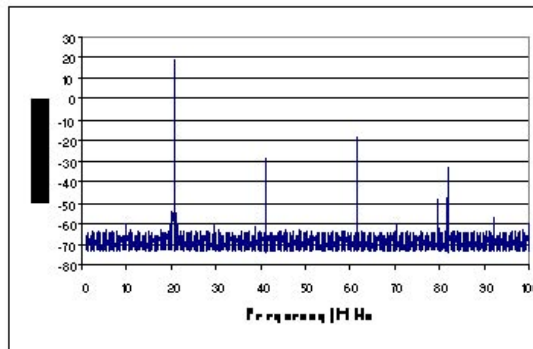


Figure 39: 20.5 MHz at +20 dBm

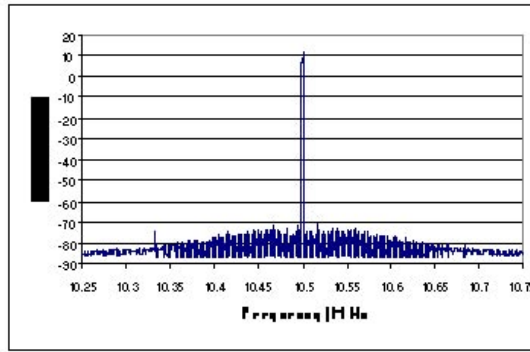


Figure 40: 10.5 MHz at +10 dBm

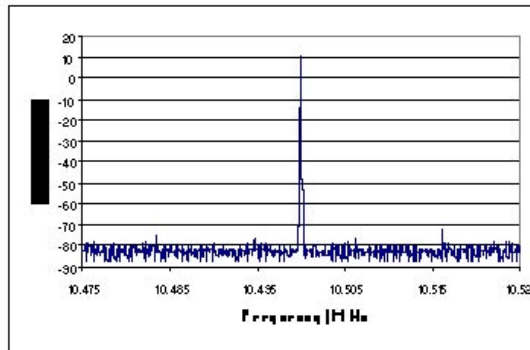


Figure 41: 10.5 MHz at +10 dBm

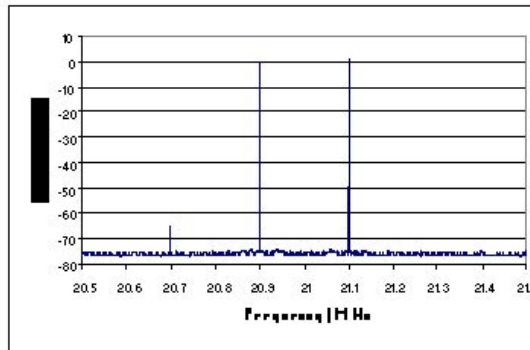


Figure 42: 21 MHz at 0 dBm

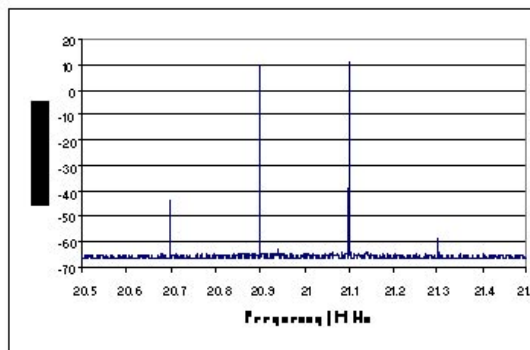


Figure 43: 21 MHz at +10 dBm

External DAC Clock

Function

External DAC Clock bypasses Phase Locked Loop

Synchronization	Both channels synchronized to external clock
Data Clock Rates	1–160 MSamples/s
DAC Clock Rates	1–160 MSamples/s
Maximum Input	±5V, no damage
Input Signal Level	500 mVpp to 1 Vpp, sine or square wave
Input Impedance	AC coupled, 50 Ω ±2%
Connector	SMB

Digital Outputs

Channels	32 (4 bits share connector pins with Sync Outputs)
Time Resolution	6.25 ns to 1 ms (160 MHz to 1 kHz)
Functions	Programmable Pattern Generator
Signal Range	TTL Compatible
Output Loading	±24 mA Drive Capability
Connectors	High-Density 50-Pin Connector
Maximum Output Rate	160 Mbits/s or 80 MHz

Sync Outputs

Channels	4 (share connector pins with 4 Digital Output bits)
Time Resolution	6.25 ns to 1 ms (160 MHz to 1 kHz)
Functions	Automatic Waveform Markers or Sync Pulses
Polarity	Programmable high or low pulses
Timing	Programmable location and width (in Data Clock samples)
Repetition	Each segment marker can be programmed independently

Signal Range	TTL Compatible
Output Loading	±24 mA Drive Capability
Connectors	High-Density 50-Pin Connector

Trigger

Trigger Source	External Trigger, PXI Star Trigger, PXITRG0–7, Software
Trigger Edge	Rising or Falling
Trigger Output	PXITRG0–7
Trigger Latency	< (14 DAC Clock Periods + 30 ns)
Trigger Detection Jitter	±½ DAC Clock Period
Trigger Delay	Programmable delay after trigger event before start of waveform
Minimum Delay	0 + Trigger Latency
Maximum Delay	655 seconds + Trigger Latency
Trigger Time Stamp	100 ns resolution, 1 second period

External Trigger Input

Maximum Input	0 to 5V, no damage
Nominal Level	TTL Compatible
Input Impedance	10 kΩ
Connector	High-Density 50-Pin Connector

Arm

Function	Arm to qualify trigger event
Source	External Trigger, PXI Star Trigger, PXITRG0–7, Software
Polarity	Positive or Negative

Waveform Sequencing

Sequencing Modes	Normal: output when initiated Triggered: output upon trigger event Qualified-Triggered Segment: output upon trigger event when armed Gated: output when arm active
Waveform Size	8 Samples to 512 k/Samples (ZT530-00) 8 Samples to 2 M/Samples (ZT530-01)
Segmentation	1 to 65536 Segments (2M Samples to 8 Samples)
Sequencing	Continuous Waveform Switching (per Sequence Table)
Sequence Table	Sequence of 1 to 65535 Segment Numbers (with looping)
Segment Repeat	A segment is repeated up to 65536 times before advancing to the next segment in the sequence.
Segment Advance	End of Segment or immediately after Trigger/Gate Event.
Sequence Looping	Infinite, Continuous Sequence

Differential Waveform Synthesis Mode

Analog Waveforms	Differential analog outputs on both channel pairs Waveform compliment automatically generated for pairs
Digital Waveforms	Differential pair outputs on alternating digital output pins Pattern compliment automatically generated for pairs

Internal Waveform Library

DC

Amplitude	$\pm 100\%$ of Maximum Range
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Sine

Frequency	2 mHz to 79.9999 MHz
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Initial Phase	0 to 360°
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Square

Frequency 2 mHz to 80 MHz

Duty Cycle 50%

Initial Phase 0 to 360°

Triangle

Frequency 2 mHz to 10 MHz

Initial Phase 0 to 360°

Sinc: $\sin(x)/x$

Frequency 2 mHz to 10 MHz

Initial Phase 0 to 360°

Pulse

Frequency 2 mHz to 10 MHz

Pulse Width (1 Data Clock cycle) to (Period – 1 Data Clock cycle)

Rise/Fall Time (1 Data Clock cycle) to (Period – 2 Data Clock cycles)

Initial Delay 0 to (Period – 2 Data Clock cycles)

Polarity Normal or Inverted

Ramp

Frequency 2 mHz to 10 MHz

Initial Phase 0 to 360°

Noise

Period 1 μ s to 500 s

Noise Type Uniform White

Multi-Tone

Frequencies	100 Hz to 79.9999 MHz
Tone Resolution	100 Hz minimum
Number of Tones	1 to 100

AM

Modulation Frequency	1 Hz to 1 MHz
Percent Modulation	0 to 100 percent

FM

Modulation Frequency	1 Hz to 1 MHz
Frequency Deviation	1 Hz to 1 MHz

Digital Patterns

Types	Constant, Up-count, Down-count, Shift Left, Shift Right
Count Parameters	Initial Count, End Count, Step Size
Shift Parameter	Number of Bits

Arbitrary Waveforms

Custom	Sample-by-Sample Synthesis
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Data Interface

PCI Bus	33 MHz, 32 bit address, 16 bit data
PCI Voltage	Universal, +3.3V or +5V
PCI Compatibility	Version 2.2
PXI Signals	PXI_TRIG0–7 input/output selectable PXI_STAR input 10 MHz reference input Left and right side buses not used
Manufacturer ID	4172 (104C ₁₆)

PXI J2 Trigger and Clock Pin Usage

Pin A16	PXI Trigger 1	(TTL level bidirectional)
Pin A17	PXI Trigger 2	(TTL level bidirectional)
Pin A18	PXI Trigger 3	(TTL level bidirectional)
Pin B16	PXI Trigger 0	(TTL level bidirectional)
Pin B18	PXI Trigger 4	(TTL level bidirectional)
Pin C18	PXI Trigger 5	(TTL level bidirectional)
Pin D17	PXI Star Trigger	(TTL level input)
Pin E16	PXI Trigger 7	(TTL level bidirectional)
Pin E17	PXI CLK10 In	(TTL level input)
Pin E18	PXI Trigger 6	(TTL level bidirectional)

LED Status Indicators

READY	Unit has passed power-up self-diagnostics toggles when unit has an error pending in the error queue
OUT	Unit has at least one output on

Instrument Setup Storage

Reset	Non-volatile storage of default instrument setup configuration
Save & Recall	Non-volatile storage of 31 instrument setup configurations
Analog Settings	Bandwidth, range, offset, output enable, load impedance, idle voltage
Record Settings	Clock rate, clock source, interpolation, waveform size
Sequence Settings	Mode, looping, repeat count
Waveform Settings	Non-arbitrary waveform type, differential mode, auto selection
Sync Settings	source, start, stop, polarity, output enable, idle pattern
Trigger Settings	Source, level, edge, delay, output enable, hold off
Arm Settings	Source, polarity

Physical

Physical Size 3U, single slot, cPCI/PXI Module (PXI)
Single-Slot Short PCI Card (PCI)

Weight 11.2 oz.

DC Power

Cooling & Power Consumption

Product Option	Typical Cooling & Power	Maximum Cooling & Power
ZT530-00	13.1 W	18.8 W
ZT530-01	13.7 W	19.4 W

Note: Optional PCI Cooling Fan adds 0.12A to +5VDC current requirements and 0.6W to total power consumption.

Power Supplies

Product Option	Voltage	Typical Current	Maximum Current
ZT530-00	+3.3V	1.7A	1.9A
	+5V	0.05A	0.1A
	+12V	0.3A	0.5A
	-12V	0.3A	0.5A
ZT530-01	+3.3V	1.9A	2.1A
	+5V	0.05A	0.1A
	+12V	0.3A	0.5A
	-12V	0.3A	0.5A

Temperature Range

Operating 0 to 40 °C Ambient

Storage -40 to +75 °C

Over-Temp Protection Automatic shutdown if internal temperature exceeds +55 °C (PCI)

Calibration Range 20 to 30 °C Ambient, after a 20 minute warm-up period, to meet all calibration specification accuracies

Relative Humidity

Operating or Storage 10 to 90%, non-condensing, up to +40 °C

Altitude

Operating	Up to 2,000 m
Storage	Up to 15,000 m

Safety

This product is designed to meet the requirements of the following standard of safety for electrical equipment for measurement, control and laboratory use:

EN 61010-1

Electromagnetic Compatibility

CE Marking EN 61326-1:1997 with A1:1998 and A2:2001 Compliant
FCC Part 15 (Class A) Compliant

Emissions

EN 55011	Radiated Emissions, ISM Group 1, Class A, distance 10 m, emissions < 1 GHz
EN 55011	Conducted Emissions, Class A, emissions < 30 MHz

Immunity

EN 61000-4-2	Electrostatic Discharge (ESD), 4 kV by Contact, 8 kV by Air
EN 61000-4-3	RF Radiated Susceptibility, 10 V/m
EN 61000-4-4	Electrical Fast Transient Burst (EFTB), 2 kV AC Power Lines
EN 61000-4-5	Surge
EN 61000-4-6	Conducted Immunity
EN 61000-4-8	Power Frequency Magnetic Field, 30 A/m
EN 61000-4-11	Voltage Dips and Interrupts

CE Compliance

This product meets the necessary requirements of applicable European Directives for CE Marking as follows:

73/23/EEC	Low Voltage Directive (Safety)
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See Declaration of Conformity for this product for additional regulatory compliance information.