

M-Class Waveform Generator Specifications

PCI, PXI, VXI, & LXI

ZT5210 Series: 14-bit, 200 MS/s, 50 MHz, 2 or 4 Channels



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Outputs

Channels	2 (ZT5211) 4 (ZT5212)
Analog Bandwidth	DC to 10 MHz (± 0.1 dB passband flatness) DC to 25 MHz (-1 dB bandwidth) DC to 50 MHz (-3 dB bandwidth)
Lowpass Filters	50 MHz, 5-pole Bessel 10 MHz, 5-pole Bessel 1 MHz, 5-pole Bessel 100 kHz, 5-pole Bessel
Slew Rate ¹	> 2000 V/ μ s into 50Ω (50 MHz Filter)
Rise/Fall Time	< 7 ns for 10V step into 50Ω (50 MHz Filter)
Range Adjust ²	15 mVpp to 28 Vpp into high impedance 7.5 mVpp to 14 Vpp into 50Ω Range independently adjustable for each channel
DC Offset Adjust	0 to ± 7 V into 50Ω 0 to ± 14 V into high impedance
Output Voltage Limit ³	$ V_{amp} + V_{offset} \leq 7$ V into 50Ω $ V_{amp} + V_{offset} \leq 14$ V into high impedance
Output Current Limit	± 140 mA recommended operating maximum ± 350 mA short circuit maximum
Range Resolution ⁴	0.5 mVpp
Range Accuracy ⁴	$< \pm(0.5\%$ of Range + 10 mVpp) at 25 °C ambient
Range Drift ⁴	$< \pm 1.5$ mVpp per °C
DC Offset Resolution ⁴	0.5 mV
DC Offset Accuracy ⁴	$< \pm(0.5\%$ of Offset Setting + 2 mV) at 25 °C ambient
DC Offset Drift ⁴	$< \pm 75$ μ V per °C
Output Impedance	50Ω typical

¹ Harmonic distortion increases for Range-Bandwidth combination above 400 Vpp-MHz

² Full-scale range adjustment preserves function generator 14-bit DAC resolution and dynamic range

³ $V_{amp} = \text{range}/2$, $V_{offset} = \text{DC offset}$

⁴ Resolution, accuracy & drift specifications shown for high-impedance load, divide specifications by 2 for 50Ω load

Digital-to-Analog Converter (DAC)

DAC Resolution 14 Bits (0.0061% of Full-Scale Range)

Range (Vpp) high impedance/no load	Range (Vpp) 50 Ω load	DAC resolution
28.0 – 1.0	14.0 – 0.5	14 bits
0.9995 – 0.5	0.4995 – 0.25	13 bits
0.4995 – 0.25	0.2495 – 0.125	12 bits
0.2495 – 0.125	0.1245 – 0.0625	11 bits
0.1245 – 0.0625	0.062 – 0.031	10 bits
0.062 – 0.031	0.0305 – 0.0155	9 bits
0.0305 – 0.015	0.015 – 0.0075	8 bits

Waveform Length 4 Samples to 32 MSamples/channel

DAC Clock DAC sample clocks generated by Direct Digital Synthesizers
All channels have independent or common DAC sample clocks

DAC Clock Rates 200 Samples/s to 200 MSamples/s

DAC Clock Resolution < 0.01 ppm or > 8 digits (i.e. 0.116 Hz from 20 MS/s to 200 MS/s)

DAC Clock Sweep Swept DAC clock rate, linear or log sweep
See Sweep Mode for additional details

DAC Clock Output External Output: 100 Hz to 100 MHz common clock source

DAC Clock Jitter < 20 ps

Timebase Reference 10 MHz

Timebase Reference Source Internal TCXO, External Input, Backplane (PXI, VXI),
Timing Expansion Connector (PCI)

Internal TCXO Timebase ± 2.5 ppm accuracy

Timebase Output External Output, Timing Expansion Connector Reference I/O (PCI)

Channel-to-Channel Skew < 500 ps difference between channels (50 MHz Filter)

Channel-to-Channel Isolation ≥ 60 dB

RMS Noise (with DAC clock above filter cutoff) ≤ 1 mV into 50 Ω (50 MHz Filter)

Spectral Purity (sine)

Output Level	Output Frequency	Harmonic	Non Harmonic
≤ +20 dBm	100 kHz	< -73 dBc	< -52 dBc
	20 MHz	< -50 dBc	< -52 dBc
	50 MHz	< -38 dBc	< -52 dBc
> +20 dBm	100 kHz	< -70 dBc	< -52 dBc
	20 MHz	< -30 dBc	< -52 dBc
	50 MHz	< -20 dBc	< -52 dBc

Operation Modes

Continuous Mode

Functionality Generate output continuously when initiated

Burst Mode

Functionality Generate a discrete number on cycles upon trigger event

Number of Cycles 1 to 65535, programmable
A cycle is one waveform period or one waveform sequence

Binary Modulation Mode

Functionality Toggle between two preloaded waveforms based upon modulation state,
Two unique waveforms preloaded into memory,
Enables Amplitude, Phase, Frequency Shift Keying, or Gated Output

Modulation Source External Input, Bus Trigger 0-7, Star Trigger (PXI),
ECL Trigger 0-1 (VXI), Internal Trigger, Software

Sweep Mode

Functionality Sweeps DAC clock rate for swept frequency of output signal
Programmable start frequency & stop frequency
Programmable up, down, or up & down modes

Sweep Types Linear or logarithmic sweep

Sweep Range 1000:1 maximum sweep frequency range (start-to-stop ratio)

Sweep Time 1 ms to 100 s sweep time programmable, 1μs resolution

Trigger

Trigger Source External Input, Bus Trigger 0-7, Star Trigger (PXI), ECL Trigger 0-1 (VXI) Pattern, Internal Trigger, Software

Edge Trigger Mode	Rising or falling edge
Pattern Trigger Mode	Pattern match true or false
Pattern Sources	External Input, Bus Trigger 0-7, Star Trigger (PXI), ECL Trigger 0-1 (VXI)
Trigger Latency	< (20 DAC clock periods + 100 ns)
Trigger Detection Jitter	$\pm\frac{1}{2}$ DAC clock period
Trigger Delay	Programmable delay after trigger event before start of waveform 0 to 6.5535 ms programmable, 100 ns resolution
Internal Trigger	Programmable internal trigger source, 10 μ s to 100 s period, 100 ns resolution
Trigger Timestamp	Captures trigger event time, 1 second wrap period, 100 ns resolution

Arm

Functionality	Arm to qualify trigger event
Source	External Input, Bus Trigger 0-7, Star Trigger (PXI), ECL Trigger 0-1 (VXI), Software
Polarity	Positive or Negative

External Input

Functionality	External Trigger, External 10 MHz Timebase Reference, External Arm, or External Modulation Input
Maximum Input	± 5 V (DC + peak AC), CAT I
Threshold Adjustment	± 2 V
Threshold Accuracy	± 20 mV
Threshold Resolution	0.5 mV
Input Impedance	1 M Ω 30 pF or 50 Ω
Impedance Accuracy	$\pm 2\%$
Input Bandwidth	300 MHz typical 250 MHz minimum

Input Hysteresis	20 mV (overdrive required)
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Connector	BNC (VXI, LXI) SMB (PCI, PXI)
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Sync Outputs

Channels	2 (ZT5211) 4 (ZT5212)
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Outputs	External Output, Bus Trigger 0-7, ECL Trigger 0-1 (VXI) Timing Expansion Connector I/O (PCI)
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Time Resolution	5 ns to 500 μ s (200 MHz to 2 kHz) Synchronized to DAC clock
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Polarity	Programmable high or low pulses
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Timing	Programmable location and width (in DAC clock samples)
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External Output

Output Source	SYNC1-2, SYNC3-4 (ZT5212), Arm Event, Trigger Event, Generation Complete, Operation Complete, Master Status Event, Constant Level, Timebase Reference Clock, Common DAC Clock/2, Programmable Clock, Programmable Pulse
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Output Level	TTL Compatible into High Impedance ($\geq 200 \Omega$) ± 24 mA Output Drive Capability
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Output Enable	Tri-State Output Capability
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Programmable Clock	Clock Period: 26.667 ns to 100 seconds 50% Duty Cycle
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Programmable Pulse	Pulse Repetition Interval: 50 ns to 100 seconds Pulse Width: 26.667 ns
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DAC Clock	Half the common DAC sample clock: 100 Hz to 100 MHz
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Programmable Width	Programmable active pulse width upon event for: Arm, Trigger, Generation Complete, Operation Complete, Master Status 20 ns to 163.83 ms, 10 ns resolution
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Connector	BNC (VXI, LXI) SMB (PCI, PXI)
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Event Outputs

Functionality	Event Output Signals
Outputs	Bus Trigger 0-7, ECL Trigger 0-1 (VXI) Timing Expansion Connector (PCI)
Source	SYNC1-2, SYNC3-4 (ZT5212), Arm Event, Trigger Event, Generation Complete, Operation Complete, Master Status Event, Constant Level
Programmable Width	Programmable active pulse width upon event for: Arm, Trigger, Generation Complete, Operation Complete, Master Status 20 ns to 163.83 ms, 10 ns resolution

Standard Functions

Sine

Frequency	0.001 Hz to 50 MHz
Initial Phase	0 to 360°

Square

Frequency	0.001 Hz to 20 MHz
Duty Cycle	0 to 100%
Initial Phase	0 to 360°

Triangle

Frequency	0.001 Hz to 20 MHz
Initial Phase	0 to 360°

Ramp (sawtooth)

Frequency	0.001 Hz to 20 MHz
Initial Phase	0 to 360°
Shape	Ramp Up or Down

DC

Amplitude	±100% of Maximum Range
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Haversine

Frequency 0.001 Hz to 50 MHz

Initial Phase 0 to 360°

Havercosine

Frequency 0.001 Hz to 50 MHz

Initial Phase 0 to 360°

Half Cycle Sine

Frequency 0.001 Hz to 50 MHz

Initial Phase 0 to 360°

Pulse

Frequency 0.001 Hz to 20 MHz

Pulse Width 0 to (Period – 1 Data Clock cycle)

Rise/Fall Time (1 Data Clock cycle) to (Period – 2 Data Clock cycles)

Initial Delay 0 to (Period – 2 Data Clock cycles)

Sinc Pulse

Frequency 0.001 Hz to 50 MHz

Sinc Frequency Frequency to 50 MHz

Initial Phase 0 to 360°

Gaussian Pulse

Frequency 0.001 Hz to 20 MHz

Standard Deviation (1 Data Clock cycle) to (Period/2)

Initial Phase 0 to 360°

Lorentz Pulse

Frequency 0.001 Hz to 50 MHz

Half Width	(1 Data Clock cycle) to (Period/2)
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Initial Phase	0 to 360°
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Noise

Period	1 μ s to 1000 s
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Noise Type	Uniform White
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AM

Center Frequency	100 Hz to 50 MHz
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Modulation Source	Internal
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Modulation Frequency	1 Hz to smaller of 1 MHz or Center Frequency
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Modulation Depth	0 to 100 percent
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Modulation Shape	Sine, Square, Triangle, Ramp Up, Ramp Down
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FM

Center Frequency	100 Hz to 50 MHz
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Modulation Source	Internal
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Modulation Frequency	1 Hz to smaller of 1 MHz or Center Frequency
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Frequency Deviation	1 Hz to smaller of 1 MHz or Center Frequency
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Modulation Shape	Sine, Square, Triangle, Ramp Up, Ramp Down
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Multi-Tone

Frequencies	100 Hz to 50 MHz
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Tone Resolution	100 Hz minimum
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Number of Tones	1 to 16
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Serial Data

Bit Rate Frequency	0.001 Hz to 20 MHz
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Word Length	4 to 64-bits
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Arbitrary Waveforms

Functionality DAC Sample-by-Sample Arbitrary Waveform Synthesis

Waveform Sequences

Sequence Predefines up to 8 sequences of arbitrary waveforms
2 to 4,096 waveform stages in sequence
Each waveform repeated 1 to 65535 times within stage
Waveforms stages from waveform library and reference channels
Each waveform stage has unique waveform handle and loop number
Amplitude, offset and DAC sample rate apply to entire sequence

Waveform Library Predefines a set of arbitrary waveforms
Up to 4,096 waveforms in waveform library
Total arbitrary waveform library memory limited to 8 MSamples (16 MB)

Reference Channels Predefines a set of non-volatile arbitrary waveforms
Quantity 4 reference waveforms
Each reference waveform limited to 32 KSamples (64 KB)

Waveform Operations

Upload Waveform memory written by host
Ping-pong buffers enable upload during active waveform generation

Download Waveform memory read by host

Copy Waveform memory copied from one location or type to another

Invert Waveform DAC codes inverted (2s compliment)

Scale Waveform DAC codes linearly adjusted by scale factor

Waveform Data Formats 16-bit signed integer, 32-bit floating point real number
Intel or Motorola Byte Order

Instrument Setup Storage

Reset Non-volatile storage of default instrument setup configuration

Undo Returns to previous state prior to reset or recall command

Save & Recall Non-volatile storage of 14 instrument setup configurations

Initial Power-On State	Configurable power-on condition to any valid saved instrument state State 0 initializes to factory default power-on condition
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Status Reporting

IEEE-488.2 Device Status	Reporting Structure including Status Byte, Standard Event Registers, Questionable Registers, Operation Registers
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PCI/PXI Data Interface

PCI Bus	33 MHz, 32 bit
PCI Data Transfer Rate	132 Mbyte/s burst, up to 120 Mbyte/s sustained ⁵
PCI Voltage	Universal, +3.3V or +5V
PCI Compatibility	Version 2.2
PXI Compatibility	PXI Standard Slot and PXI Express Hybrid Slot Compatible
PXI Signals (XJ4 connector)	PXI_TRIG0-7 input/output selectable PXI_STAR input 10 MHz reference input Left and right side buses not used
Primary ID	3712 (0E80 ₁₆)
Secondary ID	ZT5211: 5211 (145B ₁₆) ZT5212: 5212 (145C ₁₆)

VXI Data Interface

Command Interface	A16 message-based servant, SCPI compatible
Interrupt Operation	Programmable interrupter, Level 1–7
Data Interface	A16 register-based DMA D32 or D16 data transfer
Manufacturer ID	3712 (0E80 ₁₆)
Secondary ID	521 (209 ₁₆)

LXI Data Interface

Command Interface	LAN 10/100, USB 2.0 Full-Speed 12 MB/s, SCPI compatible
Manufacturer ID	3712 (0E80 ₁₆)
Secondary ID	521 (209 ₁₆)

PXI XJ4 Trigger & Clock Pin Usage

Pin A5	PXI Trigger 3	(TTL level bi-directional)
Pin A6	PXI Trigger 2	(TTL level bi-directional)
Pin A7	PXI Trigger 1	(TTL level bi-directional)
Pin B5	PXI Trigger 4	(TTL level bi-directional)
Pin B7	PXI Trigger 0	(TTL level bi-directional)
Pin C5	PXI Trigger 5	(TTL level bi-directional)
Pin D6	PXI Star Trigger	(TTL level input)
Pin E5	PXI Trigger 6	(TTL level bi-directional)
Pin E6	PXI CLK10	(TTL level input)
Pin E7	PXI Trigger 7	(TTL level bi-directional)

PCI Timing Expansion Connector Pin Usage

Pin 1	Reference	(TTL level bi-directional)
Pin 3	Star Trigger	(TTL level bi-directional)
Pin 5	Trigger 7	(TTL level bi-directional)
Pin 7	Trigger 6	(TTL level bi-directional)
Pin 9	Trigger 5	(TTL level bi-directional)

5 Sustained transfer rates are dependent upon host system configuration.

Pin 11	Trigger 4	(TTL level bi-directional)
Pin 13	Trigger 3	(TTL level bi-directional)
Pin 15	Trigger 2	(TTL level bi-directional)
Pin 17	Trigger 1	(TTL level bi-directional)
Pin 19	Trigger 0	(TTL level bi-directional)

VXIbus P2 Trigger & Clock Pin Usage

Pin A1	ECLTRG0	(ECL level bi-directional)
Pin A3	ECLTRG1	(ECL level bi-directional)
Pin A23	TTLTRG0*	(TTL level bi-directional)
Pin A24	TTLTRG2*	(TTL level bi-directional)
Pin A26	TTLTRG4*	(TTL level bi-directional)
Pin A27	TTLTRG6*	(TTL level bi-directional)
Pin C1	CLK10+	(ECL level input)
Pin C2	CLK10-	(ECL level input)
Pin C23	TTLTRG1*	(TTL level bi-directional)
Pin C24	TTLTRG3*	(TTL level bi-directional)
Pin C26	TTLTRG5*	(TTL level bi-directional)
Pin C27	TTLTRG7*	(TTL level bi-directional)

LED Indicators

READY	OFF: Hardware failure
ON: Unit has passed power-up self-diagnostics	TOGGLE: unit has an error pending in error queue
HOST or LAN	OFF: Interface fault
	ON: Normal interface operation
	TOGGLE: device identify command received

TRG	OFF: trigger event not detected ON/PULSE: trigger complete event detected
ACTIVE	OFF: Instrument Idle ON/PULSE: Data acquisition initiated
PWR (LXI only)	OFF: Instrument off ON: Instrument powered on
1588 (LXI only)	OFF: IEEE 1588 clock not synchronized or fault ON: clock locked as IEEE 1588 slave TOGGLE @ 1s: clock synchronized as IEEE 1588 master TOGGLE @ 2s: clock synchronized as IEEE 1588 grand master

Power

Power Supplies

Product Option	Platform	Voltage	Typical Current	Maximum Current
ZT5211	PCI or PXI	+3.3 VDC	3.28A	4.72A
		+5 VDC	0.49A	0.75A
		+12 VDC	0.21A	0.67A
		-12 VDC	0.00A	0.00A
	VXI	+5 VDC	3.10A	4.51A
		+12 VDC	0.21A	0.67A
		+24 VDC	0.00A	0.00A
		-2 VDC	0.07A	0.08A
		-5.2 VDC	0.26A	0.34A
		-12 VDC	0.00A	0.00A
LXI	115 VAC	0.28A	0.33A	
		0.00A	0.00A	
ZT5212	VXI	+5 VDC	4.55A	6.52A
		+12 VDC	0.42A	1.34A
		+24 VDC	0.00A	0.00A
		-2 VDC	0.07A	0.08A
		-5.2 VDC	0.37A	0.52A
		-12 VDC	0.00A	0.00A
		-24 VDC	0.00A	0.00A
		LXI	115 VAC	0.40A
	0.00A			0.00A

Total Cooling & Power Consumption

Product Option	Platform	Typical Cooling & Power	Maximum Cooling & Power
ZT5211	PCI or PXI	15.8W	27.5W
	VXI	17.9W	32.44W
	LXI	32W	38W
ZT5212	VXI	29.77W	51.42W
	LXI	45W	57W

Physical

PCI Physical size	Single-Slot Short PCI Card
PXI Physical size	Single-Wide 3U Compact PCI/PXI Instrument
VXI Physical size	Single-Wide C-size VXIbus Instrument
LXI Physical size	Half-Width 1U LXI Instrument
PCI Weight	1 lb. or 0.45 kg
PXI Weight	1 lb. or 0.45 kg
VXI Weight	3 lbs. or 1.4 kg
LXI Weight	4 lbs. or 1.8 kg

Temperature Range

Operating	0 °C to +50 °C Ambient (MIL-PRF28800F Class 3)
Storage	-40 °C to +75 °C Ambient (MIL-PRF28800F Class 3)
Over-Temperature	Automatic shutdown if internal temperature exceeds +65 °C
Calibration Range	+20 °C to +30 °C Ambient, after a 20 minute warm-up period, to meet all calibration specification accuracies.

Relative Humidity

Operating or Storage	5 to 95 ± 5%, non-condensing, up to +30 °C
	5 to 75 ± 5%, non-condensing, +30 °C to +40 °C
	5 to 45 ± 5%, non-condensing, above +40 °C

Altitude

Operating	Up to 5,000 m
Storage	Up to 15,000 m

Safety

This product is designed to meet the requirements of the following standard of safety for electrical equipment for measurement, control and laboratory use:

EN 61010-1

Electromagnetic Compatibility

CE Marking EN 61326-1:1997 with A1:1998 and A2:2001 Compliant

FCC Part 15 (Class A) Compliant

Emissions

EN 55011	Radiated Emissions, ISM Group 1, Class A, distance 10 m, emissions < 1 GHz
EN 55011	Conducted Emissions, Class A, emissions < 30 MHz Immunity
EN 61000-4-2	Electrostatic Discharge (ESD), 4 kV by Contact, 8 kV by Air
EN 61000-4-3	RF Radiated Susceptibility, 10 V/m
EN 61000-4-4	Electrical Fast Transient Burst (EFTB), 2 kV AC Power Lines
EN 61000-4-5	Surge
EN 61000-4-6	Conducted Immunity
EN 61000-4-8	Power Frequency Magnetic Field, 30 A/m
EN 61000-4-11	Voltage Dips and Interrupts

CE Compliance

This product meets the necessary requirements of applicable European Directives for CE Marking as follows:

73/23/EEC	Low Voltage Directive (Safety)
89/336/EEC	Electromagnetic Compatibility Directive (EMC)

See Declaration of Conformity for this product for additional regulatory compliance information.