

ZT500PXI Specifications

Arbitrary Waveform Generator

14-bit, 300 MS/s, 2 Ch



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“SIG” Analog Output

PEAK OUTPUT VOLTAGE	0.1V to 3.5V peak (Hi-Z) 0.05V to 1.75V peak (50 Ω) selectable in 0.001V increments
ACCURACY	$\pm 0.25\%$ accuracy (standard) $\pm 0.1\%$ accuracy (optional)
DRIFT	25 ppm per $^{\circ}\text{C}$
SPUR FREE DYNAMIC RANGE (SFDR)	80 dBc @ $f_{\text{out}} = 1$ MHz sine
TOTAL HARMONIC DISTORTION (THD)	67 dBc @ $f_{\text{out}} = 50$ MHz sine
DUTY CYCLE	-73 dBc @ $f_{\text{out}} = 1$ MHz sine
RISE/FALL TIME	0.1% to 99.9%
FILTERING	< 4 nanoseconds (10%-90% of full scale)
IMPEDANCE	25 MHz, 50 MHz, 100 MHz, and none (selectable)
CONNECTOR	50 Ω (standard) 75 Ω (optional)
	SMB

“DIG 1” AND “DIG 2” Digital Outputs:

OUTPUT VOLTAGE	TTL level
DRIVE CAPABILITY	50 Ω
CONNECTOR	SMB

Trigger

PROGRAMMABLE SOURCE	Internal (software-generated), PXIbus TRG0-7, PXIbus STAR TRG, External
FRONT PANEL TRG IN/OUT	TTL level nominal, $\pm 5\text{V}$ max 10 k Ω nominal input impedance DC coupled
ACTIVE EDGE	rising edge or falling edge (programmable)
CONNECTOR	SMB

Digital-to-Analog Converter (DAC) Characteristics

DAC WIDTH	14 bits
SAMPLE RATES	20, 40, 80, 100, 160, 200, 300 Msamples/second
WAVEFORM MEMORY SIZE	up to 2M samples
SEQUENCER MEMORY SIZE	up to 64k waveforms

10 MHz Reference

PROGRAMMABLE SOURCE	Internal TCXO or PXIbus CLK10
FREQUENCY	10 MHz nominal

DUTY CYCLE	50% nominal
INTERNAL TCXO ACCURACY	±2 ppm

Power

	DC Peak Current	Dynamic Current
+3.3V	200 mA	50 mA
+5V	1.75 A	500 mA

Mechanical

SIZE:	3U, single slot, cPCI/PXI Module
FRONT PANEL:	See Figure 1-1 for front panel drawing.
COOLING REQUIREMENTS:	10 Watts/Slot
WEIGHT:	1 lb.

Environmental

TEMPERATURE RANGE:	OPERATING	-20 °C to +60 °C Ambient
	STORAGE	-40 °C to +75 °C
RELATIVE HUMIDITY:	OPERATING OR STORAGE	0 to 95%, non-condensing

PXI/cPCI Interface

PCI COMPATIBILITY:	Version 2.2		
BACKPLANE VOLTAGE:	Universal, +3.3V or +5V		
DATA WIDTH:	16 bit		
PXI COMPATIBILITY:	all triggers are software selectable		
	10MHz reference is software selectable		
	left and right side buses not used		
cPCI P2 PIN USAGE:	Pin A16	PXI Trigger 1	(TTL level input)
	Pin A17	PXI Trigger 2	(TTL level input)
	Pin A18	PXI Trigger 3	(TTL level input)
	Pin B16	PXI Trigger 0	(TTL level bidirectional)
	Pin B18	PXI Trigger 4	(TTL level input)
	Pin C18	PXI Trigger 5	(TTL level input)
	Pin D16	PXI Star Trigger	(TTL level input)
	Pin E16	PXI Trigger 7	(TTL level input)
	Pin E17	PXI 10 MHz Clock	(TTL level input)
	Pin E18	PXI Trigger 6	(TTL level input)