



14 Bit, 300 Msps PXIbus Arbitrary Waveform Generator

Installation & Operation, Programming, and
Diagnostic Manual
0004-000030

Model ZT500PXI

Version 1

September 1, 2004

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The ZT500PXI is susceptible to ESD damage. Place instrument or module in conductive (anti-static) envelopes or carriers, when transported. Open only at an ESD approved work surface. An ESD safe work surface is defined as follows:

1. The work surface must be conductive and reliably connected to earth ground through a safety resistance of approximately 250 kilohms.
2. The surface must NOT be metal. (A resistivity of 30 to 300 kilohms per square inch is suggested.)

Ground the frame of any line-powered equipment, chassis, test instruments, lamps, soldering irons, etc., directly to earth ground. To avoid shorting out the safety resistance, be sure that grounded equipment has rubber feet or other means of insulation from the work surface.

Avoid placing tools or electrical parts on insulators. Do not use any hand tool (such as non-conductive plunger-type solder suckers) that can generate a static charge. Ground yourself reliably, through a resistance, to the work surface using, for example, a conductive strap or cable with a wrist cuff. The cuff must make electrical contact directly with your skin; do NOT wear it over clothing. (Resistance between skin contact and work surface through a commercially available personnel grounding device is typically 250 kilohms to 1 megohm.)

Avoid circumstances that are likely to produce static charges, such as wearing clothes of synthetic material, sitting on a plastic-covered stool (particularly while wearing wool), combing your hair, or making extensive erasures. These circumstances are most significant when the air is dry.

When testing static sensitive devices, be sure DC power is on before, during, and after application of test signals. Be sure all pertinent voltages have been switched off while boards or components are removed or inserted.

REVISION HISTORY

<u>Rev</u>	<u>Date</u>	<u>Section</u>	<u>Description</u>
-	11 Mar 2002		original release
-A	29 Mar 2002	4.5 6.2 & 6.2.1	corrected error in trigger source table updated function generator demo description
-B	31 May 2002	1.2 1.3 2.1 3.18 4.4 4.5	changed Rev and data through out document update PEAK OUTPUT VOLTAGE and 20 MHz removed TBD's Changed .inf statement to other section added 20 MHz sample rate deleted Update segment query address updated READ MAX SEGMENT SIZE, READ PART NUMBER, SELECT SAMPLE RATE, SELECT SEGMENT COUNT, SELECT SEGMENT SIZE, SELECT TRIGGER MODE, SELECT TRIGGER SOURCE, SELECT VOLTAGE RANGE, TRIGGER IMMEDIATELY, WRITE SEQUENCE, SELECT TRIGGER EDGE, SELECT VOLT RANGE, SELECT SAMPLE RATE
-C	1 July 2002	1.4 3.1 3.2 3.4 3.4 3.5 4.4 4.5 5.6 6.1 6.2.1	Copyright and ESD Update Figure 1-1 remove external clock, swapped DIG1 & 2 Update Figure 3-1 added Offset DAC Update Figure 3-2 added trig external and PXI 0 Update Figure 3-5 add Retrigger mode Total update and reorganization of this section Update Figure 3-19 add Offset DAC Update Figure 4-1, able 4-4 Update commands Applications section - created Create section ZT500PXI FIND UTILITY Update Figure 6-2 and section
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1 INTRODUCTION

1.1 DESCRIPTION

The ZTEC Instruments, Inc. model ZT500PXI is an 14 bit, 300 million samples per second (Msps), Arbitrary Waveform Generator (AWG). The ZT500PXI is built around a high speed, deep memory sequencer and embedded TMS320VC5409 digital signal processor (DSP) housed within a single-wide PXI module. Together with the host processor and software, the ZT500PXI provides a simple yet powerful way to generate test waveforms in wide bandwidth analog, IF, and low frequency RF applications.

The high speed sequencer generates waveforms with up to 200 MHz of bandwidth (as measured by output signal 10%-90% full scale transition time). Waveforms are read from a user definable library stored in a 2 million point memory. Sequencer instructions are stored in a 64k location memory. The ZT500PXI also produces two user definable digital signals, fully synchronized with the analog output, suitable for waveform markers or general purpose digital sync signals. A full set of controls allows the user to specify signal bandwidth, signal voltage range, and sample rate.

1.2 cPCI/PXI INTEROPERABILITY

The ZT500PXI may be used in both CompactPCI (cPCI) and PCI eXtensions for Instrumentation (PXI) applications. The PXI standard is a derivative of cPCI and maintains a high level of interoperability. As a result PXI cards may safely be used in cPCI mainframes for most installations. Compatibility issues arise because the PXI standard reserves several normally undedicated pins on the cPCI P2 connector for a selection of trigger, clock, and inter-card communication functions. Before installing the ZT500PXI into a cPCI mainframe that uses the P2 connector, the user must ensure that pin use conflicts will not occur, see Section 1.3.4 for a list of the P2 pins used by the ZT500PXI.

1.3 ZT500PXI MODULE SPECIFICATIONS

1.3.1 FUNCTIONAL SPECIFICATIONS

■ “SIG” ANALOG OUTPUT:

PEAK OUTPUT VOLTAGE	0.1V to 3.5V peak (Hi-Z) 0.05V to 1.75V peak (50Ω) selectable in 0.001V increments
ACCURACY	±0.25% accuracy (standard) ±0.1% accuracy (optional)
DRIFT	25 ppm per °C
SPUR FREE DYNAMIC RANGE (SFDR)	80 dBc @ $f_{out} = 1$ MHz sine 67 dBc @ $f_{out} = 50$ MHz sine
TOTAL HARMONIC DISTORTION (THD)	-73 dBc @ $f_{out} = 1$ MHz sine
DUTY CYCLE	0.1% to 99.9%
RISE/FALL TIME	< 4 nanoseconds (10%-90% of full scale)
FILTERING	25 MHz, 50 MHz, 100 MHz, and none (selectable)
IMPEDANCE	50Ω (standard) 75Ω (optional)
CONNECTOR	SMB

■ “DIG 1” AND “DIG 2” DIGITAL OUTPUTS:

OUTPUT VOLTAGE	TTL level
DRIVE CAPABILITY	50Ω
CONNECTOR	SMB

■ TRIGGER:

PROGRAMMABLE SOURCE	Internal (software-generated), PXIbus TRG0-7, PXIbus STAR TRG, External
FRONT PANEL TRG IN/OUT	TTL level nominal, ±5V max 10 kΩ nominal input impedance DC coupled
ACTIVE EDGE	rising edge or falling edge (programmable)
CONNECTOR	SMB

■ DIGITAL-to-ANALOG CONVERTER (DAC) CHARACTERISTICS:

DAC WIDTH	14 bits
SAMPLE RATES	20, 40, 80, 100, 160, 200, 300 Msamples/second
WAVEFORM MEMORY SIZE	up to 2M samples
SEQUENCER MEMORY SIZE	up to 64k waveforms

- **10 MHz REFERENCE:**

PROGRAMMABLE SOURCE	Internal TCXO or PXIbus CLK10
FREQUENCY	10 MHz nominal
DUTY CYCLE	50% nominal
INTERNAL TCXO ACCURACY	±2 ppm

- **POWER:**

	<i>DC Peak Current</i>	<i>Dynamic Current</i>
+3.3V	200 mA	50 mA
+5V	1.75 A	500 mA

1.3.2 MECHANICAL

- **SIZE:** 3U, single slot, cPCI/PXI Module
- **FRONT PANEL:** See Figure 1-1 for front panel drawing.
- **COOLING REQUIREMENTS:** 10 Watts/Slot
- **WEIGHT:** 1 lb.

1.3.3 ENVIRONMENTAL

- **TEMPERATURE RANGE:**

OPERATING	-20 °C to +60 °C Ambient
STORAGE	-40 °C to +75 °C
- **RELATIVE HUMIDITY:**

OPERATING OR STORAGE	0 to 95%, non-condensing
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1.3.4 PXI/cPCI INTERFACE

- **PCI COMPATIBILITY:** Version 2.2
- **BACKPLANE VOLTAGE:** Universal, +3.3V or +5V
- **DATA WIDTH:** 16 bit
- **PXI COMPATIBILITY:**
 - all triggers are software selectable
 - 10MHz reference is software selectable
 - left and right side buses not used

- **cPCI P2 PIN USAGE:**

Pin A16	PXI Trigger 1	(TTL level input)
Pin A17	PXI Trigger 2	(TTL level input)
Pin A18	PXI Trigger 3	(TTL level input)
Pin B16	PXI Trigger 0	(TTL level bidirectional)
Pin B18	PXI Trigger 4	(TTL level input)
Pin C18	PXI Trigger 5	(TTL level input)
Pin D16	PXI Star Trigger	(TTL level input)
Pin E16	PXI Trigger 7	(TTL level input)
Pin E17	PXI 10 MHz Clock	(TTL level input)
Pin E18	PXI Trigger 6	(TTL level input)

1.4 FRONT PANEL

A diagram of the ZT500PXI front panel is shown in Figure 1-1. On the front panel, there are four SMB coaxial connectors. Table 1-1 lists the connector functions.

Label	Description
DIG 1	user definable TTL sync/marker output 1
DIG 2	user definable TTL sync/marker output 2
TRG	external trigger input
SIG	signal output

Table 1-1. Front Panel Connectors

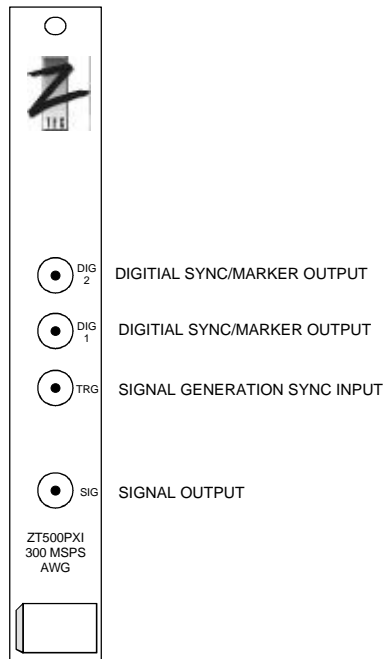


Figure 1-1 Front panel of the ZT500PXI

1.5 ZTEC INSTRUMENTS, INC. CONTACT INFORMATION

ZTEC Instruments, Inc. can provide detailed technical information about the ZT500PXI performance and applications, as well as installation and configuration assistance. ZTEC Instruments, Inc. can be contacted at the following address.

ZTEC Instruments, Inc.
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ALBUQUERQUE, NM 87109
(505) 342-0132 VOICE
(505) 342-0222 FAX
www.ztec-inc.com
ztec-inc@ztec-inc.com

2 INSTALLATION & CONFIGURATION

2.1 INSTALLATION PROCEDURE

Before installing the ZT500PXI hardware and software, LabVIEW version 5 or 6 must be present on the host computer.

2.1.1 SOFTWARE INSTALLATION

- 1) Selecting the appropriate ZIP file for your installation, (use the xxx_LV60 file for LabVIEW™ 6.0 and xxx_LV61 for LabVIEW™ 6.1), extract the ZT500PXI demo ZIP file into the destination drive root directory, the correct directory structure should be automatically created,
- 2) from the <c:>\ZTEC directory, where <c:> is the install drive, right click the ".inf" file appropriate for the host computer operating system and select the "Install" option, see the list below for additional guidance,

Windows 9x	select the file "Z-Card_9x.inf"
Windows NT4	select the file "Z-Card_nt4.inf"
Windows 2000	select the file "Z-Card_nt5.inf".

2.1.2 HARDWARE INSTALLATION

- 1) Power off the cPCI/PXI mainframe and slide the ZT500PXI into the chassis until the front panel handle contacts the chassis. Use any PXIbus slot marked with the "O" glyph, or any open cPCI slot. Complete unit installation by pressing upward on the front panel handle until the handle lock engages,
- 2) Once the module is seated in the mainframe, tighten the captive screw at the top and bottom of the ZT500PXI into the mainframe,
- 3) Power up the mainframe and then reboot the host computer, the operating system should detect the new device and automatically configure the support driver.

2.1.3 INSTALLATION COMPLETION

- 1) open and run the "ZT500PXI_Find.vi", located in the <c:>\ZTEC\ZT500PXI directory, and note the VISA Name of all identified ZT500PXI units, an example VISA name is "PXI2::9::INSTR",
- 2) before running the panel open all the *.ini files in the "config" directory and update both the SEQ_FILE and SEG_FILE addresses to the proper location.
- 3) open the "ZT500PXI_AWG_demo_Rev_?.vi", also located in the <c:>\ZTEC\ZT500PXI directory, and enter the VISA name identified above into the VISA Resource Name control, located at the panel lower right, then right-click on the control and select the "Data Operations > Make Current Value Default" option, and then save the panel. This will save the VISA name for future use.
- 4) Repeat the previous step for the ZT500PXI_func_demo_Rev?.vi.

2.1.4 ZT500PXI DIRECTORY STRUCTURE

The normal ZT500PXI software installation requires the creation of the directory structure shown in Figure 2-1. The top level directory must be created by the user. Lower level directories should be created by the unzip process.

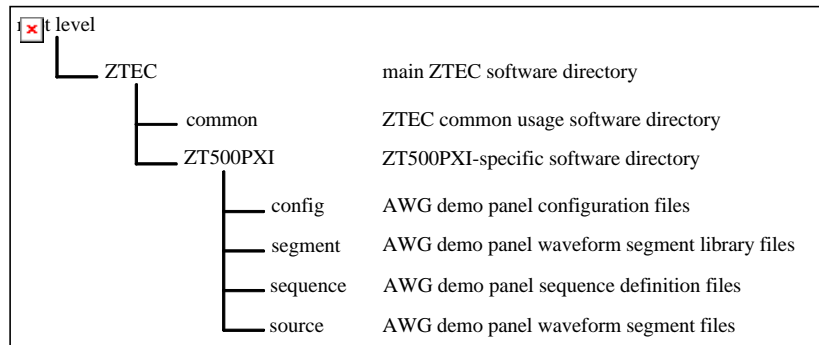


Figure 2-1 ZT500PXI Software Install Directories

2.2 ADVANCED CONFIGURATION OPTIONS

The ZT500PXI has one internal jumper that is configured at the factory and should not be changed without proper guidance from the manufacturer. The function of this jumper is included here for completeness. Table 2-1 lists the function of the jumper. The default configuration is shown in the left column in bold type. Figure 2-2 shows the location of this jumper.

Ref #	Default Position	Other Positions
JP1	Remove: Isolate chassis and signal grounds	Install: Connect chassis and signal grounds

Table 2-1. Jumper Configuration Options

The ZT500PXI has internal programming headers that are used to download firmware and test the unit at the factory. These headers should not be used without proper guidance from the manufacturer. The function of these headers is included here for completeness. Table 2-2 lists the functions of the headers. Figure 2-2 shows the locations of these headers.

Ref #	Description
J1	cPCI main connector
J2	cPCI user I/O connector
J4	JTAG connector for in-circuit emulation and downloading of DSP
J5	JTAG connector for CPLD device programming
J6	Debug terminal port

Table 2-2. Header Connector Functions

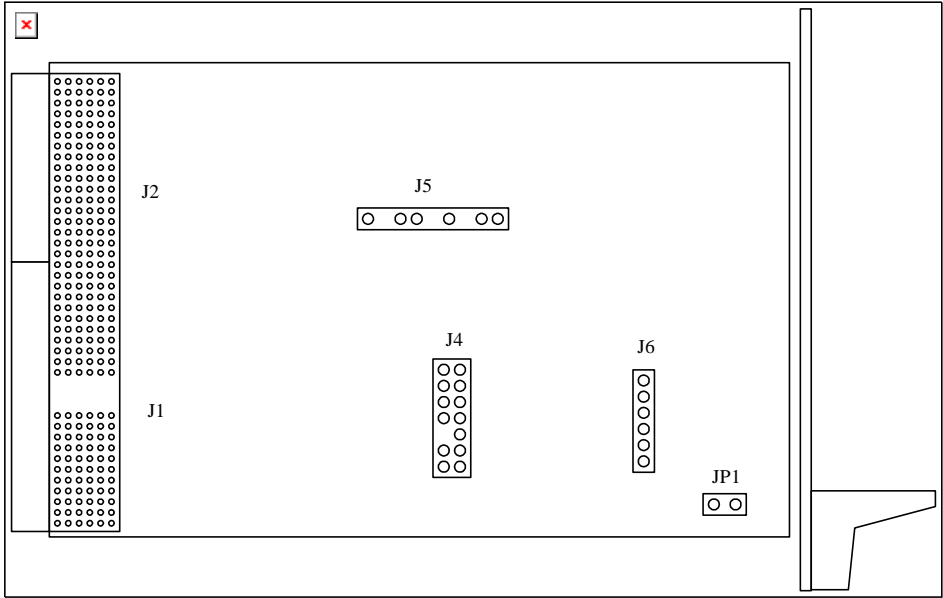


Figure 2-2. ZT500PXI Jumper and Connector Locations

3 DEVICE OPERATION

3.1 FUNCTIONAL BLOCK DIAGRAM

A functional block diagram of the ZT500PXI is shown in Figure 3-1. Sampled waveforms are read by the Sequencer from a library of waveform segments held in the Segment Table. The order of segment readout is determined by a segment index list held in the Sequencer Table. Waveform samples are read by a Sequencer and are then converted to analog by the Signal DAC. The analog Signal DAC output is passed through a selectable bank of linear phase lowpass filters and is then buffered for output to the SIG connector. Synchronously with the waveform sample conversion, the two digital sync/marker outputs are buffered and sent to the DIGx connectors. The analog signal voltage range is set by the Range DAC. The analog output offset is set by the Offset DAC. The Signal DAC sample rate is generated from the selected 10 MHz reference by the Sample Rate PLL.

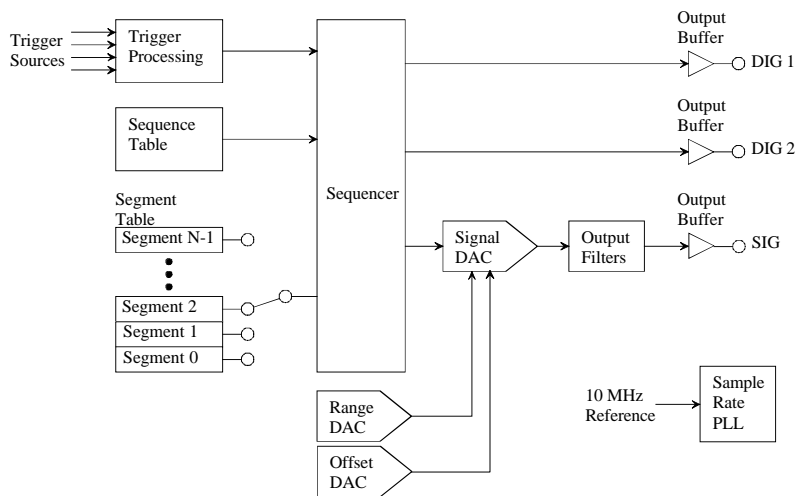


Figure 3-1 ZT500PXI Functional Block Diagram

3.2 TRIGGER PROCESSING

The ZT500PXI accepts triggers from all PXI backplane trigger sources including PXI_TRG[0:7] and PXI_STAR, see the (SELECT TRIGGER SOURCE) command. In addition, the ZT500PXI allows selection of the front panel trigger input and a software initiated trigger, see the (TRIGGER IMMEDIATELY) command. The front panel trigger input uses normal TTL logic levels, with a 0.5V nominal threshold for a low level and a 2V nominal threshold for a high level. The ZT500PXI requires a positive truth/rising edge trigger. In order to accommodate negative truth or falling edge trigger inputs, the selected trigger may be inverted, see the (SELECT TRIGGER EDGE) command. Figure 3-2 shows a diagram of the ZT500PXI trigger processing.

The FRONT PANEL TRIGGER OUT and PXI TRG0 TRIGGER OUT functions are programmable outputs from the ZT500PXI. They can be used to output a copy of the currently selected ZT500PXI trigger signal.

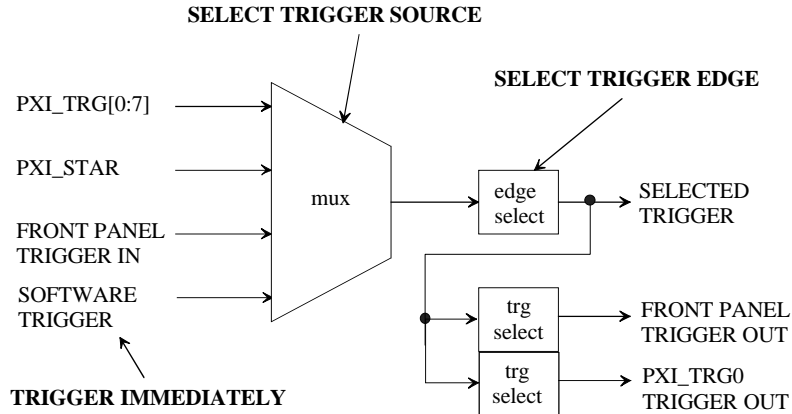


Figure 3-2 ZT500PXI Trigger Processing

3.3 SEGMENT AND SEQUENCER TABLES

The ZT500PXI provides two tables for control of waveform generation: the Segment Table and the Sequencer Table. Figure 3-3 shows a diagram of these tables and associated commands.

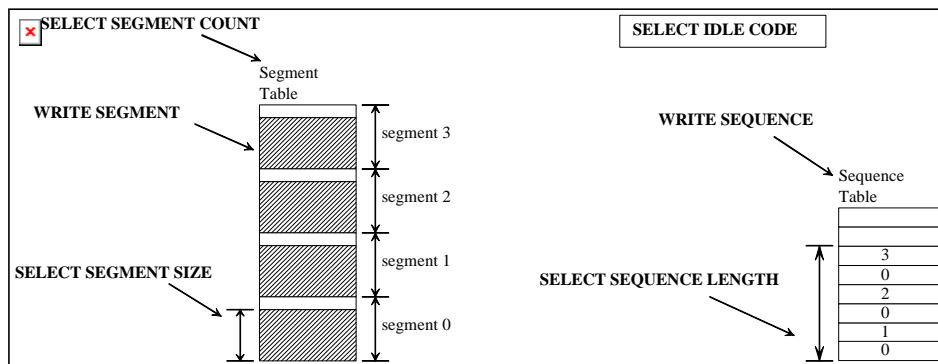


Figure 3-3 Segment and Sequencer Tables

The Segment Table is a library of waveforms or waveform segments that are read by the Sequencer and forwarded to the Signal DAC for conversion to analog. The 2 Msample deep Segment Table is divided into a user selectable number (1, 2, 4, .. 65536) of equally sized storage segments, see the (SELECT SEGMENT COUNT) command. The segment length can be limited to a size smaller than the storage size, see the (SELECT SEGMENT SIZE) command, ex. a 2048 length segment store (2097152 memory size/1024 segments) can be limited to 2000 samples. The segment size must be a multiple of 2 and must be greater than or equal to 4.

The Segment Table is loaded segment by segment using the (WRITE SEGMENT) command. During segment load the analog output is disconnected during waveform download causing the waveform to return to 0V, when this occurs a series of 0.5V, 20 μ sec transients will occur on the SIG output. The ZT500PXI analog signal level output when the device is not running can be configured using the (SELECT IDLE CODE) command. *NOTE: the last two memory locations in the 2 Msample Segment Table are reserved for storage of the idle code.*

Each location in the Segment Table is 16 bits wide. As shown in Figure 3-4, the most significant 14 bits are reserved for the code going to the Signal DAC, the next bit is reserved for the DIG 2 output and the least significant bit is reserved for the DIG 1 output, ex. a Segment Table entry of 8002_{16} would result in the bit pattern 10000000_2 being sent to the Signal DAC, a 1 being sent to the DIG 2 output, and a 0 being sent to the DIG 1 output. *NOTE: there is a 4 stage pipeline delay between the data paths for the analog and digital outputs, thus the digital outputs will always appear at the output 4 sample times before the analog code stored in the same memory location.*

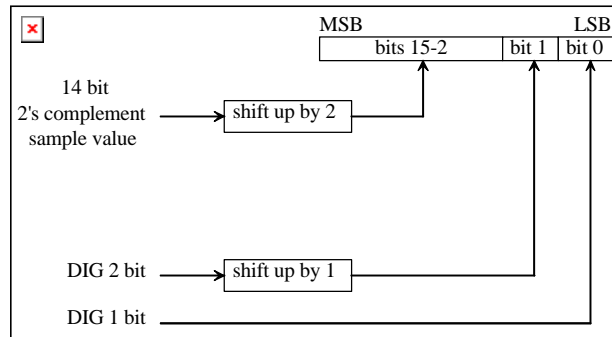


Figure 3-4 ZT500PXI Sample Word Format

The Sequencer Table is a list indicating the order that waveform segments should be read out. For simple waveforms only one segment would be defined, segment 0, and this list may contain only 1 entry, a 0. For more complicated waveforms, for example a video signal, segment 0 could be reserved for the horizontal sync and segments 1 to N could be reserved for individual line contents. In this application the sequence list would be: 0,1,0,2,0,3, ... The length of the table may be set to any value from 1 to 65536, see the (SELECT SEQUENCE LENGTH) command. The Sequencer Table is loaded using the (WRITE SEQUENCE) command.

3.4 WAVEFORM SEQUENCER

The Waveform Sequencer (or Sequencer) reads waveform segments from the Segment Table and forwards the samples to the Output Channel according to instructions from the Sequencer Table. As shown in Figure 3-5, sequencer operation is configured by commands that determine master run/stop state, playback initiate/pause state, segment advance condition, retrigger mode and sequencer table end response.

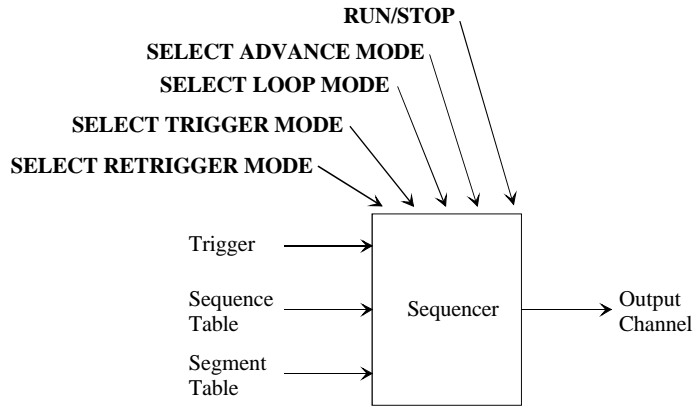


Figure 3-5 ZT500PXI Waveform Sequencer

Overall ZT500PXI waveform output control is provided by a master run/stop command (RUN/STOP). When running, the sequencer can be set to advance to the next segment in the sequence list either at segment end or on a trigger event (SELECT ADVANCE MODE). When the end of the sequence list is reached, the sequencer can either stop or loop to the beginning of the table and replay the list (SELECT LOOP MODE).

The ZT500PXI sequencer provides a variety of ways to initiate and pause waveform replay (SELECT TRIGGER MODE). The four basic modes are non-triggered, triggered, trigger gated and delayed trigger. The ZT500PXI sequencer provides a retrigger mode (SELECT RETRIGGER MODE), which defines how the Sequencer handles the end of segment and end of sequence conditions. The following sections show each control supported and their flexibility. Refer to Section 5 for more detailed information on triggering modes and applications.

3.4.1 SEQUENCER LOOP MODE

Sequencer Loop mode (SELECT LOOP MODE) is set to loop or single. In Figure 3-6 the Sequencer is set to loop, the Sequencer will endlessly repeat the Sequencer Table as long as the Sequencer is set to Run. In Figure 3-7 the Sequencer is set to single, the Sequencer plays the Sequencer Table once, when the device is set to Run. When the last segment, Segment 2, is completed the waveform generation will stop.

Sequence Mode = Loop
 Sequence Advance = Auto
 Trigger Mode = Non-Triggered
 Retrigger Mode = Non
 Sequence Length = 3
 Sequence Order = 1, 6, 3, 2
 Segment Loop = 1

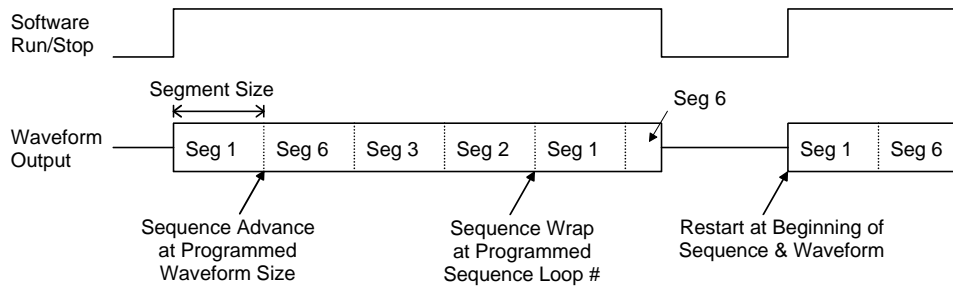


Figure 3-6. Sequencer Loop Mode - Loop

Sequence Mode = Single
 Sequence Advance = Auto
 Trigger Mode = Non-Triggered
 Retrigger Mode = Non
 Sequence Length = 3
 Sequence Order = 1, 6, 3, 2
 Segment Loop = 1

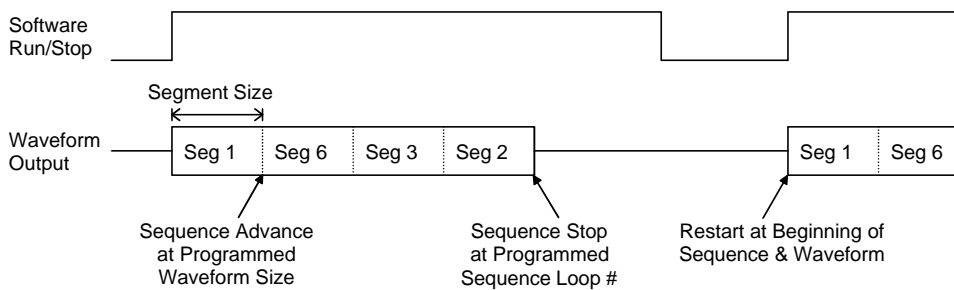


Figure 3-7. Sequencer Loop Mode - Single

3.4.2 SEQUENCER ADVANCE MODE

Sequencer Advance mode (SELECT ADVANCE MODE) is either set to Auto or Triggered. Auto allows the Sequencer to proceed to the next segment when the current segment is completed as shown in Figure 3-8. When Advance Mode is set to Triggered the Sequencer will advance to the next segment when a trigger event is detected as shown in Figure 3-9.

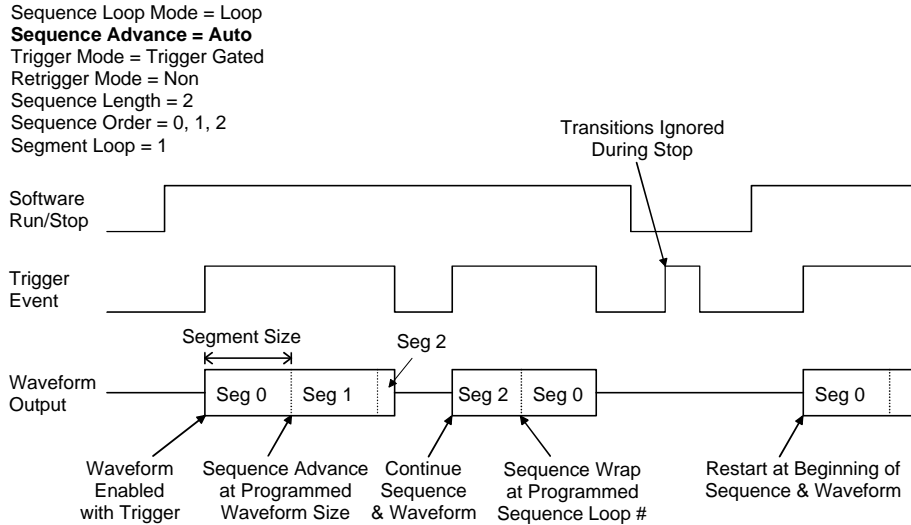


Figure 3-8. Sequencer Advanced Mode – Auto

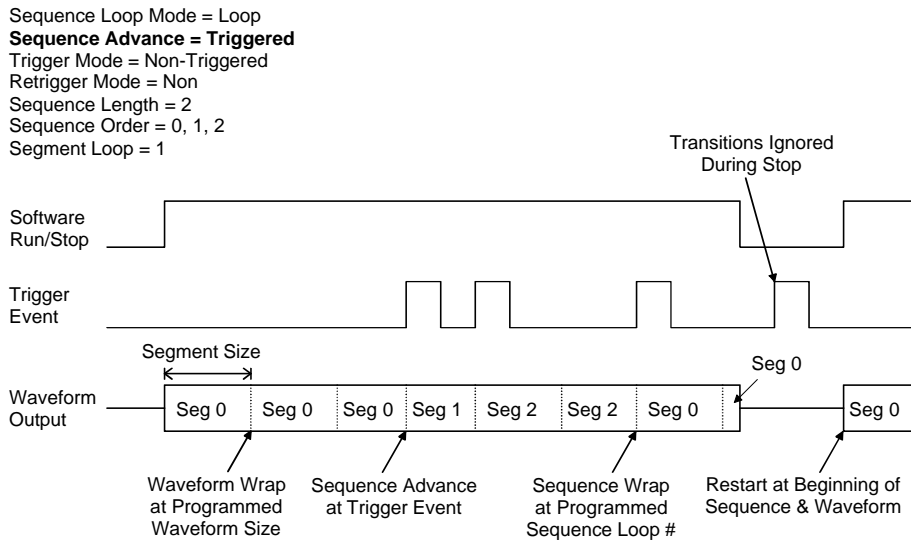


Figure 3-9. Sequencer Advanced Mode – Trigger

3.4.3 TRIGGER MODE

Trigger mode (SELECT TRIGGER MODE) is set to Non Triggered, Triggered, Trigger Gate or Delayed Trigger. Figure 3-10 illustrates the Non-Triggered mode in which waveform output begins immediately after Run is active.

When Trigger Mode is set to Triggered, the Sequencer is set to delay waveform output until a trigger event is detected. As shown Figure 3-11 Run must be active as the Sequencer waits for a valid trigger event to start the Waveform Output sequencing.

When Trigger Mode is set to Trigger Gate the Waveform Output is valid only when the trigger event is high. As shown in Figure 3-12 when Run is activated the Sequencer waits for a valid trigger event and as long as the trigger event is high the waveform is present at the output.

When Trigger Mode is set to Delayed Trigger and the Sequencer is set to Run, the Sequencer waits for an active trigger event and then delays for a user selectable delay period before initiating waveform output as shown in Figure 3-13.

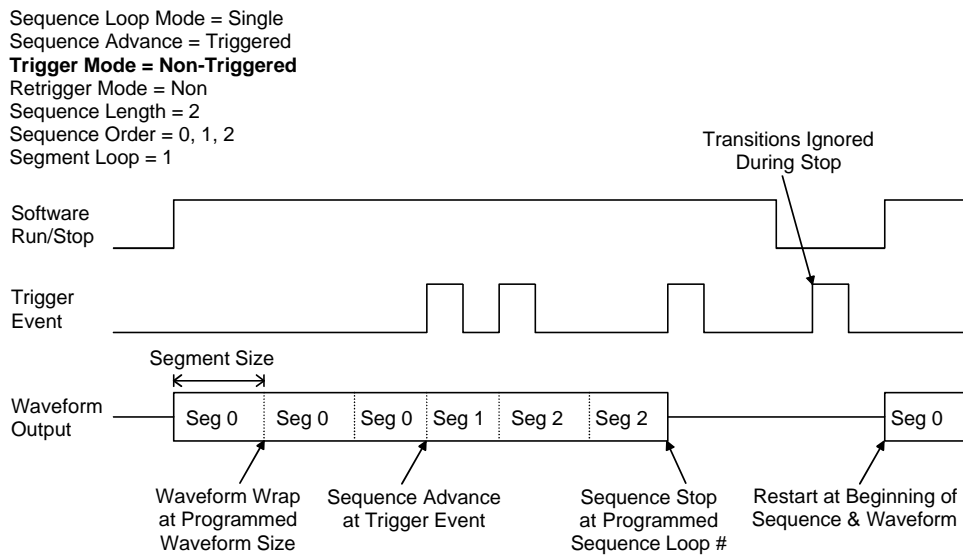


Figure 3-10. Trigger Mode – Non Triggered

Sequence Loop Mode = Loop
 Sequence Advance = Triggered
Trigger Mode = Triggered
 Retrigger Mode = Non
 Sequence Length = 2
 Sequence Order = 0, 1, 2
 Segment Loop = 1

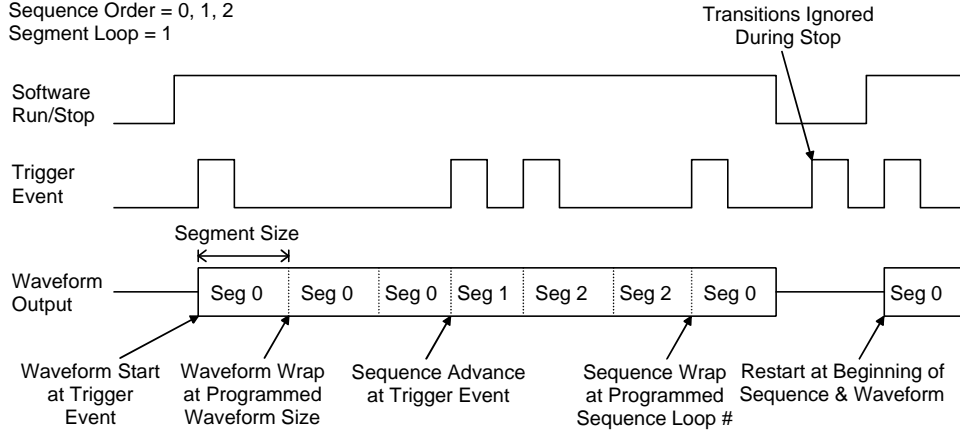


Figure 3-11. Trigger Mode – Triggered

Sequence Loop Mode = Loop
 Sequence Advance = Triggered
Trigger Mode = Trigger Gated
 Retrigger Mode = Non
 Sequence Length = 2
 Sequence Order = 0, 1, 2
 Segment Loop = 1

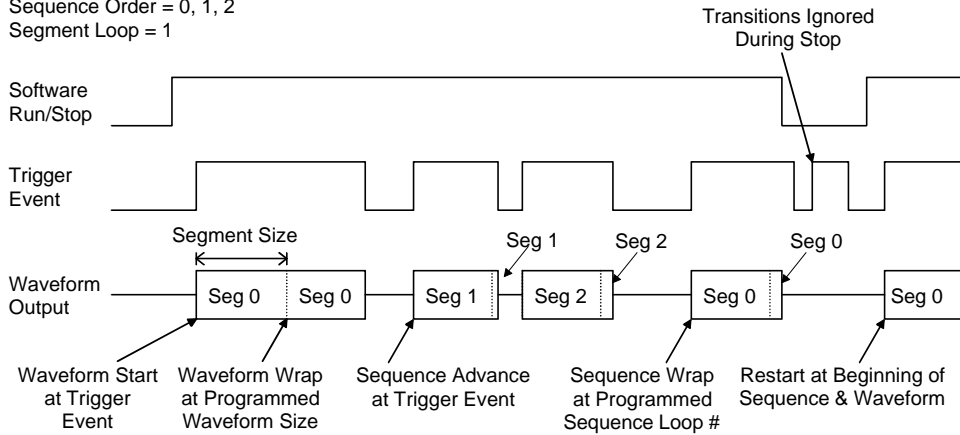


Figure 3-12. Trigger Mode – Trigger Gate

Sequence Loop Mode = Single
 Sequence Advance = Auto
Trigger Mode = Delayed Trigger
 Retrigger Mode = Non
 Sequence Length = 2
 Sequence Order = 0, 1, 2
 Segment Loop = 1

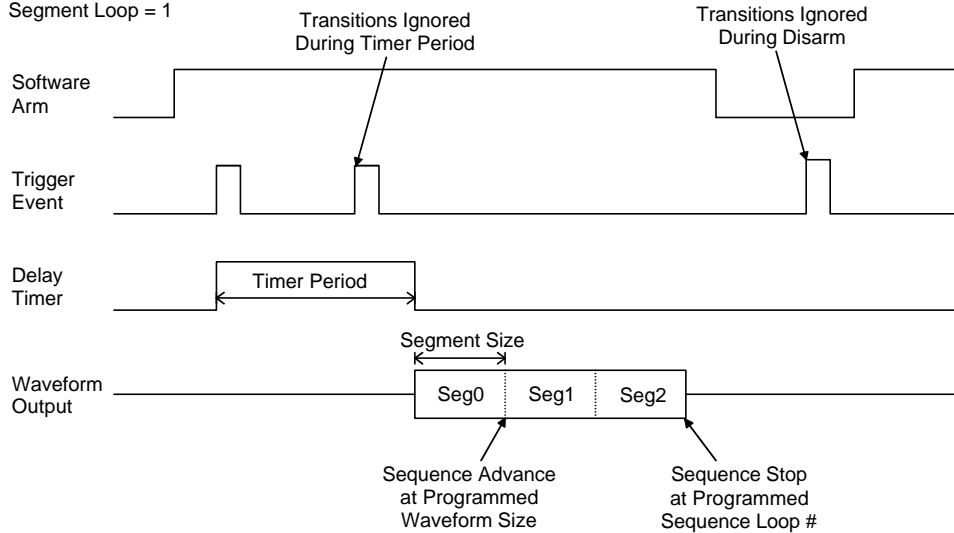


Figure 3-13. Trigger Mode – Delayed Triggered

3.4.4 RETRIGGER MODE

Retrigger mode (SELECT RETRIGGER) is set to Non-Retrigger, Segment Retrigger or Sequence Retrigger. When the Retrigger Mode is not set to Non-Retrigger, the Sequence Loop Mode must be set to Single and the Sequence Advance mode must be set to Auto. The Trigger Mode Trigger Gated setting is not supported when using retriggered operation.

When Retrigger Mode is set to Non-Retrigger, as shown in Figure 3-13 of the last section, the sequencer plays the sequence once.

When the Retrigger Mode is set to Segment Retrigger as shown in Figure 3-14, the Sequencer waits for Run to be active, then plays the first segment, and then pause waveform output. When a retrigger event is detected, the next segment will be played and then waveform output again is stopped.

When the Retrigger Mode is set to Sequence Retrigger as shown in Figure 3-15, the Sequencer waits for Run to be active, then waits for an active trigger event, and then plays the entire sequence once. When a second active trigger event is detected the entire sequence is played again.

Sequence Loop Mode = Single
 Sequence Advance = Auto
 Trigger Mode = Triggered
Retrigger Mode = Segment
 Sequence Length = 1
 Sequence Order = 0, 3
 Segment Loop = 1

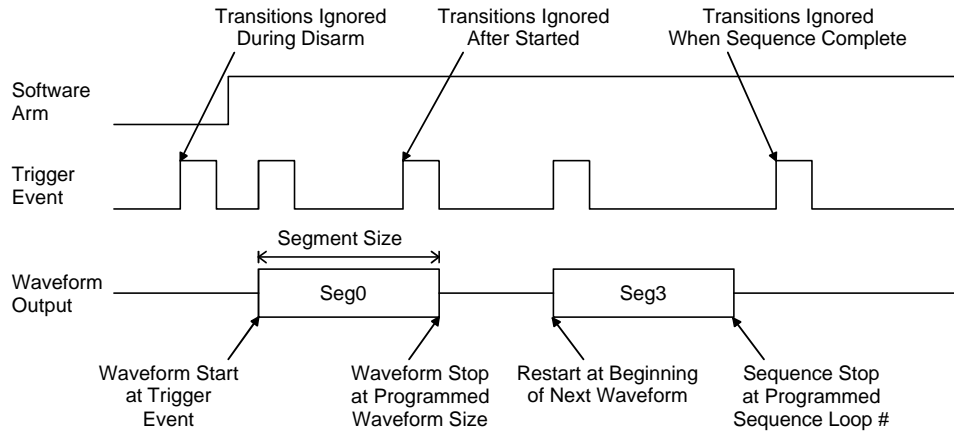


Figure 3-14. Retrigger Mode – Segment

Sequence Loop Mode = Single
 Sequence Advance = Auto
 Trigger Mode = Triggered
Retrigger Mode = Sequence
 Sequence Loop# = 2
 Sequence = 0, 1, 2
 Segment Loop = 1

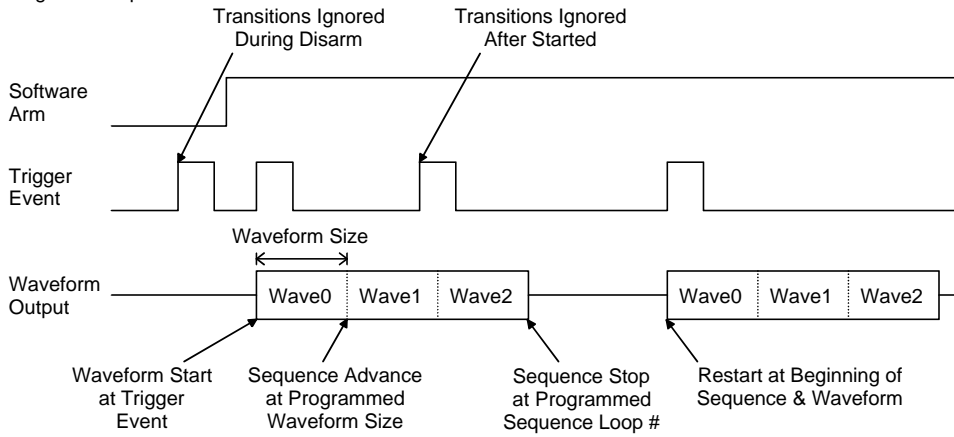


Figure 3-15. Retrigger Mode – Sequence

3.4.5 SEQUENCE LENGTH

Sequence Length (SELECT SEQUENCE LENGTH) determines the number of entries in the Sequencer Table. Valid sequence length settings vary from 0 to 65535. The actual number of Sequencer Table entries is one larger than the sequence length setting. Figure 3-16 illustrates that a sequence length setting of two will result in three entries being taken from the Sequencer Table.

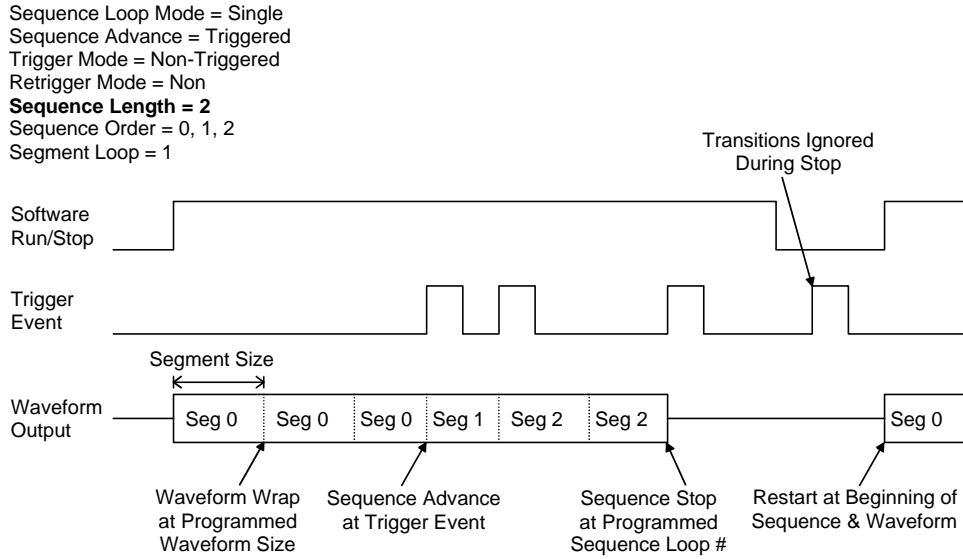


Figure 3-16. Sequence Length

3.4.6 SEQUENCE ORDER

Sequence Order (WRITE SEQUENCE ORDER) determines the order that segments are sent to the Waveform Output by the Sequencer. Figure 3-17 illustrates that the Sequencer is set to process segments in the following Sequence Order 1, 6, 3 & 2.

Sequence Loop Mode = Single
 Sequence Advance = Auto
 Trigger Mode = Non-Triggered
 Retrigger Mode = Non
 Sequence Length = 3
Sequence Order = 1, 6, 3, 2
 Segment Loop = 1

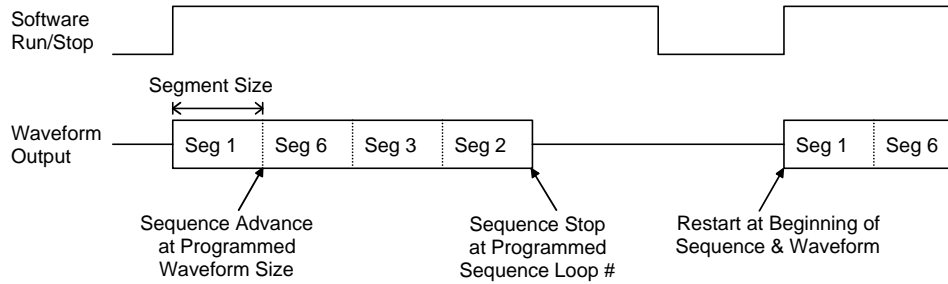


Figure 3-17. Sequence Order

3.4.7 SEGMENT COUNT

The Segment Count (SELECT SEGMENT COUNT) determines how the Segment Memory will be partitioned. Segment count code may be set from 0 to 16. The actual number of segments selected may be calculated as shown in EQUATION 1.

$$\text{Number of Segments} = 2^{\text{Segment Count Code}} \quad (\text{Equation 1})$$

3.4.8 SEGMENT SIZE

The Segment Size (SELECT SEGMENT SIZE) is the number of samples used from each segment. Valid segment sizes range from 4 to the maximum number of samples for the selected segment count and must be a multiple of 2. The maximum segment size may be queried directly (READ MAXIMUM SEGMENT SIZE) or may be calculated as shown in EQUATION 2 where "2M" is the segment memory size. An error will be generated if a large segment size is selected and then the segment count setting is increased to a value that makes the segment size too large (i.e. segment size > maximum segment size). To prevent this error always set the new segment size before setting the segment count.

$$\text{Segment Size}_{\text{max}} = 2M / 2^{\text{Segment Count Code}} \quad (\text{Equation 2})$$

3.4.9 SEGMENT LOOP

The Segment Loop (SELECT SEGMENT LOOP) determines how many times each segment may be played before the Sequencer advances to the next segment. If the Segment Loop is set to 2 then each segment in the Sequencer Table will be played twice. If the Sequence Order is 1, 6, 3 & 2 then the Waveform Output will be 1, 1, 6, 6, 3, 3, 2 and 2 as shown in Figure 3-18.

Sequence Loop Mode = Loop
 Sequence Advance = Auto
 Trigger Mode = Non-Triggered
 Retrigger Mode = Non
 Sequence Length = 3
 Sequence Order = 1, 6, 3, 2
Segment Loop = 2

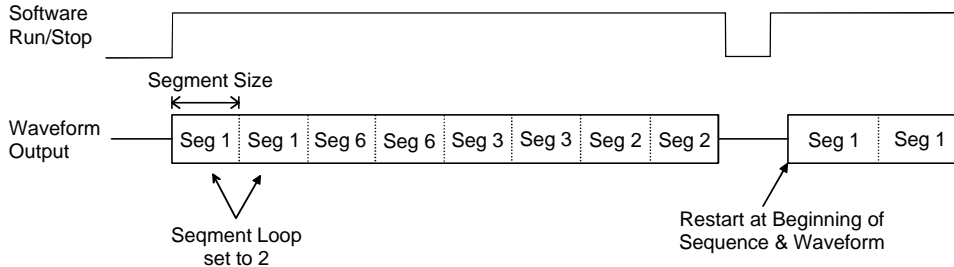


Figure 3-18. Segment Loop

3.5 OUTPUT CHANNEL OPERATION

The ZT500PXI analog output channel is based on a high speed, 14-bit digital-to-analog converter (DAC) and supporting signal conditioning to designed to optimize the output signal integrity. Figure 3-19 shows a diagram of the output channel.

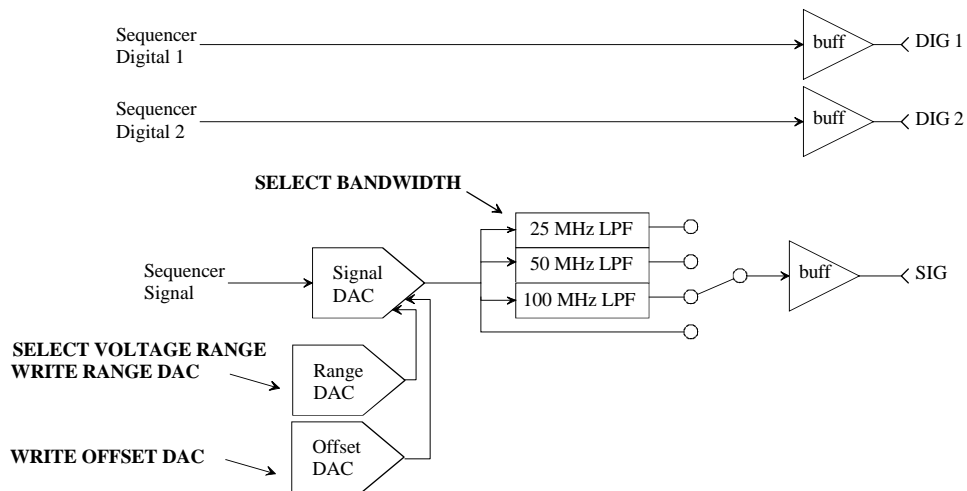


Figure 3-19. ZT500PXI Output Channel

The maximum output signal level is determined by the Range DAC setting. The range is normally set in 0.001V steps using the (SELECT VOLTAGE RANGE) command. The Range DAC setting is interpolated from a calibration table. The standard calibration points are: 0.1V, 0.2V, 0.5V, 1.0V, 1.5V, 2.0V, 2.5V, 3.0V, 3.3V, and 3.5V. Each calibration table entry is accurate to $\pm 0.1\%$.

A bank of selectable, 5 pole, linear phase, lowpass filters allows improved reconstruction of the analog output signal (SELECT BANDWIDTH). The standard cutoff frequencies are: 25 MHz, 50 MHz, and 100 MHz. The filters can also be bypassed for reproduction of very wide band or logic signals. The analog output includes a series 50 Ω 0.1% tolerance resistor (standard, 75 Ω optional) as back termination.

Two synchronized digital outputs are provided for use as auxiliary signal outputs or as sync/markers. The digital outputs are designed to achieve TTL levels with a 50 Ω load. The digital outputs operate at $\frac{1}{2}$ the DAC sample rate.

For advanced control, the (WRITE/READ RANGE DAC) command allows user setting and query of the 16 bit Range DAC to directly control the full scale voltage range of Signal DAC. This command bypasses the normal command processing and should be used with care. The (WRITE/READ RANGE DAC) command replaces the (SELECT VOLTAGE RANGE) command and the two commands should not be used together.

For calibration purposes, the (WRITE/READ OFFSET DAC) command allows the user setting and query of the 16 bit Offset DAC to directly control the offset of the output waveform. It is necessary to note that the (WRITE/READ OFFSET DAC) command may be affected by the (SELECT BANDWIDTH) command.

3.6 SAMPLE RATE PLLS

The ZT500PXI uses two PLLs to convert the selected 10 MHz reference into the sample clock. The first PLL is used by the Sequencer for memory access coordination, and the second is used by the Signal DAC for sample clocking. Figure 3-20 shows a diagram of the Sample Rate PLL function. Seven clock rates are provided: 20 MHz, 40 MHz, 80MHz, 100 MHz, 160 MHz, 200 MHz, and 300 MHz, (SELECT SAMPLE RATE). The ZT500PXI includes a high quality 2 ppm 10 MHz local reference, but allows select of the PXI CLK10 reference for system wide reference coordination, (SELECT REFERENCE).

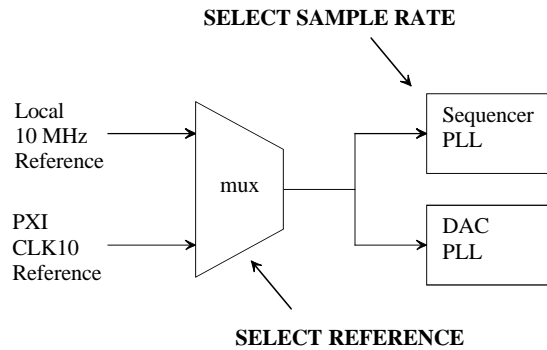


Figure 3-20 Sample Rate PLLs

3.7 STATUS REPORTING

The ZT500PXI maintains two mechanisms for status reporting: a status word located in shared PXIbus memory and an error queue maintained by the unit DSP processor. The status word is readable from the PXIbus without DSP intervention and is an indication of current unit status. This status can be read at the UNIT_STATUS location as described in Section 4.2. Status word bits are described in Table 3-1.

Bit #	Name	Description
15	nu	reserved
14	nu	reserved
13	nu	reserved
12	nu	reserved
11	nu	reserved
10	nu	reserved
9	nu	reserved
8	Run/Stop	1 = unit running
7	nu	reserved
6	nu	reserved
5	Error Log	1 = at least one entry in error log
4	nu	reserved
3	Busy	1 = unit performing command
2	Unit Fault	1 = unit self test failed
1	Self Test	1 = unit performing self test
0	Unit Ready	1 = unit ready for commands

Table 3-1. Status Word Bit Descriptions

The ZT500PXI maintains an error queue containing codes for faults conditions encountered during unit operation. These codes are listed in Table 3-2 below along with a brief description of the code meaning. The error log may be read by using the (READ ERROR) command.

Error Code	Source	Description
0504	Host	response buffer overrun
0940	EEPROM Controller	EEPROM timeout during read
0941	EEPROM Controller	EEPROM timeout during write
0D40	Mfg Info	invalid unit mfg info
0D41	Mfg Info	invalid baseboard mfg info
0D42	Mfg Info	invalid TRSE mfg info
1140	Memory	invalid memory page
150A	Command Processor	invalid command
1540	Command Processor	invalid mfg info device during read
1541	Command Processor	invalid mfg info device during write
1542	Command Processor	command locked out
1543	Command Processor	invalid parameter
1548	Command Processor	invalid command SW version, Unit P/N or Unit serial #
15C0	Command Processor	invalid command to the arbitrary waveform generator
15C1	Command Processor	query not supported
15C2	Command Processor	only query supported
1904	Flash	Flash programming or verify failed
1907	Flash	command locked out
1980	Flash	timeout while erasing
1981	Flash	timeout while writing
1982	Flash	flash verify failed
1D40	AWG Controller	Sequencer PLL unlocked
1D41	AWG Controller	Signal DAC PLL unlocked
1D80	AWG Controller	invalid sample rate to ZT500SM
1DC0	AWG Controller	invalid run/stop code
1DC1	AWG Controller	invalid bandwidth setting
1DC2	AWG Controller	invalid segment count
1DC3	AWG Controller	invalid segment length
1DC4	AWG Controller	invalid sample rate
1DC5	AWG Controller	invalid voltage range
1DC6	AWG Controller	invalid Range DAC setting
1DC7	AWG Controller	invalid Offset DAC setting
1DC8	AWG Controller	invalid advance mode setting
1DC9	AWG Controller	invalid trigger mode
1DCA	AWG Controller	invalid loop mode setting
1DCB	AWG Controller	invalid memory type select
1DCC	AWG Controller	invalid memory page
1DCD	AWG Controller	invalid segment or segment address
21C1	Trigger Controller	invalid PXI trigger control
21C2	Trigger Controller	invalid retigger mode setting
21C3	Trigger Controller	invalid set run trigger control
21CC	Trigger Controller	invalid front panel trigger control

Table 3-2. ZT500PXI Error Codes

3.8 MISCELLANEOUS COMMANDS

The ZT500PXI also supports readout of the unit part number and serial number (Read Model Number) and (Read Serial Number). The model number will be reported as the ASCII string "0001-001036". The serial number will be reported as a 16-bit unsigned binary value.

3.9 DIGITAL SIGNAL PROCESSOR

The ZT500PXI includes an embedded Texas Instruments TMS320VC5409 DSP for control both on-chip and external peripherals as well as implementation of waveform analysis functions. On-chip peripherals include static random-access memory (SRAM), serial ports, DMA controllers, and a phase-locked loop clock generator. The on-chip SRAM is used to store program and data during DSP operation and as PXIbus shared memory. Access to this memory is accomplished via the Texas Instrument PCI2040 PCI-to-DSP bridge. This bridge chip supports all PCI interface requirements such as configuration space registers and bus handshaking. The phase-locked loop clock generator is used to provide the on-chip operating clock frequency from the 10 MHz reference clock. A JTAG boundary scan connector allows DSP firmware development.

External memory peripherals for the DSP include Flash EEPROM memory and serial EEPROM memory. External Flash memory is used to store the DSP firmware that is downloaded upon power-up. The serial EEPROM is used to store configuration data in non-volatile memory.

Other external peripherals include module control registers and the AWG submodule. The DSP interfaces to the PXIbus host processor using the PXIbus interface registers. The module control registers allow the DSP to reset peripherals, select memory pages, and select the trigger and clock conditions, etc. The AWG submodule interface provides the AWG control/status and memory interface.

The embedded DSP performs supervisory control functions, but is also capable of high-speed data processing. Please contact ZTEC Instruments, Inc. for more information on custom DSP firmware development.

4 PXI INTERFACE & PROGRAMMING

4.1 PXI HARDWARE INTERFACE

The ZT500PXI uses the Texas Instruments PCI2040 PCI-to-DSP Bridge to handle PCI bus traffic. The PCI2040 responds to configuration space queries by the PCI bus and presents a simple four register interface for command and data transfers. PCI Base Address Register 1 points to this four register interface. Table 4-1 shows the ZT500PXI command and data transfer interface. All registers are 16 bits wide.

Address		Description
AD31-AD15	AD14-AD00	
set by PCIbus config	0000 ₁₆	Control Register
set by PCIbus config	0800 ₁₆	Data Register (auto-increment)
set by PCIbus config	1000 ₁₆	Address Register
set by PCIbus config	1800 ₁₆	Data Register (no increment)

Table 4-1. Low Level PCI Interface

The control register is set by the ZT500PXI initialization function to a value of 0101₁₆ and should be left unchanged. Host access to shared memory is accomplished by writing to the Address Register to set the target address and then reading/writing one of the data registers. Any access to address 0800₁₆ causes the contents of the Address Register to be incremented. This facility is useful for transferring command parameters or data blocks.

Access to ZT500PXI shared memory should use one of the following procedures:

Write to a single location

1. set the memory address by writing the address to the Address Register,
2. update the memory location by writing the new value to the Data Register (no increment).

Read from a single location

1. set the memory address by writing the address to the Address Register,
2. read the memory location value from the Data Register (no increment).

Write to a block of N locations

1. set the initial memory address by writing the first address to the Address Register,
2. update the memory locations by writing to the Data Register (auto-increment) N times.

Read from a block of N locations

1. set the initial memory address by writing the first address to the Address Register,
2. read the memory locations by reading from the Data Register (auto-increment) N times.

4.2 COMMAND INTERFACE

The ZTEC Instruments, Inc model ZT500PXI uses a non-queued, 1 command packet in – 1 response packet out, control technique that is encapsulated in the device driver software. Burst data transfers may proceed in parallel with command/response activity. Commands to and responses from the ZT500PXI are exchanged using shared memory located within the ZT500PXI DSP. Table 4-2 describes the memory map.

Address Register	Name	Description
4000 ₁₆	HOST_SIGNAL	host command activity signal
4001 ₁₆	HOST_COMMAND	host command code
4002 ₁₆ - 4041 ₁₆	HOST_PARAMETER	parameters required by the host command
4042 ₁₆	UNIT_STATUS	ZT500PXI status flags
4043 ₁₆	UNIT_SIGNAL	unit response activity signal
4044 ₁₆	UNIT_RESPONSE	unit response code
4045 ₁₆ - 4084 ₁₆	UNIT_PARAMETER	parameters reported with response

Table 4-2. Command/Response Memory Map

In order to exchange commands and responses, the host computer and ZT500PXI must execute the following steps:

1. the host must write a 0 to the UNIT_SIGNAL register,
2. the host must set up the HOST_COMMAND and HOST_PARAMETERS,
3. the host must write a 0002₁₆ to the HOST_SIGNAL register and begin monitoring the UNIT_SIGNAL register for a non-zero value,
4. the ZT500PXI monitors the HOST_SIGNAL register and will execute the HOST_COMMAND when a non-zero HOST_SIGNAL is detected,
5. upon completion of command processing the ZT500PXI will copy the command code into the UNIT_RESPONSE register, set up the UNIT_PARAMETER registers, and write a 0 to the HOST_SIGNAL register,
6. finally, the ZT500PXI will update the UNIT_SIGNAL register. This code, as shown in Table 4-3, defines the command processing result.

Response Code	Meaning
0001 ₁₆	CMD_DONE, command successfully completed
0002 ₁₆	CMD_UNK_CMD, unknown command
0004 ₁₆	CMD_INV_DATA, command parameter error
0008 ₁₆	CMD_REJECT, command rejected, incompatible with current state
0010 ₁₆	CMD_FAIL, requested operation failed

Table 4-3. ZT500PXI Response Signal Codes

4.3 DATA INTERFACE

Waveform records will be sent to the host using the shared memory located on the baseboard DSP chip. This memory will always begin at 4085_{16} , and has a maximum length of 800_{16} (2048_{10}). Both the Segment and Sequencer Tables are loaded using this memory. See the (UPDATE SEGMENT), (WRITE SEGMENT), and (WRITE SEQUENCE) commands for more information.

4.4 ZT500PXI HIGH LEVEL COMMAND SET

The ZT500PXI provides a set of commands for unit control and readout. The command set is diagrammed in Figure 4-1 and listed by command code in Table 4-4. These commands and the ZT500PXI responses are exchanged using the procedure outlined in Section 4.3 above.

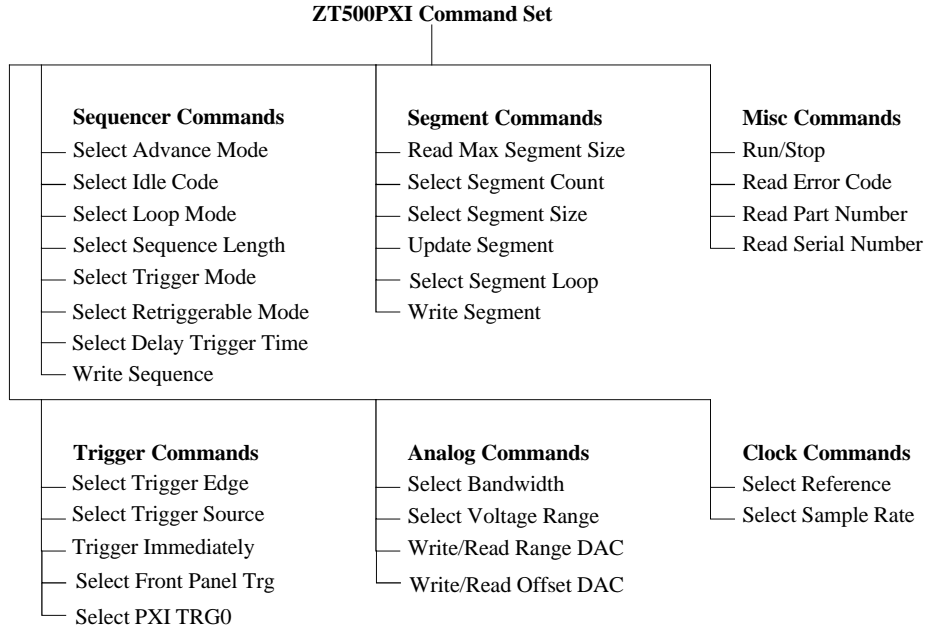


Figure 4-1. ZT500PXI Command Tree

Command Code	Query Code	Command Name
	8100 ₁₆	Read Part Number
	8101 ₁₆	Read Serial Number
0200 ₁₆	8200 ₁₆	Select Reference
0201 ₁₆	8201 ₁₆	Select Trigger Source
0202 ₁₆		Trigger Immediately
0203 ₁₆	8203 ₁₆	Select Trigger Edge
0204 ₁₆	8204 ₁₆	Select Front Panel Trg In/Out
0205 ₁₆	8205 ₁₆	Select PXI Trg0 In/Out
0300 ₁₆	8300 ₁₆	Run/Stop
0400 ₁₆	8400 ₁₆	Select Voltage Range
0401 ₁₆	8401 ₁₆	Select Sample Rate
0402 ₁₆	8402 ₁₆	Select Bandwidth
0403 ₁₆	8403 ₁₆	Select Idle Code
	8500 ₁₆	Read Max Segment Size
0501 ₁₆		Write Segment
0502 ₁₆	8502 ₁₆	Select Sequence Length
0503 ₁₆		Write Sequence Order
0504 ₁₆	8504 ₁₆	Select Loop Mode
0505 ₁₆	8505 ₁₆	Select Segment Count
0506 ₁₆	8506 ₁₆	Select Segment Size
0507 ₁₆	8507 ₁₆	Select Advance Mode
0508 ₁₆		Update Segment
0509 ₁₆	8509 ₁₆	Select Trigger Mode
050A ₁₆	850A ₁₆	Select Delay Trigger Time
050B ₁₆	850B ₁₆	Select Segment Loop
050C ₁₆	850C ₁₆	Select Retrigger
0600 ₁₆	8600 ₁₆	Write/Read Offset DAC
0601 ₁₆	8601 ₁₆	Write/Read Range DAC
	F000 ₁₆	Read Error Code

Table 4-4. ZT500PXI Command List

Each command described below is structured as a command code written to the HOST_COMMAND memory location and a list of parameters written to the HOST_PARAMETER memory block. The parameter list consists of a word count at offset 0 followed by the command parameters starting at offset 1. In a similar manner, the unit responses consist of a word count at location 0, followed by a parameter list. The keyword "none" indicates that there are no parameters. Some commands may be modified to a query by setting the command MSB. The supported forms of each command are shown as follows:

command name: param1,param2,etc.

command name? param1,param2,etc.

command and parameter descriptions.

command code

query code

Example:

SELECT TRIGGER EDGE: slope 0203₁₆
SELECT TRIGGER EDGE? none 8203₁₆
selects the trigger detection active edge. "slope" = 0000₁₆ for rising edge, 0020₁₆ for falling edge.

Note that the "word count" parameter is omitted in the command description but must be calculated and included before command processing is initiated by writing to the HOST_SIGNAL register.

4.5 COMMAND DESCRIPTIONS

READ ERROR CODE? none F000₁₆
reports the next entry from the unit error log. The command has no parameters. The ZT500PXI responds with the error code. If no errors were pending, an FFFF₁₆ is reported.

READ PART NUMBER? none 8100₁₆
reports the unit part number. The command has no parameters. The ZT500PXI responds with the ASCII string "0001-001036-XX" followed by one ASCII NULL, where the XX is a number that depicts the ZT500PXI options, ex. -00, -01 etc.

READ MAXIMUM SEGMENT SIZE? none 8500₁₆
reports the size of the segment store in the Segment Table. This value is determined as the overall Segment Table size (2097152) divided by the number of segments. The command has no parameters. The ZT500PXI responds with the 32 bit maximum segment size reported Most Significant Word (MSW) first followed by the Least Significant Word (LSW).

READ SERIAL NUMBER? none 8101₁₆
reports the unit serial number. The command has no parameters. The ZT500PXI responds with a 16 bit, unsigned unit serial number.

RUN/STOP: sw 0300₁₆
RUN/STOP? none 8300₁₆
enables or resets the waveform sequencer. Setting the "sw" parameter to 1 enables sequencer operation, setting "sw" to 0 stops waveform generation and resets the sequencer. There are no command response parameters. The ZT500PXI responds to the query with the unit run/stop state. NOTE: the unit run/stop state is also query-able from the UNIT_STATUS register without command handshaking overhead.

SELECT ADVANCE MODE: sw 0507₁₆
SELECT ADVANCE MODE? none 8507₁₆
selects the Waveform Sequencer segment advance mode. Setting "sw" to 0, AUTO mode, causes the Sequencer to automatically advance to the next segment as soon as the current segment is completed. Setting "sw" to 0080₁₆, TRIGGERED mode, causes the Sequencer to endlessly repeat the current segment until a trigger event is detected. There are no response parameters to the command. The ZT500PXI responds to the query with the advance mode setting.

SELECT BANDWIDTH: sw 0402₁₆
SELECT BANDWIDTH? none 8402₁₆
 selects an output bandlimit filter. The filters are 5 pole, lowpass Bessel (linear phase) filters with varying cutoff frequencies. The “sw” may be selected from the values in Table 4-5. There are no response parameters to the command. The ZT500PXI responds to the query with the filter setting.

Setting	Description
0000 ₁₆	Bypass, no output filter is used
0001 ₁₆	100 MHz lowpass Bessel filter
0002 ₁₆	50 MHz lowpass Bessel filter
0003 ₁₆	25 MHz lowpass Bessel filter

Table 4-5. ZT500PXI Output Filter Selections

SELECT DELAY TRIGGER TIME: 0, delay 050A₁₆
SELECT DELAY TRIGGER TIME? none 850A₁₆
 selects the amount of time the output will be delayed following an active trigger event. The code is an unsigned 32 bit number, with entry 0 as a 0, entry 1 as the MSW and entry 2 as the LSW. The delay time must be entered as a hexadecimal number. For example, 1000 usec delay requires the user to input 0000₁₆ in entry 1 and 03E8₁₆ in entry 2. There are no response parameters to the command. The ZT500PXI responds to the query with the current Delay Trigger code, MSW first followed by the LSW.

SELECT FRONT PANEL TRG IN/OUT: code 0204₁₆
SELECT FRONT PANEL TRG IN/OUT? none 8204₁₆
 selects the front panel trigger as an input or output. The “code” parameter is a 16 bit value. A 0040₁₆ is used for output and 0000₁₆ for an input. There are no response parameters to the command. The ZT500PXI responds to the query with the current front panel TRG in/out setting.

SELECT IDLE CODE: code 0403₁₆
SELECT IDLE CODE? none 8403₁₆
 selects the value sent to the Signal DAC and digital sync/marker outputs while the ZT500PXI is idle, i.e. not running and not downloading waveforms. The “code” parameter is a 16 bit value divided into an analog and two digital parts, see Section 3.3 for more information. There are no response parameters to the command. The ZT500PXI responds to the query with the current idle code.

SELECT LOOP MODE: sw 0504₁₆
SELECT LOOP MODE? none 8504₁₆
 selects the Waveform Sequencer loop mode. Setting “sw” to 0, SINGLE mode, causes the Sequencer to play the Sequencer Table one time, setting “sw” to 1, LOOP mode, causes the Sequencer to endlessly repeat the Sequencer Table. There are no response parameters to the command. The ZT500PXI responds to the query with the loop mode setting.

SELECT PXI TRG0 IN/OUT: code 0205₁₆
SELECT PXI TRG0 IN/OUT? none 8205₁₆
 selects the direction of the PXI TRG0. The “code” parameter is a 16 bit value. A 0001₁₆ is used for output and 0000₁₆ for an input. There are no response parameters to the command. The ZT500PXI responds to the query with the PXI TRG0 in/out setting.

SELECT RETRIGGER: code
SELECT RETRIGGER? none

050C₁₆
850C₁₆

selects the Retrigger mode. The Retrigger mode value is set to the 16 bit values indicated in Table 4-6. There are no response parameters to the command. The ZT500PXI responds to the query with the Retrigger setting.

Setting	Description
0000 ₁₆	Non-Retrigger
0001 ₁₆	Segment-Retrigger
0002 ₁₆	Sequence-Retrigger

Table 4-6. ZT500PXI Retrigger Selections

SELECT REFERENCE: sw
SELECT REFERENCE? none

0200₁₆
8200₁₆

selects the 10 MHz timebase reference used by the instrument to either the local 2 ppm reference or the PXI backplane reference clock. Setting “sw” to 0000₁₆ selects the local reference, setting “sw” to 0004₁₆ selects the PXI reference. There are no response parameters to the command. The ZT500PXI responds to the query with the reference clock select.

SELECT SAMPLE RATE: 0,rate
SELECT SAMPLE RATE? none

0401₁₆
8401₁₆

selects the sample rate in Hertz, Hz. The first entry is the sample rate MSW followed by the LSW as indicated in Table 4-7. There are no response parameters to the command. The ZT500PXI responds to the query with the sample rate in Hz, MSW first followed by the LSW.

MSW	LSW	Description
11E1 ₁₆	A300 ₁₆	300000000 Hz
0BEB ₁₆	C200 ₁₆	200000000 Hz
0989 ₁₆	6800 ₁₆	160000000 Hz
05F5 ₁₆	E100 ₁₆	100000000 Hz
04C4 ₁₆	B400 ₁₆	80000000 Hz
0262 ₁₆	5A00 ₁₆	40000000 Hz
0131 ₁₆	2D00 ₁₆	20000000 Hz

Table 4-7. ZT500PXI Sample Rate Selections

SELECT SEGMENT COUNT: cnt 0505₁₆
SELECT SEGMENT COUNT? none 8505₁₆
selects the number of Segment Table entries. The “cnt” parameter is used as an exponent of 2 in determining the number of segments, ex. setting “cnt” to 0 results in 1 segment (2^0), 1 results in 2 segments (2^1), 2 results in 4 segments (2^2), ... The “cnt” value may vary from 0 to 16 (1 to 65536 segments). This command modifies the segment size so the (SELECT SEGMENT SIZE) command should always be sent before this command. The maximum number of storage locations in each segment can be determined by dividing the memory size, 2097152, by the number of segments or by issuing the (READ MAXIMUM SEGMENT SIZE) command. There are no response parameters to the command. The ZT500PXI responds to the query with the segment count setting.

SELECT SEGMENT LOOP: cnt 050B₁₆
SELECT SEGMENT LOOP? none 850B₁₆
selects the number of times each segment will be performed before going to the next segment in the Sequencer Table. This is a 16 bit hexadecimal value that indicates the number of loops per segment. There are no response parameters to the command. The ZT500PXI responds to the query with the segment loop number.

SELECT SEGMENT SIZE: 0,size 0506₁₆
SELECT SEGMENT SIZE? none 8506₁₆
selects the number of locations used within each Segment Table segment. The first entry must be the value 0000₁₆, the “size” parameter is the 32 bit unsigned segment size. The maximum segment size is set by the (SELECT SEGMENT COUNT) command. This command allows the number of segment locations to be set in the range $4 \leq \text{size} \leq \text{maximum size}$. The maximum segment size is affected by the (SELECT SEGMENT COUNT) command, so this command should be sent before the (SELECT SEGMENT COUNT) command. There are no response parameters to the command. The ZT500PXI responds to the query with the segment size, MSW first followed by the LSW.

SELECT SEQUENCE LENGTH: len 0502₁₆
SELECT SEQUENCE LENGTH? none 8502₁₆
selects the number of entries in the Sequencer Table. The “len” parameter is incremented by 1 before being used by the Sequencer, ex. setting the sequence length to 0 results in a table length of 1. The sequence length may vary from 0 to 65535. There are no response parameters to the command. The ZT500PXI responds to the query with the sequence length setting 0 to 65535.

SELECT TRIGGER EDGE: slope 0203₁₆
SELECT TRIGGER EDGE? none 8203₁₆
fixes the active trigger edge using a selectable inverter. Setting the trigger “slope” parameter to 0000₁₆ disables the inverter and selects rising edge mode. Setting “slope” to 0020₁₆ enables the inverter and selects falling edge mode. A rising edge is defined as a lower voltage to higher voltage transition past the trigger level, falling edge is defined as a higher voltage to lower voltage transition past the trigger level. There are no response parameters to the command. The ZT500PXI responds to the query with the trigger slope setting.

SELECT TRIGGER MODE: sw0509₁₆**SELECT TRIGGER MODE? none**8509₁₆

selects the Waveform Sequencer response to trigger activity. In general, this command determines when the Sequencer initiates and pauses waveform generation. Valid trigger “sw” codes are defined in Table 4-8. There are no response parameters to the command. The ZT500PXI responds to the query with the trigger mode setting.

Code	Mode	Description
0000 ₁₆	Non-Triggered	trigger activity is ignored
0020 ₁₆	Triggered	waveform generation is initiated when a trigger event is detected, subsequent trigger events are ignored
0040 ₁₆	Trigger Gated	waveform generation is initiated when the trigger goes high and paused when the trigger goes low
0060 ₁₆	Timer Delay	selects delay trigger used along with (SELECT DELAY TRIGGER TIME) command

Table 4-8. ZT500PXI Trigger Modes

SELECT TRIGGER SOURCE: source0201₁₆**SELECT TRIGGER SOURCE? none**8201₁₆

selects the trigger source. Valid trigger “source” codes are defined in Table 4-9. There are no response parameters to the command. The ZT500PXI responds to the query with the trigger source setting.

Code	Source	Notes
0000 ₁₆	Software	see Trigger Immediately command
0001 ₁₆	PXI TTL0	
0002 ₁₆	PXI TTL1	
0003 ₁₆	PXI TTL2	
0004 ₁₆	PXI TTL3	
0005 ₁₆	PXI TTL4	
0006 ₁₆	PXI TTL5	
0007 ₁₆	PXI TTL6	
0008 ₁₆	PXI TTL7	
0009 ₁₆	PXI Star Trigger	
000A ₁₆	External Trigger Input	

Table 4-9. Trigger Source List

SELECT VOLTAGE RANGE: range0400₁₆**SELECT VOLTAGE RANGE? none**8400₁₆

selects the output voltage range in millivolts. When driving a low impedance load (50 or 75 ohms), this command sets the peak-to-peak voltage. When driving a high impedance load, this command sets the peak voltage. An example of this would be setting the output voltage to 1000, would result in a $0.5V_{\text{peak}}$ output ($1V_{\text{peak-to-peak}}$) for a 50 Ω load and a $1V_{\text{peak}}$ output ($\pm 1V$ or $2V_{\text{peak-to-peak}}$) for a high impedance load. The “range” parameter is specified in millivolts and may vary from 100₁₀ (0.1V) to 3500₁₀ (3.5V). There are no response parameters to the command. The ZT500PXI responds to the query with the current range setting.

TRIGGER IMMEDIATELY: none0202₁₆

causes a software trigger. This command temporarily overrides the current trigger source setting and forces a trigger event. There are no response parameters to the command.

UPDATE SEGMENT: seg,addr,len 0508₁₆
writes a block of values to the Segment Table. This command is intended for applications that require changes to the Segment Table with the shortest possible interruption of waveform generation. When this command is received, the Waveform Sequencer is Stopped, the Segment Table write is performed, and the Sequencer is then Run. The "seg" parameter selects the destination segment, the "addr" parameter is a 32 bit value identifying the first address within the segment to be written, and the "len" parameter is the number of values to be written. The source data should be written into PXIbus shared memory beginning at location 4085₁₆. The largest value for the "len" parameter is 800₁₆ (2048₁₆), the PXIbus data memory size, see Section 4.3. There are no response parameters to the command.

WRITE/READ OFFSET DAC: code 0600₁₆
WRITE/READ OFFSET DAC? none 8600₁₆
selects the offset DAC value. The offset DAC will be set to the 16 bit value entered by this command. There are no response parameters to the command. The ZT500PXI responds to the query with the offset DAC setting. The DAC offset is also set by the SELECT BANDWIDTH command so this command must be re-issued after changing the bandwidth.

WRITE/READ RANGE DAC: code 0601₁₆
WRITE/READ RANGE DAC: none 8601₁₆
selects the Range DAC value. The Range DAC is used to set the Signal DAC full scale range. The "code" parameter may vary from 0000₁₆ (< 0.1V_{peak}) to FFFF₁₆ (> 3.5V_{peak}). The Range DAC is set to calibrated values by the (SELECT VOLTAGE RANGE) command. When the (WRITE RANGE DAC) command is used, the ZT500PXI is being operated in the uncalibrated mode. There are no response parameters to the command. The ZT500PXI responds to the query with the current range DAC setting.

WRITE SEGMENT: seg,addr,len 0501₁₆
writes a block of values to the Segment Table. The "seg" parameter selects the destination segment, the "addr" parameter is a 32 bit value identifying the first address within the segment to be written, and the "len" parameter is the number of values to be written. The source data should be written into PXIbus shared memory beginning at location 4085₁₆. The largest value for the "len" parameter is 800₁₆ (2048₁₆), the PXIbus data memory size, see Section 4.3. There are no response parameters to the command.

WRITE SEQUENCE ORDER: addr,len 0503₁₆
writes a block of values to the Sequencer Table. The "addr" parameter is a 16 bit value identifying the first address within the Sequencer Table to be written and the "len" parameter is the number of values to be written. The source data should be written into PXIbus shared memory beginning at location 4085₁₆. The largest value for the "len" parameter is 800₁₆ (2048₁₀), the PXIbus data memory size, see Section 4.3. There are no response parameters to the command.

5

5 APPLICATIONS

5.1 TYPICAL UNIT CONFIGURATION

A typical ZT500PXI configuration sequence is given below:

1. set the number of segments to 16 SELECT SEGMENT COUNT 4
2. set the segment size to 1000 SELECT SEGMENT SIZE 0,1000
3. download 3 waveform segments use the block write to set up the first segment,
see Sections 4.2 and 4.3
WRITE SEGMENT 0,0,1000
use the block write to set up the second
segment
WRITE SEGMENT 1,0,1000
use the block write to set up the second
segment
WRITE SEGMENT 2,0,1000
4. set the Sequencer Table length to 3 not that the segment length setting is incremented by 1
before being used SELECT SEQUENCE LENGTH 2
5. download the Sequencer Table use a block write to set up the new Sequencer
Table, sequence = 0,1,2
WRITE SEQUENCE 0,3
6. configure the sequencer for loop mode, auto-advance, non-triggered mode
SELECT ADVANCE MODE 0
SELECT LOOP MODE 1
SELECT TRIGGER MODE 0
7. set the Range DAC for $\pm 0.5V$ output (HiZ) SELECT VOLTAGE RANGE 500
8. set the sample rate to 100 Msps SELECT SAMPLE RATE 0,100000000
9. set the bandwidth to 25 MHz SELECT BANDWIDTH 3
10. set the idle code for +full scale, DIG 2 low and DIG 1 high
SELECT IDLE CODE FFFD₁₆
11. begin waveform generation RUN/STOP 1

5.2 LARGE WAVEFORM SEGMENT/SEQUENCER TABLE LOAD

In some cases waveforms or sequence lists larger than the 2048 PXIbus shared memory block size must be loaded. In this case several WRITE SEGMENT or WRITE SEQUENCE commands must be issued to complete the load. For large waveform segments, the waveform segment download described in Section 5.1, Step 3 should be replaced by the following steps:

1. initialize this variables on the host `seg = 0`
2. initialize these variables on the host `addr = 0`
 `remaining len = waveform size`
3. select this block's size `len = minimum(2048,remaining len)`
4. download this block to PXIbus memory block write of "len" determined above
5. report the block to the ZT500PXI `WRITE SEGMENT seg,addr,len`
6. update the address and remaining len `addr = addr + len`
 `remaining len = remaining len - len`
7. repeat steps 2-5 until the remaining len = 0
8. go to the next segment and repeat until all segments have been downloaded

For a large Sequencer Table use the following steps:

1. initialize these variables on the host `addr = 0`
 `remaining len = table size`
2. select this block's size `len = minimum(2048,remaining len)`
3. download this block to PXIbus memory block write of "len" determined above
4. report the block to the ZT500PXI `WRITE SEQUENCE addr,len`
5. update the address and remaining len `addr = addr + len`
 `remaining len = remaining len - len`
6. repeat steps 2-5 until the remaining len = 0

5.3 PERIODIC WAVEFORM GENERATION

The ZT500PXI can be used as a flexible function generator, providing greater freedom of waveform selection and all of the common controls found in other more traditional function generators. However due to its method of generating waveforms, much care must be given to ensuring that true waveform periodicity is achieved, i.e. when the end of the Sequencer Table is reached and the unit loops back to the table start the waveform segments must mesh seamlessly. Because the ZT500PXI has a limited number of sample rate selections and finite memory, not all frequencies can be achieved exactly. Consider the following examples:

1. a 2 MHz sine wave

2 MHz can be simply generated by storing 1 cycle of the sine wave, sampled at 200 Msps, (1 cycle x 200 Msamples/sec divided by 2 Mcycles/sec = 100 samples)

2. a 2.1 MHz sine wave

for this case, 95.238.. samples are needed (1 cycle x 200 Msamples/sec divided by 2.1 Mcycles/sec). This is not physically realizable but if 21 cycles of the waveform are stored then 2000 samples will faithfully reproduce the desired signal (21 cycles x 200 Msamples/sec divided by 2.1 Mcycles/sec)

3. a 2.00001 MHz sine wave

for this case, 99.9995 samples are needed (1 cycle x 200 Msamples/sec divided by 2.00001 Mcycles/sec). Again, this is not physically realizable and a second problem arises if additional cycles are used: 200001 cycles and 20 Msamples would be needed, (200001 cycles x 200 Msamples/sec divided by 2.00001 Mcycles/sec). The ZT500PXI does not have this much memory!

As these examples demonstrate, there is always a trade-off between time and frequency when attempting to distinguish between two signals, the more similar they are in frequency, the more time is required to resolve the difference.

The required memory and sample rate can be calculated by the following procedure:

1. calculate the necessary time duration by taking the reciprocal of the required frequency resolution, ex. 10 kHz resolution requires $1/10000$ or 100 μ sec,
2. select a sample rate that is fast enough to generate the wave, i.e. $> 2x$ the frequency,
3. calculate the required memory size by multiplying the sample rate by the time duration, ex. 200 Msps x 100 μ sec = 20,000 samples,
4. select a segment count that is larger than the required memory size, ex segment count = 6 or $2097152 / 2^6 = 32768$.

The ZT500PXI with its 2M sample memory can resolve about a million to 1 ratio between the maximum and minimum periodic waveforms it can generate, ex. the 200 Msps rate used above can generate periodic waveforms from 100 MHz to DC in 100 Hz steps. Note that many frequencies in between the 100 Hz steps can be generated because of the way the relationship described above works, but the million to 1 ratio is a good rule of thumb.

5.4 VIDEO SIGNAL GENERATION, PART 1

The Segment and Sequencer Tables on the ZT500PXI can be used to build composite video signals for video monitor test by dividing the video signal into equal length time slices. Then by playing the time slices in correct order the composite signal could be regenerated. Tables 5-1 and 5-2 show an example:

Segment	Time Slice Description
0	DC, sync level
1	DC, black level
2	color burst tone
3	25% gray level
4	50% gray level
5	75% gray level
6	white level

Table 5-1. Composite Video Segment Table

Sequence List	Notes
1	beginning of sync
0	
1	end of sync
2	color burst
1	
3	
4	stair step
5	
6	
1	black & white stripes
6	
1	
etc.	

Table 5-2. Composite Video Sequence List

5.5 VIDEO SIGNAL GENERATION, PART 2

One issue when coordinating video signal generation between multiple pieces of equipment is that even small differences in timebase result in noticeable changes in video displays. The ZT500PXI's ability to accept external synchronization input provides a way to avoid this problem. When configured in a triggered advance and loop mode, such as Sequencer Mode 7, and each segment defined as a display line, the ZT500PXI waveform generation automatically keeps pace with the rest of the test system, avoiding video drift problems.

5.6 SEQUENCER CONFIGURATION

This section will discuss some application scenarios that can be used to understand the flexibility of the ZT500PXI. These applications, along with the discussion in Section 3.4 of this document, will give the user a deeper understanding of the ZT500PXI.

5.6.1 SEQUENCER SCENARIO 1

Figure 5-1 illustrates Sequence Scenario 1. This scenario could be used to delay output of a waveform until a system wide trigger event is generated and then endlessly repeat the sequence until the test is ended. In this configuration the Sequencer is set to endlessly repeat the Sequencer Table, automatically advance to the next segment when the current segment is completed, and initiate waveform generation after a trigger event is detected. The Sequencer should be configured using the command options illustrated at the top left corner of the figure.

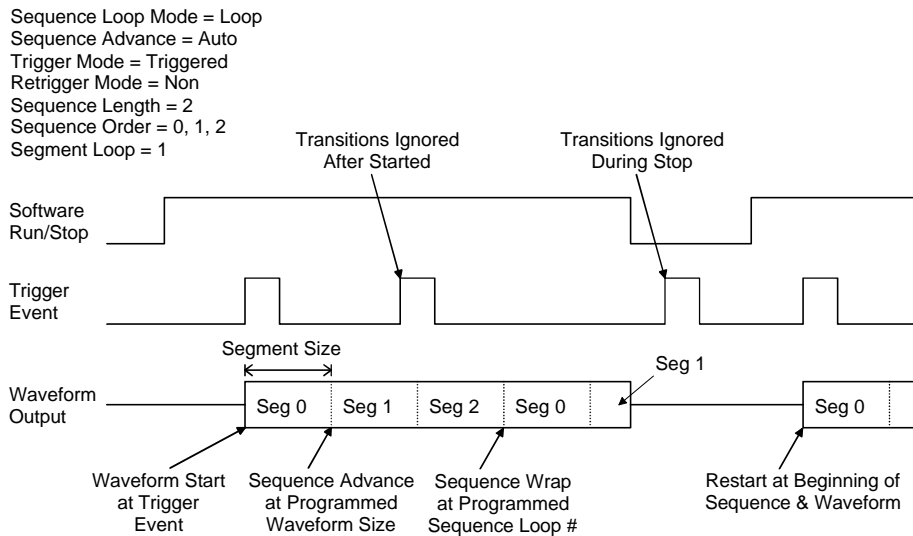


Figure 5-1. Sequence Scenario 1

In this example waveform generation is performed in the following steps:

1. the host computer issues the Run command,
2. waveform generation is delayed until the first trigger event at which time the first Sequencer Table entry, Segment 0, is started,
3. at the end of Segment 0 the Sequencer automatically advances to the next Sequencer Table entry, Segment 1,
4. segment advances continue until the end of the last Sequencer Table entry, Segment 2, then the Sequencer loops back to the start of the Sequencer Table, Segment 0, note that in this mode only the first trigger is used by the ZT500PXI,
5. part way through Segment 1 the host issues the Stop command and waveform generation ends,

6. trigger transitions are ignored while the ZT500PXI is Stopped,
7. the host restarts waveform generation by issuing a new Run command, note that the segment readout begins at the start of the Sequencer Table.

5.6.2 SEQUENCER SCENARIO 2

Figure 5-2 shows Sequence Scenario 2. This scenario could be used to simulate a push-to-talk radio. In this configuration the Sequencer is set to play the Sequencer Table once, automatically advance to the next segment when the current segment is completed, and initiate waveform generation when the selected trigger is in the high state only. The Sequencer should be configured using the command options illustrated at the top left corner of the figure.

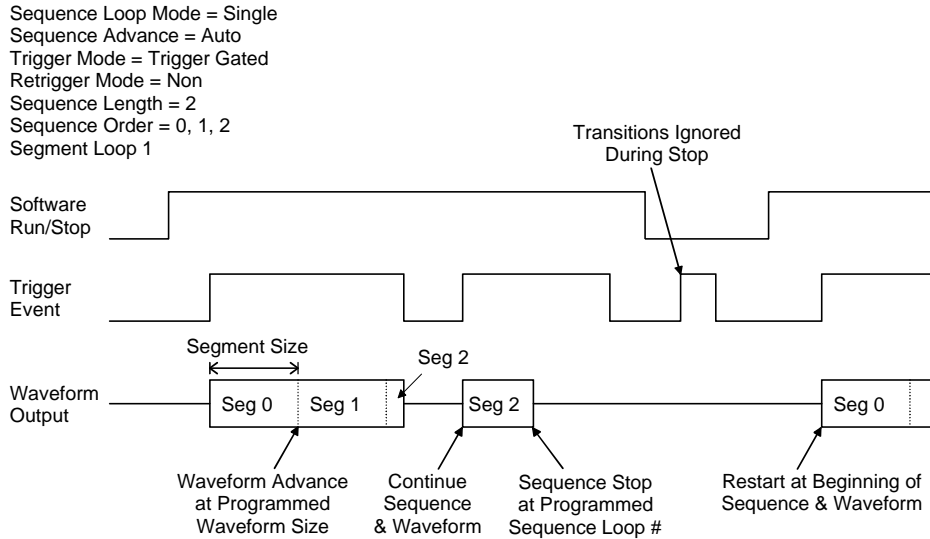


Figure 5-2. Sequence Scenario 2

In this example waveform generation is performed in the following steps:

1. the host computer issues the Run command,
2. waveform generation is delayed until the first trigger event at which time the first Sequencer Table entry, Segment 0, is started,
3. at the end of Segment 0 the Sequencer automatically advances to the next Sequencer Table entry, Segment 1,
4. segment advances continue until the trigger returns to the low state at which time waveform generation pauses, the location in Segment 2 is retained,
5. waveform generation resumes when the trigger returns to the high state and segment advances continue until the end of the last Sequencer Table entry, Segment 2, then waveform generation stops,
6. the host issues the Stop command,
7. trigger transitions are ignored while the ZT500PXI is Stopped,

8. the host issues a new Run command and waveform generation restarts upon the next trigger event, note that the segment readout begins at the start of the Sequencer Table.

5.6.3 SEQUENCER SCENARIO 3

Figure 5-3 shows Sequence Scenario 3. This could be used for performing a linearity and accuracy test on an analog channel by varying the output voltage at each segment to accommodate the input range of the analog channel from \pm full-scale. In this configuration the Sequencer is set to play the Sequencer Table once and advance to the next segment when a trigger event is detected. The Sequencer should be configured using the command options illustrated at the top left corner of the figure.

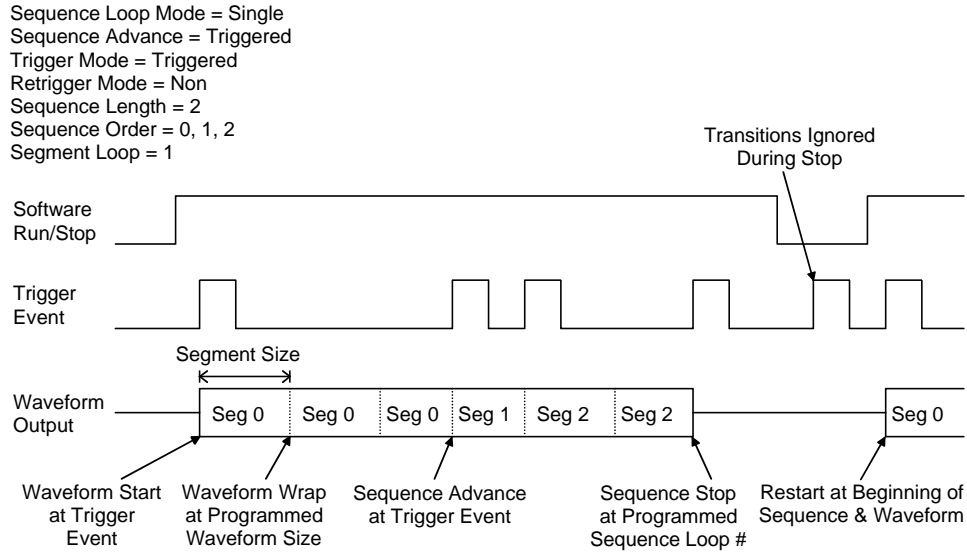


Figure 5-3. Sequence Scenario 3

In this example waveform generation is performed in the following steps:

1. the host computer issues the Run command,
2. waveform generation is delayed until the first trigger event at which time the first Sequencer Table entry, Segment 0, is started,
3. Segment 0 is repeated until part way through the third play of Segment 0 a trigger event is detected, at which time the Sequencer advances to the next Sequencer Table entry, Segment 1,
4. a second trigger event, part way through Segment 1, advances generation to the next Sequencer Table entry, Segment 2,
5. Segment 2 is repeated until part way through the second play of Segment 2 a trigger event is detected, at which time waveform generation is stopped,
6. the host issues the Stop command,
7. trigger transitions are ignored while the ZT500PX1 is Stopped,

8. the host issues a new Run command and waveform generation restarts upon the next trigger event, note that the segment readout begins at the start of the Sequencer Table.

5.6.4 SEQUENCER SCENARIO 4

Figure 5-4 shows Sequence Scenario 4. This could be used to perform pulse testing on Pulse Width Modulated (PWM) systems. In this configuration the Sequencer is set to play the Sequencer Table once, advance to the next segment, initiate waveform generation when a trigger event is detected, ignoring all triggers while the Sequence is played. Once the sequence is complete the Sequencer waits for a valid trigger event and repeats the Sequence once. The Sequencer should be configured using the command options illustrated at the top left corner of the figure.

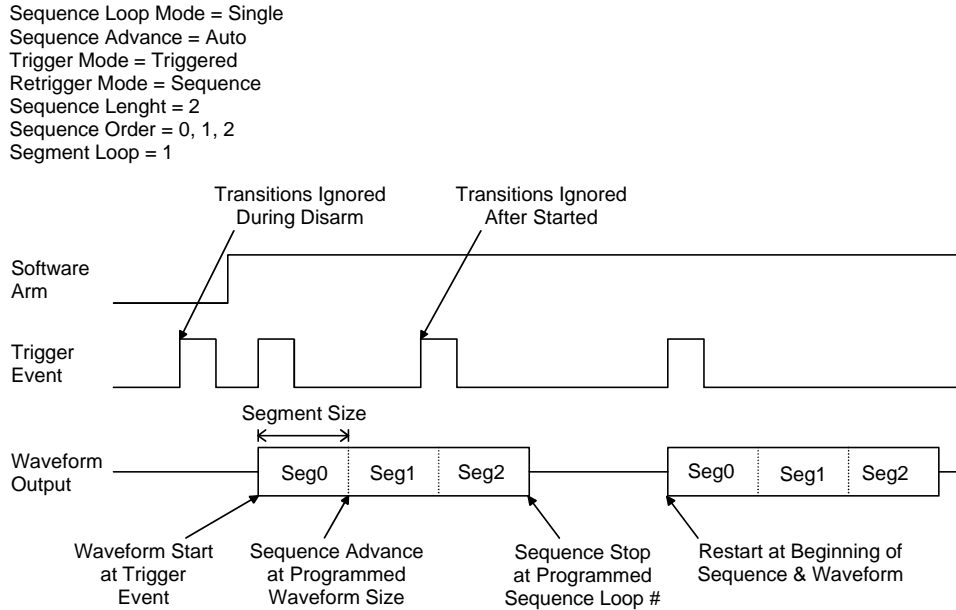


Figure 5-4. Sequence Scenario 4

In this example waveform generation is performed in the following steps:

1. the host computer issues the Run command,
2. waveform generation is delayed until the first trigger event at which time the first Sequencer Table entry, Segment 0, is started,
3. each Segment in the Sequencer Table is played well the Sequencer ignores all trigger events,
4. once the Sequence is complete the Sequencer waits for a valid trigger event,
5. once a valid trigger event is detected the Sequencer repeats the Sequence because of the Retrigger Mode being set to Sequence.

6 ZT500PXI DEMO SOFTWARE GUIDE

6.1 ZT500PXI FIND UTILITY

The ZTEC Instruments, Inc. model ZT500PXI is delivered with a LabVIEW™ panel to aid in identifying the VISA resource name associated with the ZT500PXI chassis slot. When run, the utility will scan the list of VISA resources and list all names associated with a ZT500PXI as well as the serial number of the identified unit. The software interface front panel is shown in Figure 6-1. The LabVIEW™ compatible software includes the entire source for the software interface.

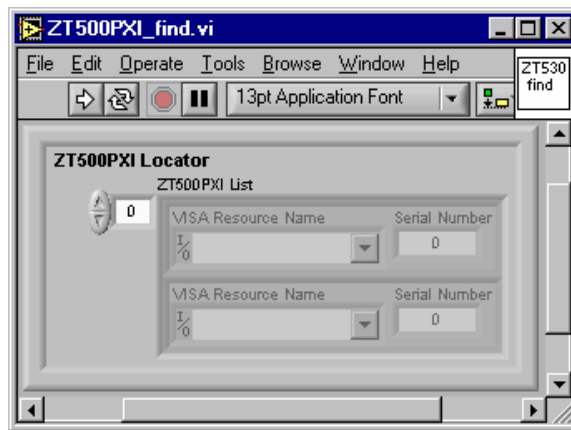


Figure 6-1 ZT500PXI Find Utility

6.2 ARBITRARY WAVEFORM GENERATOR (AWG) DEMO

6.2.1 AWG DEMO DESCRIPTION

The ZTEC Instruments, Inc. model ZT500PXI is delivered with a LabVIEW™ panel that demonstrates the arbitrary waveform generator (AWG) capabilities of the ZT500PXI. The software interface front panel is shown in Figure 6-2. The panel automates the initialization, sequence load, and segment load of the ZT500PXI. The LabVIEW™ compatible software includes the entire source for the software interface.

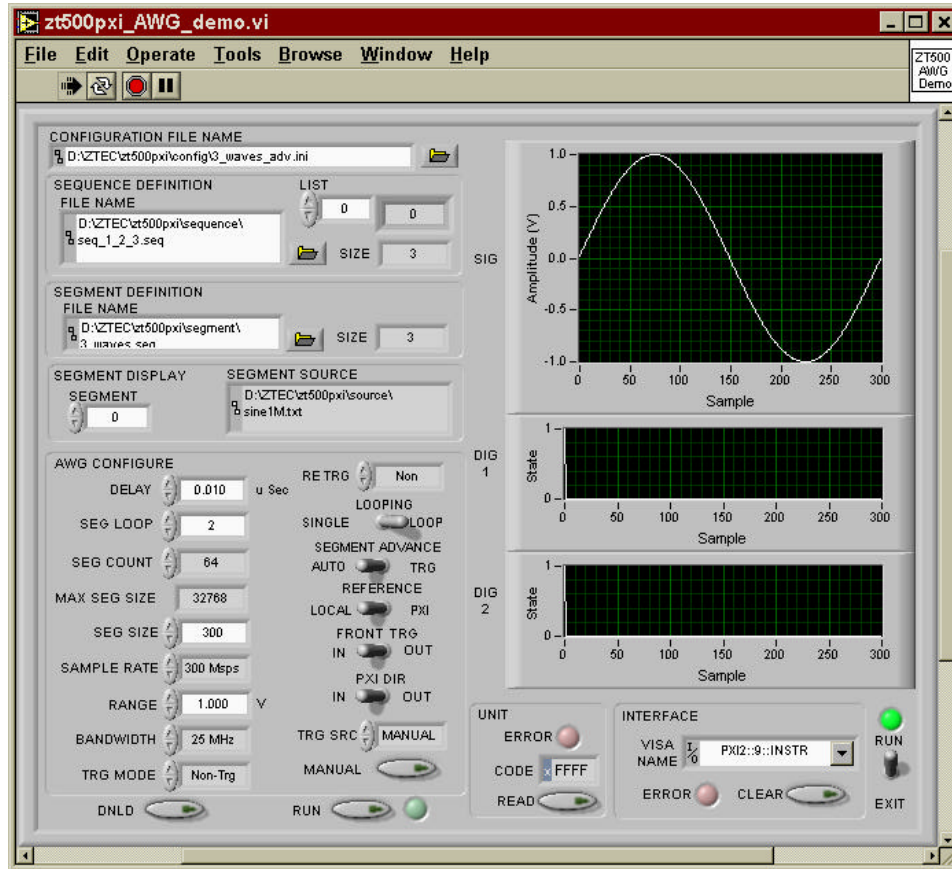


Figure 6-2. ZT500PXI Arbitrary Waveform LabVIEW™ Demo Panel

6.2.2 AWG DEMO CONTROLS AND DISPLAYS

Figure 6-2 shows the ZT500PXI AWG Demo Control Panel. The controls and displays are described below by panel section.

CONFIGURATION FILE NAME (located at the panel upper left)

this control selects a ".ini" file that can be used to quickly configure the ZT500PXI. The ".ini" file performs all unit configuration except for the actual download of segment and Sequencer Tables. The "default.ini" file is loaded when the panel is run. These ".ini" files can be created and examined with the utilities described in Section 6.2.3.

SEQUENCE DEFINITION (located at the panel upper left)

FILE NAME	selects a text file containing a Sequencer Table, see Section 6.2.3 for more details on the sequence file structure
LIST	allows display of the Sequencer Table
SIZE	shows the Sequencer Table length

SEGMENT DEFINITION (located at the panel center left)

FILE NAME	selects a text file containing a list of waveform segment source files, see Section 6.2.3 for more details on the segment file structure, <i>NOTE: only the number of values shown in the SEG SIZE control are read from the file, extra values are truncated and unused values are filled with 0</i>
SIZE	shows the number of segments described in the segment file

SEGMENT DISPLAY (located at the panel center left and right side)

SEGMENT	selects a segment for display in the SIG, DIG 1, and DIG 2 windows
SEGMENT SOURCE	shows the path and file name of the waveform segment being displayed
SIG	displays the Signal DAC portion of the waveform segment
DIG 1 & 2	displays the sync/marker portion of the waveform segment

AWG CONFIGURE (located at the panel lower left)

DELAY	selects delay time setting
SEG LOOP	selects the segment loop setting
SEG COUNT	selects the segment count setting
MAX SEG SIZE	displays the maximum storage space for a waveform segment
SEG SIZE	selects the number of storage location used for each segment
SAMPLE RATE	selects the DAC sample rate
RANGE	selects the DAC output voltage range
BANDWIDTH	selects the output bandlimit filter
TRG MODE	selects the sequencer trigger mode
RE TRIG	selects the retrigger sequencer mode
LOOPING	selects the sequencer looping mode
SEGMENT ADVANCE	selects the sequencer segment advance mode
REFERENCE	selects the 10 MHz reference clock source

FRONT TRG	selects the front panel trigger in or out
PXI DIR	selects the PXI TRG 0 direction in or out
TRG SRC	selects the trigger used by the sequencer, <i>NOTE: only rising edge triggers are allowed by the demo panel debug commands</i>
MANUAL	generates a trigger pulse

Miscellaneous Controls (located at the panel lower left)

DNLD	downloads the sequence and segment tables, the switch will stay illuminated until the downloads are complete
RUN	toggles the ZT500PXI between Run and Stop modes, the associated indicator is read from the UNIT_STATUS variable and illuminates when the ZT500PXI is running

UNIT (located at the panel lower center)

ERROR	when illuminated indicates that an error report is pending
CODE	indicates the most recently read error code, FFFF ₁₆ indicates that no error code was available
READ	reads an error code from the ZT500PXI

INTERFACE (located at the panel lower right)

VISA NAME	selects the ZT500PXI VISA resource name, <i>NOTE: this control must be set before the LabVIEW panel is started</i>
ERROR	when illuminated indicates that an interface error such as a timeout has occurred, the most common reason for an interface error is that an invalid VISA name has been selected
CLEAR	clears an interface error
RUN/EXIT	stops the LabVIEW panel in an orderly fashion, <i>NOTE: if the panel is stopped without using the RUN/EXIT switch the VISA resource name may become unavailable until the host computer is rebooted, the associated indicator is illuminated when the ZT500PXI is running</i>

6.2.3 AWG DEMO FILES AND UTILITIES

The AWG Demo makes use of a variety of files to simplify its use. These files and supporting utilities are:

“.ini” Configuration Files

these files contain a complete set of AWG demo panel control settings and are typically located in the \ZTEC\ZT500PXI\config directory. “.ini” files can be created with the ZT500PXI_make_ini.vi and examined with the ZT500PXI_read_ini.vi utilities also located in the "config" directory

“.seq” Sequence Files

these are text files containing a Sequencer Table and are typically located in the \ZTEC\ZT500PXI\sequence directory. The file should consist of integer values between 0 and 65535 with one value per line

“.seg” Segment Files

these are text files containing a list of file paths and names for waveform segment source files and are typically located in the \ZTEC\ZT500PXI\segment directory. The file should consist of file paths with one path per line

“.txt” Source Files

these are text files containing the waveform sample values and are typically located in the \ZTEC\ZT500PXI\source directory. The file should consist of base 10 integer values with one value per line. This format was selected for ease of interfacing with spreadsheet and related programs. Refer to Section 3.3 and Figure 3-4 for details on sample word formatting.

6.3 FUNCTION GENERATOR DEMO

The ZTEC Instruments, Inc. model ZT500PXI is delivered with a LabVIEW™ panel that demonstrates the function generator capabilities of the ZT500PXI. The software interface front panel is shown in Figure 6-3. The panel automates the initialization, sequence load, and segment load of the ZT500PXI. The LabVIEW™ compatible software includes the entire source for the software interface. Marker signals synchronous to the output waveform are output on the “DIG 1” front panel connector.

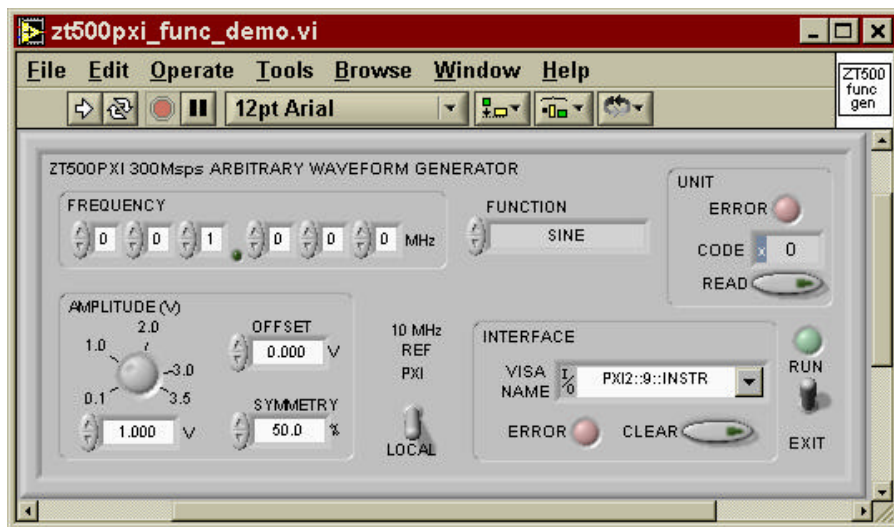


Figure 6-3. ZT500PXI Function Generator LabVIEW™ Demo Panel

6.3.1 FUNCTION GENERATOR CONTROLS AND DISPLAYS

Figure 6-3 shows the ZT500PXI Function Generator Demo Control Panel. The controls and displays are described below by panel section. *NOTE: signal output levels that do not fall within the ZT500PXI $\pm 3.5V$ output range will be clipped.*

FREQUENCY (located at the panel upper left)

digits selects the function generator output frequency in MHz, the available frequencies range from 1 kHz to 100 MHz. *Note: the panel will take several seconds to update when kHz range frequencies are selected, ex. 0.001 kHz or 50.001 kHz.*

AMPLITUDE (located at the panel lower left), for some signal types this control will be overridden,

dial selects the function generator non-DC signal amplitude
text control allows precise setting of the non-DC signal amplitude to 1 millivolt accuracy

OFFSET (located at the panel lower left), for some signal types this control will be overridden,

text control allows precise setting of the DC signal level to 1 millivolt accuracy

SYMMETRY (located at the panel lower left), for some signal types this control will be overridden,

text control allows setting of the signal symmetry or duty cycle to 0.1 accuracy, this control is only used for the square wave and logic signal types, *Note: for some frequencies not all symmetries can be achieved, in this case the output waveform will reflect the nearest available symmetry to the control setting.*

FUNCTION (located at the panel upper center)

menu list allows setting of the output signal type, menu entries are shown in Table 6-1. *Note: for all non-sine waveforms, wave shapes will degenerate below the maximum selectable frequency because of harmonic aliasing, ex. for the sawtooth setting, frequencies over 12 MHz are noticeably distorted.*

10 MHz REF (located at the panel lower center)

selector allows selection of the ZT500PXI 10 MHz reference source as either the local 2 ppm TCXO or the PXIbus CLK10 input

UNIT (located at the panel upper right)

ERROR when illuminated indicates that an error report is pending
CODE indicates the most recently read error code, FFFF₁₆ indicates that no error code was available
READ reads an error code from the ZT500PXI

INTERFACE (located at the panel lower right)

VISA NAME	selects the ZT500PXI VISA resource name, NOTE: this control must be set before the LabVIEW panel is run
ERROR	when illuminated indicates that an interface error such as a timeout has occurred, the most common reason for an interface error is that an invalid VISA name has been selected
CLEAR	clears an interface error
RUN/EXIT	stops the LabVIEW panel in an orderly fashion, NOTE: if the panel is stopped without using the RUN/EXIT switch the VISA resource name may become unavailable until the host computer is rebooted, the associated indicator is illuminated when the ZT500PXI is running

Signal Type	Description
sine	sine wave, amplitude and offset controls are active, the symmetry control is overridden
square	square wave, amplitude, offset, and symmetry controls are active
triangle	triangle wave, amplitude and offset controls are active, the symmetry control is overridden
sawtooth	sawtooth wave, amplitude and offset controls are active, the symmetry control is overridden
pulse	pulse wave, the output will range from 0V to "amplitude", the amplitude and symmetry controls are active, the offset control is overridden
TTL	logic wave, the output will range from 0V to 3.5V, the symmetry control is active, the amplitude and offset controls are overridden
ECL	logic wave, the output will range from -0.8V to -1.8V, the symmetry control is active, the amplitude and offset controls are overridden
uniform white noise	flat spectral and histogram noise, the noise bandwidth will be one half the selected sample rate, the sample rate will be chosen to include the value selected by the FREQUENCY control, the amplitude and offset controls are active, the symmetry control is overridden
Gaussian white noise	flat spectral and Gaussian histogram noise, the 3 dB noise bandwidth will be set by the FREQUENCY control, the amplitude and offset controls are active, the symmetry control is overridden
uniform pink noise	pink spectral and flat histogram noise, the output is generated from a uniform, white noise signal that has been filtered with a simple, one pole integrator, the amplitude and offset controls are active, the symmetry control is overridden
Gaussian pink noise	pink spectral and Gaussian histogram noise, the output is generated from a Gaussian, white noise signal that has been filtered with a simple, one pole integrator, the amplitude and offset controls are active, the symmetry control is overridden
DC	DC level, only the offset control is active, the amplitude and symmetry controls are overridden

Table 6-1. ZT500PXI Function Generator Signal Types