PCI 800 Series

PCI PnP Digital I/O Boards User's Manual for

PCI836A/C PCI848A/C PCI896A/C PCI8192A/C

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Digital I/O and Counter Boards

Data Acquisition and Process Control

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Product Warranty
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1. Introduction

The PCI800 series are 32-bit PCI bus architecture digital input/output and counter-timer data acquisition boards. They support 36 to 192 digital input/output lines and 3 counters. They come in 4 basic models, PCI836, PCI848, PCI896 and PCI8192.

Features

The PCI800 series has some very unique features and are listed below:

- 32-bit PCI bus Revision 2.2 compliant at 33MHz.
- PCI Bus 3.3V compatible.
- Intel 8255 compatible digital I/O ports.
- Intel 8254 compatible counter-timer.
- Opto-isolated input.
- Programmable interrupts.

Feature	PCI 836	PCI 848	PCI 896	PCI 8192
Number of digital channels – A Version	24	48	96	192
Number of digital channels – C Version	40	48	96	192
Number of counters – A Version	0	0	0	0
Number of counters – C Version	0	3	3	3
Number of 8255 compatible ports (8-bit)	3	6	12	24
Number of high current ports (16-bit) – C Version	1	0	0	0
Number of opto-isolated inputs – A Version	0	0	0	0
Number of opto-isolated inputs – C Version	1	1	1	1
Number of interrupt sources - A Version	0	0	0	0
Number of interrupt sources - C Version	3	10	10	10

Table 1-1 PCI800 Versions

Applications

The PCI800 series can be used in the following applications:

- Automation test equipment.
- TTL compatible status monitoring.
- Plant/Factory process control.
- Pulse counting.
- Frequency measurement.
- Frequency generation.
- Controlling and monitoring of any TTL compatible equipment.

Key Specifications

- 3,6,12 or 24 x 8-bit ports.
- 3 x 16-bit counters.
- Fully programmable digital input/output system.
- Fully programmable counter-timer system.
- Fully programmable interrupt support.

Software Support

The PCI800 series is supported by EDR Enhanced and comes with an extensive range of examples. The software will help you to get your hardware going very quickly. It also makes it easy to develop complicated control applications. All operating system drivers, utility and test software are supplied on the EDR Enhanced CD-Rom. The latest drivers can also be downloaded from the Eagle Technology website. For further support information see the Contact Details section.

Contact Details

Below are the contact details of Eagle Technology.

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2. Installation

This chapter describes how to install and configure the PCI800 for the first time. Minimal configuration is necessary; almost all settings are done through software. The PCI BIOS or operating system will take care of all resource assignments.

Package

PCI800 package will contain the following:

- PCI800 PCI board
- Eagle Technology Software CD-Rom.

Operating System Support

The PCI800 series support the Windows NT and Windows Driver Models (WDM) driver types. The operating systems are listed in the table below.

Board Type	Revision	Operating Systems	Driver Type
PCI836A/C	Revision 1	Windows NT/2000/98/ME	NT Sys, WDM PnP
PCI848A/C	Revision 1	Windows NT/2000/98/ME	NT Sys, WDM PnP
PCI896A/C	Revision 1	Windows NT/2000/98/ME	NT Sys, WDM PnP
PCI8192A/C	Revision 1	Windows NT/2000/98/ME	NT Sys, WDM PnP

Table 2-1 Operating System Support

Hardware Installation

This section will describe how to install your PCI board into your computer.

- Switch off the computer and disconnect from power socket.

Failure to disconnect all power cables can result in hazardous conditions, as there may be dangerous voltage levels present in externally connected cables.

- Remove the cover of the PC.
- Choose any open PCI slot and insert PCI board
- Insert bracket screw and ensure that the board sits firmly in the PCI socket.
- Replace the cover of the PC.
- Reconnect all power cables and switch the power on.
- The hardware installation is now completed.

Software Installation

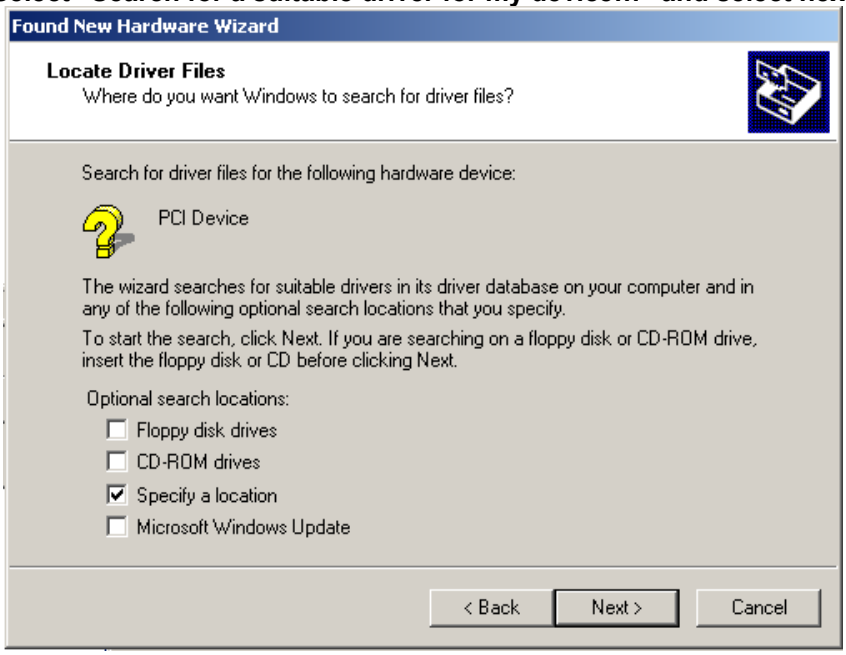
Windows 98/2000/ME

Installing the Windows 98/2000 device driver is a very straightforward task. Because it is plug and play Windows will auto detect the PCI board as soon as it is installed. No setup is necessary. You simply have to supply Windows with a device driver.

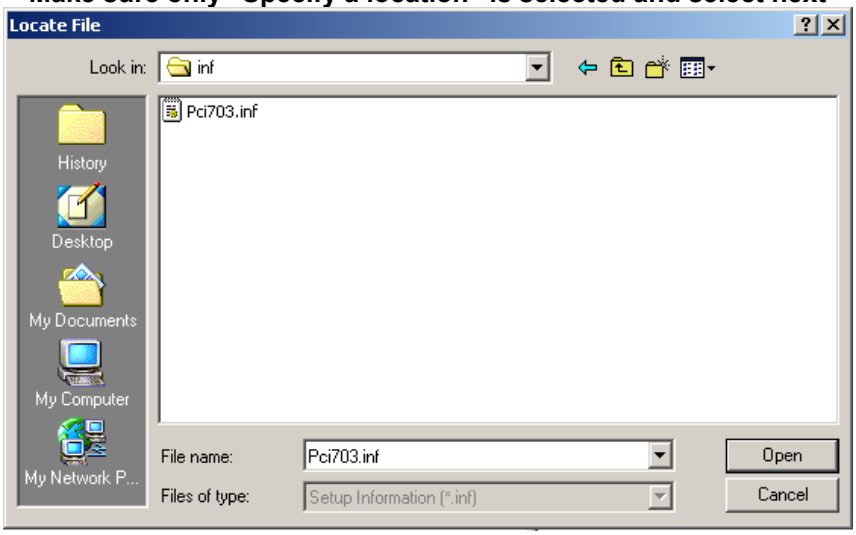
Wait until Windows detects the new hardware

Select Next

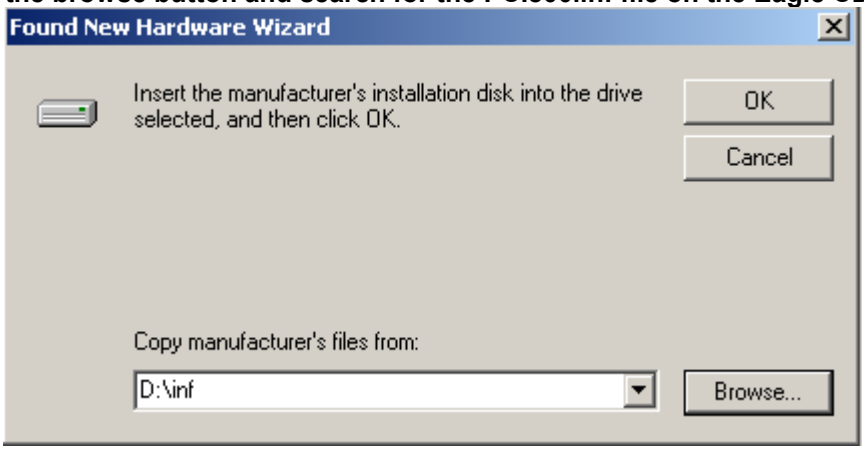
Select "Search for a suitable driver for my device…" and select next



Make sure only "Specify a location" is selected and select next

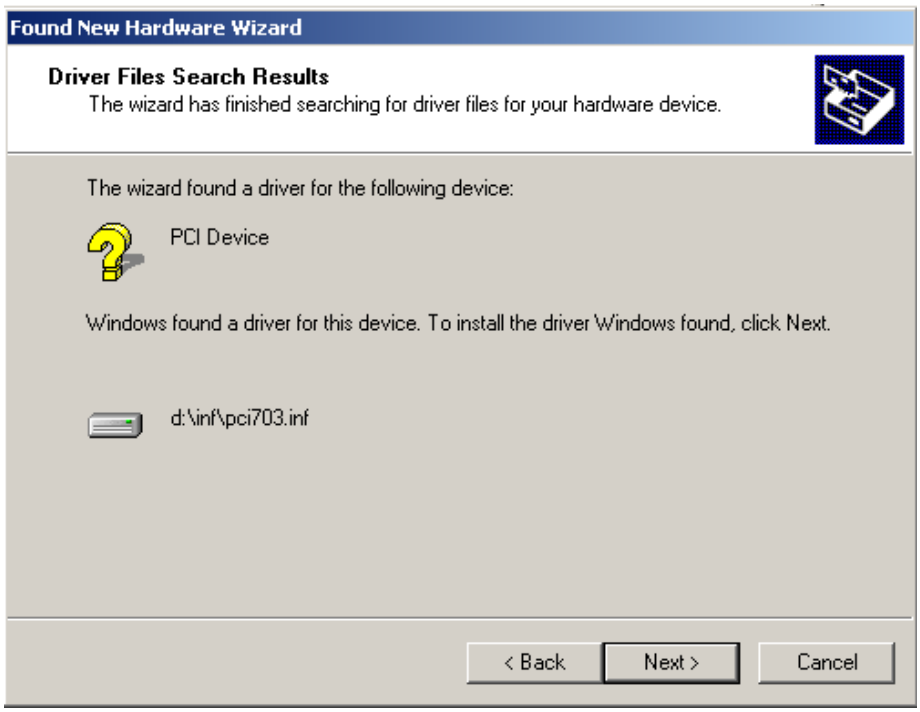


Select the browse button and search for the PCI800.inf file on the Eagle CD-Rom.

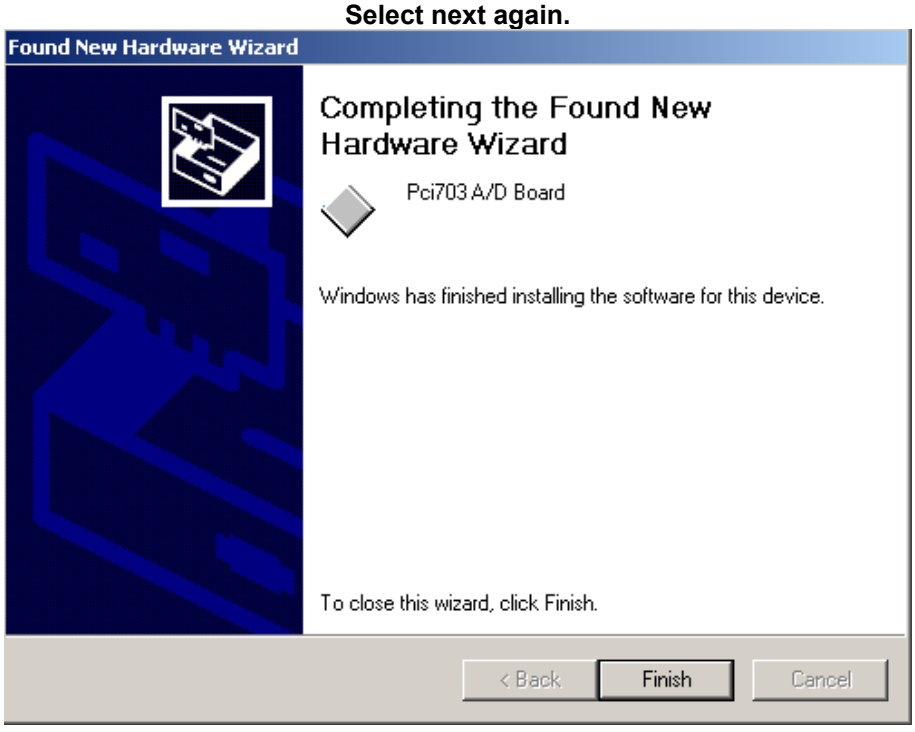


The driver is normally located in the <CDROM>:\EDRE\DRIVERS\WDM\PCI800 directory.

Select next when found.



Select next again.

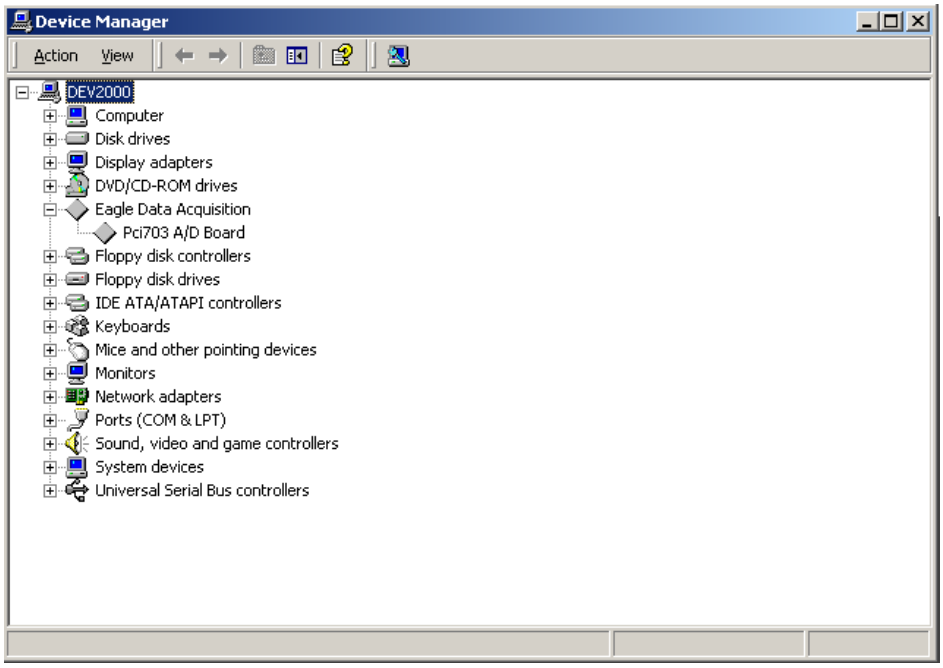


When done you might have to restart your computer.

Post installation

When done with the driver installation the device manager can be open to make sure the installation was a success.

- First make sure that the driver is working properly by opening the *Device Manager*.
- Check under the Eagle Data Acquisition list if your board is listed and working properly. See picture below.



- Clearly you can see that the PCI device is listed and working properly.
- Further open the control panel and then the *EagleDAQ* folder. This dialog should list all installed hardware. Verify your board's properties on this dialog. See picture below

Now the first part of your installation has been completed and ready to install the EDR Enhanced Software Development Kit.

- Run ***edreapi.exe*** found on the Eagle CD-Rom and follow the on screen instructions

Windows NT

The Windows NT driver supports both Windows NT4.0 and Windows 2000. It does not require any special setup. To install the Windows NT drivers simply run ***edrewinnt.exe*** on the Eagle CD-Rom. This will automatically install the device drivers. Restart your computer when done. Open the *EagleDAQ* folder in the control panel to check if your installation was successful.

If you are running on Windows 2000 and it detects a new device simply install a default driver, or so called placeholder. This will disable the device in the plug and play manager. The NT driver will take control of the device.

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3. Interconnections

The PCI800 series has connectors for digital I/O and counter-timers. The PCI800 range of boards are compatible with older board like the PC(I)36C and PC192A. The PCI800 boards make use of DB37, IDC20, IDC50 and DB25 connectors. The PCI836 is compatible with the older PC36B/C and PCI36C. The PCI848, PC896 and PC8192 are compatible with digital I/O connectors of the PC192A and the counter-timer connector on the PC14B.

External Connector and Accessories

Depending on the version of PCI800 board, different connectors are fitted of which some are the same. Use the table below as reference for each type of board.

Board Type	DB37(M) External	IDC20 Internal	IDC50 Internal	DB25(M) External
PCI836A	1	0	0	0
PCI836C	1	1	0	0
PCI848A	0	0	2	0
PCI848C	0	0	2	1
PCI896A	0	0	4	0
PCI896C	0	0	4	1
PCI8192A	0	0	8	1
PCI8192C	0	0	8	0

Table 3-1 PCI800 Connectors

Pin Assignments

PCI836A/C – DB37 (M) External

The table below shows the pin assignments for the DB37(M) connector found on the PCI836A and C. This is also compatible with the ISA PC36C and PCI36C.

Pin	Name	Pin	Name
1	+12V_FUSED	20	PC3
2	+5V_FUSED	21	PC2
3	DGND	22	PC1
4	PA0	23	PC0
5	PA1	24	PC4
6	PA2	25	PC5
7	PA3	26	PC6
8	PA4	27	PC7
9	PA5	28	DGND
10	PA6	29	DGND
11	PA7	30	DGND
12	PB0	31	DGND
13	PB1	32	DGND
14	PB2	33	EXT_TRIG
15	PB3	34	EXT_TRIG_RET
16	PB4	35	-12V_FUSED
17	PB5	36	NC
18	PB6	37	DGND
19	PB7		

Table 3-2 PCI836A/C External Connector – DB37 (M)

PCI836C – IDC20 (M) - Internal

The table below shows the pin assignments for the IDC20 (M) connector found on the PCI836C. This is also compatible with the PCI36C.

Pin	Name	Pin	Name
1	DO0	2	DO1
3	DO2	4	DO3
5	DO4	6	DO5
7	DO6	8	DO7
9	DO8	10	DO9
11	DO10	12	DO11
13	DO12	14	DO13
15	DO14	16	DO15
17	DGND	18	DGND
19	+5V_FUSED	20	+5V_FUSED

Table 3-3 PCI836A/C Internal Connector – IDC20 (M)

PCI836C – DB25 (M) – External via Cable

The table below shows the pin assignments for the DB25 (M) connector found on the PCI836C internal ribbon cable

Pin	Name	Pin	Name
1	DO0	14	DO1
2	DO2	15	DO3
3	DO4	16	DO5
4	DO6	17	DO7
5	DO8	18	DO9
6	DO10	19	DO11
7	DO12	20	DO13
8	DO14	21	DO15
9	DGND	22	DGND
10	+5V_FUSED	23	+5V_FUSED
11	NC	24	NC
12	NC	25	NC
13	NC		

Table 3-4 PCI836A/C External Connector via Internal Cable– DB25 (M)

PCI848/896/192 – IDC50 (M) Internal

The table below shows the pin assignments for the IDC(M) connector found on the PCI848/896/9192A and C. This is also compatible with the ISA PC192A.

Pin	Name	Pin	Name
1	PC7	2	DGND
3	PC6	4	DGND
5	PC5	6	DGND
7	PC4	8	DGND
9	PC3	10	DGND
11	PC2	12	DGND
13	PC1	14	DGND
15	PC0	16	DGND
17	PB7	18	DGND
19	PB6	20	DGND
21	PB5	22	DGND
23	PB4	24	DGND
25	PB3	26	DGND
27	PB2	28	DGND
29	PB1	30	DGND
31	PB0	32	DGND
33	PA7	34	DGND
35	PA6	36	DGND
37	PA5	38	DGND
39	PA4	40	DGND
41	PA3	42	DGND
43	PA2	44	DGND
45	PA1	46	DGND
47	PA0	48	DGND
49	+5V_FUSED	50	DGND

Table 3-5 PCI848/896/8192 IDC50 (M) Connector

PCI848/896/8192 C-Version – DB25 (M) - External

The table below shows the pin assignments for the DB25 (M) connector found on the PCI848C, PCI896C and PCI192C. This is also compatible with the PC14B counter-timer connector.

Pin	Name	Pin	Name
1	+12V_FUSED	14	NC
2	-12V_FUSED	15	NC
3	NC	16	NC
4	CLK0	17	NC
5	GATE0	18	OUT0
6	OUT2	19	CLK2
7	CLK1	20	GATE2
8	OUT1	21	GATE1
9	DGND	22	NC
10	+5V_FUSED	23	NC
11	NC	24	EXT_TRIG_RET
12	EXT_TRIG	25	FREQ_IN
13	FREQ_OUT		

Table 3-6 PCI848/896/8192C External Connector – DB25 (M)

Signal Definitions

This sections deal with all the signals abbreviations.

Signal	Description
PA0-7	8255 PPI Port A
PB0-7	8255 PPI Port B
PB0-7	8255 PPI Port C
EXT_TRIG	External Trigger to Opto-Isolator
EXT_TRIG_RET	External Trigger Return from Opto-Isolator – Can be jumpered to digital ground.
DGND	Digital ground.
+5V_FUSED	Fused +5V power supply line (PCI848C, PCI896C, PCI8192C – MAX 200mA, PCI836 - MAX 1.5A).
+12V_FUSED	Fused +12V power supply line (MAX 200mA).
-12V_FUSED	Fused –12V power supply line (MAX 200mA).
CLK0-2	External clock input

GATE0-2	External gates
OUT0-2	Counter outputs
FREQ_OUT	Frequency output from frequency scaler
FREQ_IN	External frequency input
NC	Not Connected

Table 3-7 Signal definitions

Pin Descriptions

Digital Inputs/Outputs (PA0-7, PB0-7, PC0-7)

These lines are connected to the 3 ports of the 8255 PPI. Each port can be configured as either an input or an output.

External Trigger System (EXT_TRIG, EXT_TRIG_RET)

The external trigger is an optically isolated digital line that can be read from software and trigger an interrupt. This is only available on the C-models.

FREQ_IN and FREQ_OUT

These pins relate to the frequency scaler. The output comes directly from the scaler. The input can be used to drive the frequency scaler from a source other than the onboard crystal. This is software selectable.

CLK0-2

These are the external clock inputs. The clock source is jumper selectable.

GATE0-2

These are the external gate inputs. The gate source is jumper selectable.

OUT0-2

These are the outputs of each counter-timer.

+5V Power Pin (+5V)

This is a +5 volt fused power pin.

+12V Power Pin (+12V)

This is a +12 volt fused power pin.

-12V Power Pin (-12V)

This is a -12 volt fused power pin.

Digital Ground (DGND)

All digital ground signals should be connected to this pin.

4. Programming Guide

The PCI800 series is supplied with a complete software development kit. EDR Enhanced (EDRE SDK) comes with drivers for many operating systems and a common application program interface (API). The API also serves as a hardware abstraction layer (HAL) between the control application and the hardware. The EDRE API makes it possible to write an application that can be used on all hardware with common sub-systems.

The PCI800 series can also be programmed at register level, but it is not recommended. A detailed knowledge of the PCI800 series is needed and some knowledge about programming Plug and Play PCI devices. We recommend that you only make use of the software provided by Eagle Technology.

EDR Enhanced API

The EDR Enhanced SDK comes with both ActiveX controls and a Windows DLL API. Examples are provided in many different languages and serve as tutorials. EDRE is also supplied with a software manual and user's guide.

The EDRE API hides the complexity of the hardware and makes it really easy to program the PCI800 board. It has got functions for each basic sub-system and is real easy to learn.

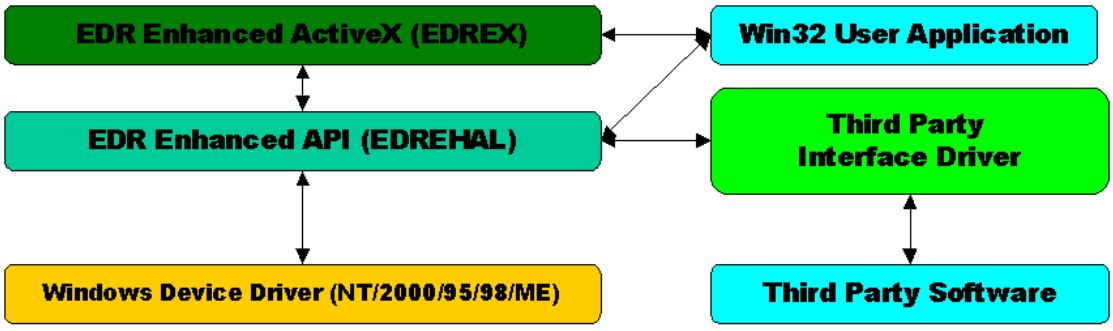


Figure 4-1 EDR Enhanced Design

Digital Inputs/Outputs

Depending on the version that you have the PCI800 device can have up to 192 digital lines. Please refer to your particular version for specific details.

Reading the Digital Inputs

A single call is necessary to read a digital I/O port.

API-CALL

Long EDRE_DioRead(ulng Sn, ulng Port, ulng *Value)

The serial number, port, and a pointer to variable to hold the result must be passed by the calling function. A return code will indicate if any errors occurred.

ACTIVEX CALL

Long EDREDioX.Read(long Port)

Only the port-number needs to be passed and the returned value will either hold an error or the value read. If the value is negative an error did occur.

Writing to the Digital Outputs

A single call is necessary to write to a digital I/O port.

API-CALL

Long EDRE_DioWrite(ulng Sn, ulng Port, ulng Value)

The serial number, port, and a value must be passed by the calling function. A return code will indicate if any errors occurred.

ACTIVEX CALL

Long EDREDioX.Write(long Port, ulng Value)

The port number and value to be written needs to be passed and the returned value holds an error or the value read. If the value is negative an error did occur.

Port	PPI No	Assigned Number	Width	Description
PCI836A				
A	0	0	8-bits	Port A
B	0	1	8-bits	Port B
C	0	2	8-bits	Port C
PCI836C				
A	0	0	8-bits	Port A
B	0	1	8-bits	Port B
C	0	2	8-bits	Port C
D	NONE	3	16-bits	High current output port
Opto	0	4	1-bit	Opto-isolated external trigger line
PCI848A				
0A	0	0	8-bits	Port A
0B	0	1	8-bits	Port B
0C	0	2	8-bits	Port C
1A	1	3	8-bits	Port A
1B	1	4	8-bits	Port B
1C	1	5	8-bits	Port C
PCI848C				
0A	0	0	8-bits	Port A
0B	0	1	8-bits	Port B
0C	0	2	8-bits	Port C
1A	1	3	8-bits	Port A
1B	1	4	8-bits	Port B
1C	1	5	8-bits	Port C
Opto	NONE	6	1-bit	Opto-isolated external trigger line
PCI896A				
0A	0	0	8-bits	Port A
0B	0	1	8-bits	Port B
0C	0	2	8-bits	Port C
1A	1	3	8-bits	Port A
1B	1	4	8-bits	Port B
1C	1	5	8-bits	Port C

2A	2	6	8-bits	Port A
2B	2	7	8-bits	Port B
2C	2	8	8-bits	Port C
3A	3	9	8-bits	Port A
3B	3	10	8-bits	Port B
3C	3	11	8-bits	Port C
PCI896C				
0A	0	0	8-bits	Port A
0B	0	1	8-bits	Port B
0C	0	2	8-bits	Port C
1A	1	3	8-bits	Port A
1B	1	4	8-bits	Port B
1C	1	5	8-bits	Port C
2A	2	6	8-bits	Port A
2B	2	7	8-bits	Port B
2C	2	8	8-bits	Port C
3A	3	9	8-bits	Port A
3B	3	10	8-bits	Port B
3C	3	11	8-bits	Port C
Opto	NONE	12	1-bit	Opto-isolated external trigger line
PCI8192A				
0A	0	0	8-bits	Port A
0B	0	1	8-bits	Port B
0C	0	2	8-bits	Port C
1A	1	3	8-bits	Port A
1B	1	4	8-bits	Port B
1C	1	5	8-bits	Port C
2A	2	6	8-bits	Port A
2B	2	7	8-bits	Port B
2C	2	8	8-bits	Port C
3A	3	9	8-bits	Port A
3B	3	10	8-bits	Port B
3C	3	11	8-bits	Port C
4A	4	12	8-bits	Port A
4B	4	13	8-bits	Port B
4C	4	14	8-bits	Port C
5A	5	15	8-bits	Port A
5B	5	16	8-bits	Port B
5C	5	17	8-bits	Port C
6A	6	18	8-bits	Port A
6B	6	19	8-bits	Port B
6C	6	20	8-bits	Port C
7A	7	21	8-bits	Port A
7B	7	22	8-bits	Port B
7C	7	23	8-bits	Port C
PCI8192C				
0A	0	0	8-bits	Port A
0B	0	1	8-bits	Port B
0C	0	2	8-bits	Port C
1A	1	3	8-bits	Port A
1B	1	4	8-bits	Port B
1C	1	5	8-bits	Port C
2A	2	6	8-bits	Port A
2B	2	7	8-bits	Port B
2C	2	8	8-bits	Port C
3A	3	9	8-bits	Port A
3B	3	10	8-bits	Port B
3C	3	11	8-bits	Port C
4A	4	12	8-bits	Port A
4B	4	13	8-bits	Port B
4C	4	14	8-bits	Port C
5A	5	15	8-bits	Port A
5B	5	16	8-bits	Port B
5C	5	17	8-bits	Port C
6A	6	18	8-bits	Port A
6B	6	19	8-bits	Port B
6C	6	20	8-bits	Port C
7A	7	21	8-bits	Port A
7B	7	22	8-bits	Port B
7C	7	23	8-bits	Port C
Opto	NONE	24	1-bit	Opto-isolated external trigger line

Table 4-1 Port Assignments

Counters

The counter sub-system is supported by functions to Write, Read, Configure and controlling the gate. There are 3 counters and 1 frequency generator. Counter-timers are only supported by the PCI848C, PCI896C and PCI192C. The table below shows the relation of the counters and their software assigned numbers. The figure below shows the architecture of the counter-timer subsystem.

Counter	Assigned Number	Description
CT1	0	Counter 0
CT2	1	Counter 1
CT3	2	Counter 2
FREQ	3	Frequency Scaler

Table 4-2 Counter Assignment

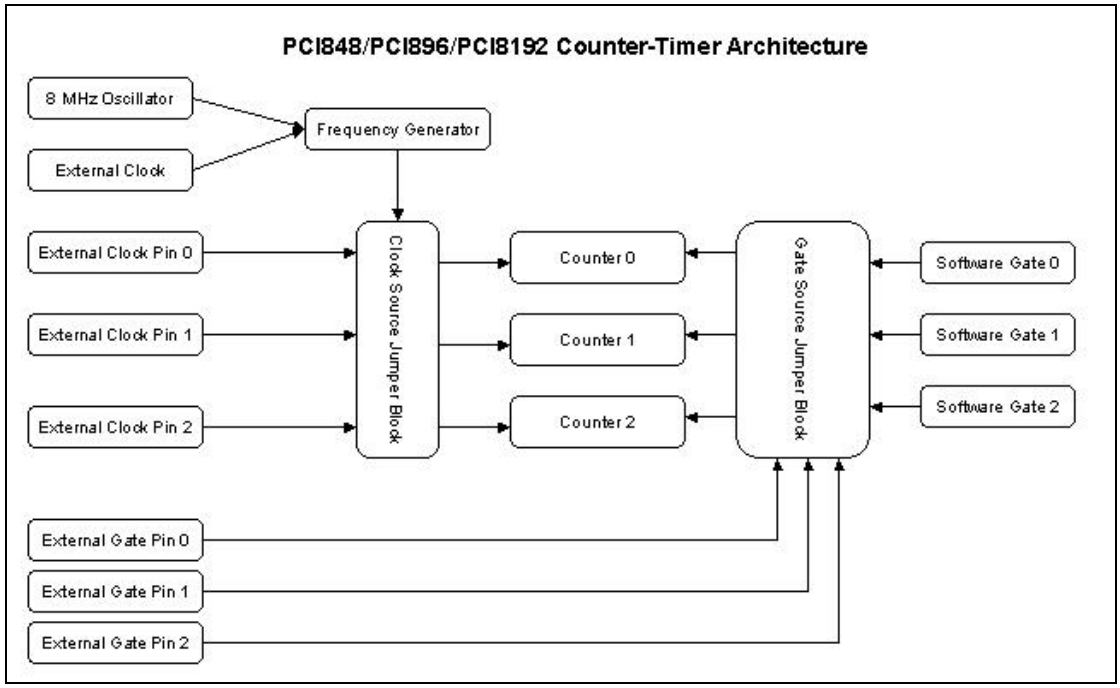


Figure 4-2 Counter-Timer Architecture

Writing the initial counter value

A single call is necessary to write a counter's initial load value.

API-CALL

Long EDRE_CTWrite(ulng Sn, ulng Ct, ulng Value)

The serial number, counter-number, and a value must be passed by the calling function. A return code will indicate if any errors occurred.

ACTIVEX CALL

Long EDRECTX.Write(long Port, ulng Value)

The counter-number and a value must be passed by the calling function. A return code will indicate if any errors occurred.

Counter	Assigned Number	Resolution
CT1	0	16-bits
CT2	1	16-bits
CT3	2	16-bits
FREQ	3	8-bits

Table 4-3 Counter Resolution

Reading the counter value

A single call is necessary to read a counter.

API-CALL

Long EDRE_CTRead(ulng Sn, ulng Ct, pulng Value)

The serial number, counter-number, and a reference parameter must be passed by the calling function. A return code will indicate if any errors occurred.

ACTIVEX CALL

Long EDRECTX.Read(long Port)

The counter number must be passed by the calling function. If the return code is negative it means an error occurred, otherwise it will be the value read from the counter.

Counter	Assigned Number	Resolution
CT1	0	16-bits
CT2	1	16-bits
CT3	2	16-bits
FREQ	3	Not supported

Table 4-4 Counter Resolution

Configuring a counter

A single call is necessary to configure a counter.

API-CALL

Long EDRE_CTConfig(ulng Sn, ulng Ct, ulng Mode, ulng Type, ulng ClkSrc, ulng GateSrc)

The serial number, counter-number, mode, type, clock source and gate source is needed to specify a counter's configuration. A return code will indicate if any errors occurred.

ACTIVEX CALL

Long EDRECTX.Configure(long ct, long mode, long type, ulng source, ulng gate)

The counter-number, mode, type, clock source and gate source is needed to specify a counter's configuration. A return code will indicate if any errors occurred.

Only the counter mode, clock source and type parameters are used by the PCI800. The table below shows the options for each parameter.

<table>
<tr><th>Parameter</th><th>Description</th></tr>
<tr><td>Sn</td><td>Serial Number</td></tr>
<tr><td>Ct</td><td>Counter Number:
0 : Counter 1
1 : Counter 2
2 : Counter 3
3 : Frequency Scaler</td></tr>
<tr><td>Mode</td><td>
<table>
<tr><td>Counter</td><td>Mode</td></tr>
<tr><td>0</td><td>82c54 Mode
See 82c54 datasheet</td></tr>
<tr><td>1</td><td>82c54 Mode</td></tr>
<tr><td>2</td><td>82c54 Mode</td></tr>
<tr><td>3</td><td>0 : Pulse Mode – Pulse on each terminal count
1 : Toggle Mode – Change state on each terminal count</td></tr>
</table>
</td></tr>
<tr><td>Type</td><td>
<table>
<tr><td>Counter</td><td>Type</td></tr>
<tr><td>0-2</td><td>0 : Binary Counting (16-bits)
1 : Binary Coded Decimal (BCD)
4 decades</td></tr>
<tr><td>3</td><td>Not supported</td></tr>
</table>
</td></tr>
<tr><td>Source</td><td>0 : Internal (8MHz)
1 : External (External connector)</td></tr>
</table>

	Only supported by the frequency scaler.
Gate	<not used>

Table 4-5 Counter Configuration

Controlling the counter gate

A single call is necessary to control a counter's gate. This function call is invalid for the frequency generator (counter 3). Counter 3 does not have a gate. For counters 0-2 the gate and clock source are selected via jumpers on the PCI800 board if supported.

API-CALL
Long EDRE_CTSoftGate(ulng Sn, ulng Ct, ulng Gate)
The serial number, counter-number and gate are needed to control a counter's gate. A return code will indicate if any errors occurred.

ACTIVEX CALL
Long EDRECTX.SoftGate(ulng Ct, ulng Gate)
The counter-number and mode is needed to control a counter's gate. A return code will indicate if any errors occurred.

These values are acceptable as a gate source.

Value	Description
0	Gate disabled
1	Gate enabled

Table 4-6 Gate Configuration

Programming Interrupts

The PCI800 can generate interrupts from different sources, which include digital inputs and counters. The interrupt sub-system is totally programmable and includes functions to configure, enable and disable interrupts.

WARNING!

Be careful when programming the interrupt sub-system because it is easy to generate interrupts that is faster than what Windows can service. Don't try and generate interrupt faster than 10KHz. This will not work. Remember this is 10KHz in total, and not per source. The PCI800 interrupt service routine will stop servicing interrupts if at any stage it is still busy with a previous interrupt and the next one is generated.

Configuring the Interrupt sub-system

A single call is necessary to configure the interrupt sub-system.
ACTIVEX-CALL
Long EDREIntX.IntConfigure(long Source, long Mode, long Type)

<table>
<tr><th>Parameter</th><th>Type</th><th>Description</th></tr>
<tr><td>Source</td><td>long</td><td>
<table>
<tr><td>Source</td><td>PCI836C</td><td>PCI848C
PCI896C
PCI8192C</td></tr>
<tr><td>0</td><td>Port C Line 0</td><td>PPI 0 Port A Line 0</td></tr>
<tr><td>1</td><td>Port C Line 4</td><td>PPI 0 Port A Line 1</td></tr>
<tr><td>2</td><td>Opto-Isolator</td><td>PPI 0 Port A Line 2</td></tr>
<tr><td>3</td><td>NONE</td><td>PPI 0 Port A Line 3</td></tr>
<tr><td>4</td><td>NONE</td><td>PPI 0 Port A Line 4</td></tr>
<tr><td>5</td><td>NONE</td><td>PPI 0 Port A Line 5</td></tr>
<tr><td>6</td><td>NONE</td><td>PPI 0 Port A Line 6</td></tr>
<tr><td>7</td><td>NONE</td><td>PPI 0 Port A Line 7</td></tr>
<tr><td>8</td><td>NONE</td><td>Counter 0 Output</td></tr>
<tr><td>9</td><td>NONE</td><td>Counter 1 Output</td></tr>
</table>
</td></tr>
<tr><td>Mode</td><td>long</td><td>Disable or Enable a source
0 : Disable
1 : Enable</td></tr>
<tr><td>Type</td><td>long</td><td>Set the type of trigger for the interrupt
<table>
<tr><td>No</td><td>Description</td></tr>
<tr><td>0</td><td>Rising Edge</td></tr>
<tr><td>1</td><td>Falling Edge</td></tr>
</table>
</td></tr>
<tr><td>RETURN</td><td>Long</td><td>This parameter contains the error code return. If =0 then no error occurred.</td></tr>
</table>

Table 4-7 EDREIntX.Configure Parameters

Enabling Interrupts

A single call is necessary to enable the interrupt sub-system. This will also enable the global interrupt on the PCI800 and connect it to the PCI Bus.
ACTIVEX-CALL
Long EDREIntX.Enable
A returned error code will contain the status of the call.

Disabling Interrupts

A single call is necessary to disable the interrupt sub-system.
ACTIVEX-CALL
Long EDREIntX.Disable
A returned error code will contain the status of the call.

Interrupt Event

If interrupts are enabled an event will occur on each interrupt. The interrupt control's interrupt event will be triggered. The source of the interrupt will also be passed to the event handler.

ACTIVEX-CALL

Interrupt(long Source)

The source is the value read from the interrupt status register of the PCI800 device. The sources are binary weighted. See table below.

Source Value	Actual source
1	0
2	1
4	2
8	3
16	4
32	5
64	6
128	7
256	8
512	9

Table 4-8 Event Source

Configure Ports

Port configuration on the PCI800 series boards is done automatically when the read or write function is called. Port configuration can be done manually as well. The EDRE_Query function can be used to configure a port. Manual configuration will cause the port to be set to a fixed state, either input or output. Automatic port configuration will be disabled for the ports that have been manually configured to prevent any accidental reconfiguration of the ports. Port status can be set back to auto configuration by using the EDRE_Query function call again.
Only ***port-C*** (see Table 4-1) can be configured as ***INANDOUT*** port. If port is configured as ***INANDOUT*** the ***upper*** 8 bits of port-C is configured as ***INPUT*** and ***lower*** 8 bits as ***OUTPUT***.

Configuring a Port

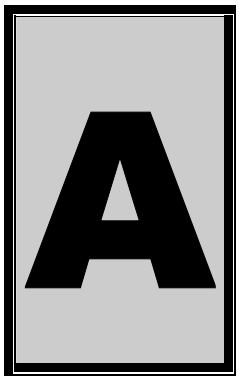
A single query call is necessary to configure a port status.
Code = 407
The query parameter is a 16 bits value. It consists of the port in the upper 8 bits and port status in the lower 8 bits.

API-CALL
Long EDRE_Query(ulng Sn, ulng Code , ulng Param)
The serial number, Query code and Parameter are needed to configure port. A return code will indicate if any errors occurred.

ACTIVEX CALL
Long EDRECTX.Query(ulng Code, ulng Param)
The Query code and Parameter is needed to configure port. A return code will indicate if any errors occurred.

Upper 8 bits	Lower 8 bits	
Port number	Value	Status
	0	OUT
	1	IN
	2	INANDOUT (Only port C)
	3	AUTO

Table 4-9 Parameter Setup



A.Specifications

Digital Input/Output Characteristics

Number of Digital Channels:

Device	DIO Channels	Opto Channels	High Current Channels
PCI 836A	24	0	0
PCI 836C	24	1	16
PCI 848A	48	0	0
PCI 848C	48	1	0
PCI 896A	96	0	0
PCI 896C	96	1	0
PCI 8192A	192	0	0
PCI 8192C	192	1	0

Number of Grouped Channels:

Device	PPI Channels	Opto Channels	High Current Ports
PCI 836A	3	0	0
PCI 836C	3	1	1
PCI 848A	6	0	0
PCI 848C	6	1	0
PCI 896A	12	0	0
PCI 896C	12	1	0
PCI 8192A	24	0	0
PCI 8192C	24	1	0

Compatibility: TTL

D.C Characteristics – PPI 8255 Compatible Ports

Level	Min	Max
Input Low Voltage	-0.5V	0.8V
Input High Voltage	2.0V	5.0V
Output High Voltage	2.4V	
Output Low Voltage		0.45V
Output Current		2mA

D.C Characteristics – High Current Ports (PCI 836C)

Level	Min	Max
Output High Voltage		5V
Output Low Voltage	0V	
Output Current		20mA

Opto-Isolator (C-Versions)

Input Characteristics

Characteristic	Description
Number of lines	1
Compatibility	TTL/ANALOG
Input High Voltage – LOGIC 1	3.1V to 28V
Input Low Voltage – LOGIC 0	0V to 3V
On Current	10 mA
Max forward current	50 mA

Counter-Timer Characteristics (C-Versions)

Number of Channels: 3 independent counters

Resolution: 16-bits

Compatibility 82C54 / TTL

Clock Source

Jumper selectable
1. Scaled internal up to 4 MHz
2. External

Gate Source

Jumper selectable
1. Software Controlled
2. External

Interrupt Source Counter 0,1 on Terminal Count (TC).

I/O Characteristics

Level	Min	Max
Input Low Voltage	0V	0.8V
Input High Voltage	2.0V	5.25V
Low Level Input Current		- 100 uA
High Level Input Current		100 uA
Output High Voltage	2.4V	
Output Low Voltage		0.6V
Low Level Output Current		-24 mA
High Level Output Current		4 mA

Bus Interface

Bus Type IBM PCI Compatible Revision 2.2 Compliant

Controller Slave

Voltage 3.3V or 5V

Power Requirements

Specification	PCI836A/C	PCI848A/C	PCI896A/C	PCI8192A/C
+5V Internal Typical	350 mA	400 mA	450 mA	500 mA
+5V External (DB37)	1.5A Fused	None	None	None
+5V Internal (IDC20 HC PORT)	200 mA	None	None	None
+5V External (IDC50)	None	200 mA	200 mA	200 mA
+5V External (DB25)	None	200 mA	200 mA	200 mA
+12V External (DB25 & DB37)	200 mA	200 mA	200 mA	200 mA
+12V External (DB25 & DB37)	200 mA	200 mA	200 mA	200 mA

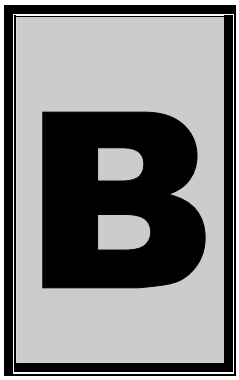
Dimensions

PCI836A/C 122 mm x 82 mm
PCI848A/C 161 mm x 105 mm

PCI896A/C	208 mm x 105 mm
PCI8192A/C	302 mm 105 mm

Connectors

PCI836A	DB37 (M) External
PCI836C	DB37 (M) External & IDC20 (M) Internal
PCI848A	2 x IDC50 (M) Internal
PCI848C	2 x IDC50 (M) Internal & DB25 (M) External
PCI896A	4 x IDC50 (M) Internal
PCI896C	4 x IDC50 (M) Internal & DB25 (M) External
PCI8192A	8 x IDC50 (M) Internal
PCI8192C	8 x IDC50 (M) Internal & DB25 (M) External



B.Configuration Constants

Query Codes

Name	Value	Description
APIMAJOR	1	Query EDRE API major version number.
APIMINOR	2	Query EDRE API minor version number.
APIBUILD	3	Query EDRE API build version number.
APIOS	4	Query EDRE API OS type.
APINUMDEV	5	Query number of devices installed.
BRDTYPE	10	Query a board's type.
BRDREV	11	Query a board's revision.
BRDYEAR	12	Query a board's manufactured year.
BRDMONTH	13	Query a board's manufactured month.
BRDDAY	14	Query a board's manufactured day.
BRDSERIALNO	15	Query a board's serial number.
DRVMAJOR	20	Query a driver's major version number.
DRVMINOR	21	Query a driver's minor version number.
DRVBUILD	22	Query a driver's build version number.
ADNUMCHAN	100	Query number of ADC channel.
ADNUMSH	101	Query number of samples-and-hold channels.
ADMAXFREQ	102	Query maximum sampling frequency.
ADBUSY	103	Check if ADC system is busy.
ADFIFOSIZE	104	Get ADC hardware FIFO size.
ADFIFOOVER	105	Check for FIFO overrun condition.
ADBUFFSIZE	106	Check software buffer size.
ADBUFFOVER	107	Check for circular buffer overrun.
ADBUFFALLOC	108	Check if software buffer is allocated.
ADUNREAD	109	Get number of samples available.
ADEXTCLK	110	Get status of external clock line – PCI30FG.
ADEXTTRIG	111	Get status of external trigger line – PCI30FG.
ADBURST	112	Check if burst mode is enabled.
ADRANGE	113	Get ADC range.
DANUMCHAN	200	Query number of DAC channels.
DAMAXFREQ	201	Query maximum DAC output frequency.
DABUSY	202	Check if DAC system is busy.
DAFIFOSZ	203	Get DAC FIFO size.
CTNUM	300	Query number of counter-timer channels.
CTBUSY	301	Check if counter-timer system is busy.
DIONUMPORT	400	Query number of digital I/O ports.
DIOQRYPORT	401	Query a specific port for capabilities.
DIOPORTWIDTH	402	Get a specific port's width.
DIOCFG	407	Configure port as IN, OUT, or INANDOUT port
INTNUMSRC	500	Query number of interrupts sources.
INTSTATUS	501	Queries interrupt system's status.
INTBUSCONNECT	502	Connect interrupt system to bus.
INTISAVAILABLE	503	Check if an interrupt is available.
INTNUMTRIG	504	Check number times interrupted

Error Codes

Name	Value	Description
EDRE_OK	0	Function successfully.
EDRE_FAIL	-1	Function call failed.
EDRE_BAD_FN	-2	Invalid function call.
EDRE_BAD_SN	-3	Invalid serial number.
EDRE_BAD_DEVICE	-4	Invalid device.
EDRE_BAD_OS	-5	Function not supported by operating system.
EDRE_EVENT_FAILED	-6	Wait on event failed.
EDRE_EVENT_TIMEOUT	-7	Event timed out.
EDRE_INT_SET	-8	Interrupt in use.
EDRE_DA_BAD_RANGE	-9	DAC value out of range.
EDRE_AD_BAD_CHANLIST	-10	Channel list size out of range.
EDRE_BAD_FREQUECY	-11	Frequency out of range.
EDRE_BAD_BUFFER_SIZE	-12	Data passed by buffer incorrectly sized
EDRE_BAD_PORT	-13	Port value out of range.
EDRE_BAD_PARAMETER	-14	Invalid parameter value specified.
EDRE_BUSY	-15	System busy.
EDRE_IO_FAIL	-16	IO call failed.
EDRE_BAD_ADGAIN	-17	ADC-gain out of range.
EDRE_BAD_QUERY	-18	Query value not supported.
EDRE_BAD_CHAN	-19	Channel number out of range.
EDRE_BAD_VALUE	-20	Configuration value specified out of range.
EDRE_BAD_CT	-21	Counter-timer channel out of range.
EDRE_BAD_CHANLIST	-22	Channel list invalid.
EDRE_BAD_CONFIG	-23	Configuration invalid.
EDRE_BAD_MODE	-24	Mode not valid.
EDRE_HW_ERROR	-25	Hardware error occurred.
EDRE_HW_BUSY	-26	Hardware busy.
EDRE_BAD_BUFFER	-27	Buffer invalid.
EDRE_REG_ERROR	-28	Registry error occurred.
EDRE_OUT_RES	-29	Out of resources.
EDRE_IO_PENDING	-30	Waiting on I/O completion

Digital I/O Codes

Name	Value	Description
DIOOUT	0	Port is an output.
DIOIN	1	Port is an input.
DIOINOROUT	2	Port can be configured as in or out.
DIOINANDOUT	3	Port is an input and an output.

C

C.Counter Modes

Mode 0 - Event counter

Output operation

The output is low after configuration. The count value is loaded on the first clock pulse. The output is low until the counter becomes 0.

Gate function

High enables counting, low disables counting. The gate does no effect the output.

Count value load timing

The count value is only loaded on the first falling edge of the clock pulse. The first clock pulse does not decrement the count value. Thus the output will be high after (N+1).

Count value writing during counting

The count value write is a 2-byte process. The counting stops after the first byte is written. The output will go low after this. After the next byte is written the count value will be loaded again and the output will go high after N+1 clocks.

Count value writing when the gate signal is low

The count value is only written the first clock after the gate goes high again.

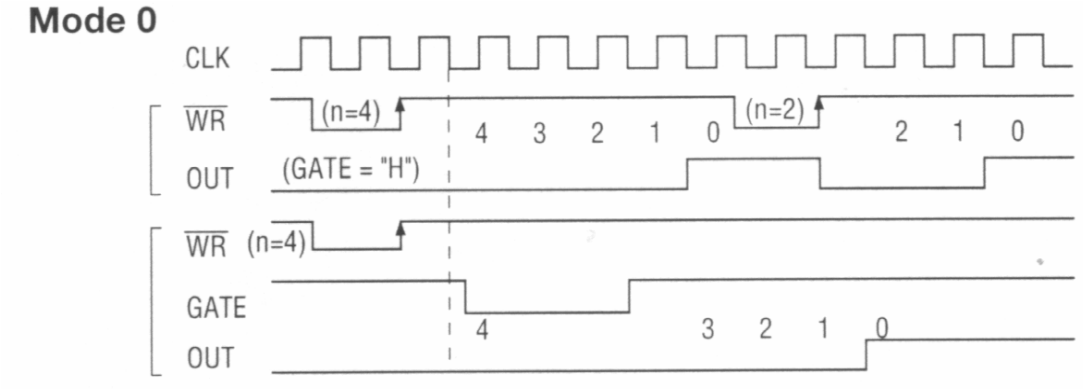


Figure C-1 Counter-Timer Mode 0

Mode 1 – Digital one-shot

Output operation

The output is high after configuration. The output is low until the counter becomes 0. The count value is loaded after a gate trigger. Once it is high it stays high until one clock pulse after a gate trigger.

Gate function

A positive edge reloads the counter. The gate does no effect the output.

Count value load timing

After the configuration and count value is written, the output will go low on a negative clock pulse succeeding a gate trigger. This will last for N clocks.

Count value writing during counting

This does not affect the output until a gate pulse triggers it.

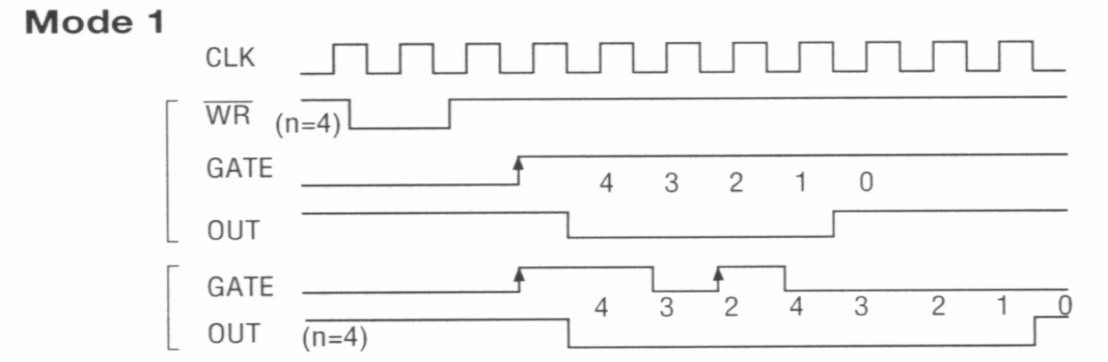


Figure C-2 Counter-Timer Mode 1

Mode 2 – Rate Generator and Real-Time Clock

Output operation

The output is high after configuration. The output is high until the counter becomes 1. The output goes low for one clock and then high again. The count value is reloaded again.

Gate function

High enables counting, low disables counting. If the gate is set low when the output is low, the output is set high immediately. At the following edge succeeding a high gate pulse the count value is reloaded again. This can be used for synchronization.

Count value load timing

After the configuration and count value is written, the output will go high on a negative clock pulse. This will last for N clocks and clock and then go low.

Count value writing during counting

The count value does not affect the current operation. The old value will be loaded if no new value is written. Otherwise the new value will be used on the next trigger or cycle.

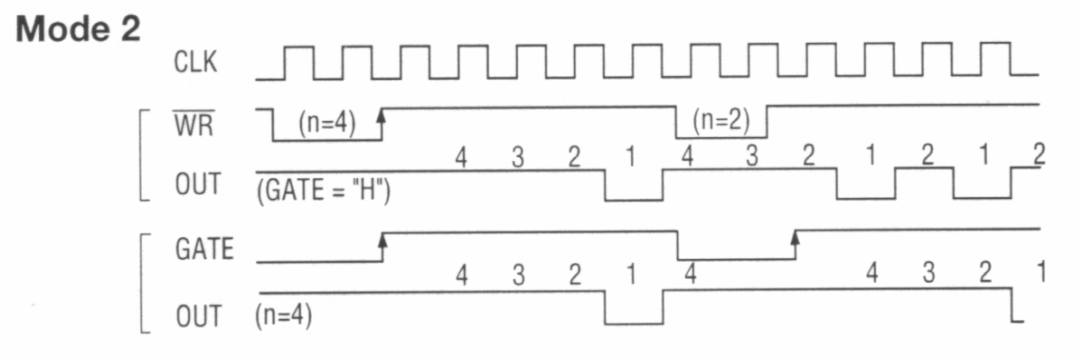


Figure C-3 Counter-Timer Mode 2

Mode 3 – Square Wave Generator

Output operation

The output is high after configuration. The output is high until the counter reaches half of its count value. The output goes low for the remainder of the count value. The process repeats its self again.

Gate function

High enables counting, low disables counting. If the gate is set low when the output is low, the output is set high immediately. At the following edge succeeding a high gate pulse the count value is reloaded again. This can be used for synchronization.

Count value load timing

After the configuration and count value is written, the output will go high on a negative clock pulse.

Count value writing during counting

The count value does not affect the current operation. The old value will be loaded if no new value is written. Otherwise the new value will be used on the next trigger or cycle.

Even number counting

Output is initially high. The count value is loaded and is decremented by 2 by consecutive clock pulses. When the counter reaches 2 the output is set to low. The count value is then reloaded and decremented by 2 per clock. When it reaches 2 the count value is reloaded and the output set to high again. The process then repeats.

Odd number counting

The output is initially high. The initial value minus 1 is loaded. The value is then decremented by 2 consecutive clock pulses. When the counter becomes 0 the output goes low. The initial value minus 1 is then loaded again. The value is then decremented by 2 by consecutive clock pulses. When the counter is 2 the output goes high again. The initial value minus 1 is loaded again. The operation repeats itself again.

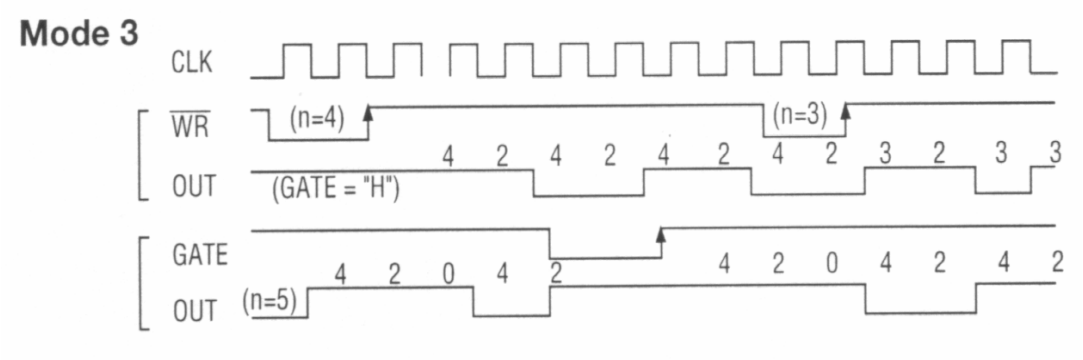


Figure C-4 Counter-Timer Mode 3

Mode 4 – Software Trigger Strobe

Output operation

The output is high after configuration. When the counter becomes 0 the output goes low for 1 clock period and then high again. The count sequence starts after the count value is written.

Gate function

High enables counting, low disables counting. The gate signal does not affect the output.

Count value load timing

After configuration and the initial count value is written the output is high for N=count clocks. The initial count value does not get decremented.

Count value writing during counting

On the next clock pulse the new count value will be loaded and therefore start a new operation. This means that the operation is retriggered by software.

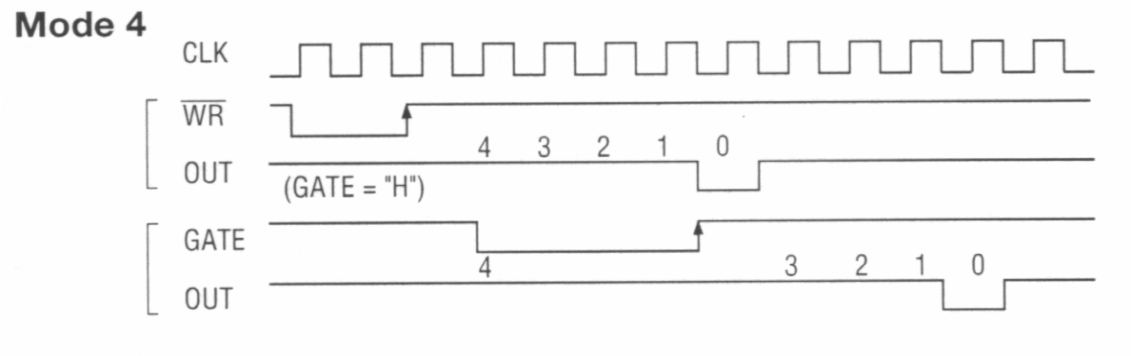


Figure C-5 Counter-Timer Mode 4

Mode 5 – Hardware Trigger Strobe

Output operation

The output is high after configuration. When the counter becomes 0 the output goes low for 1 clock period and then high again. The count sequence is triggered by rising edge on the gate pulse.

Gate function

The count value is loaded on a negative clock pulse succeeding a gate trigger. The gate pulse does not affect the output.

Count value load timing

After the configuration and count value is written, the output will go high on a negative clock pulse succeeding a trigger. This will last for N clocks and then go low for 1 clock pulse.

Count value writing during counting

A new count value does not affect the current operation. Only a trigger can load new value.

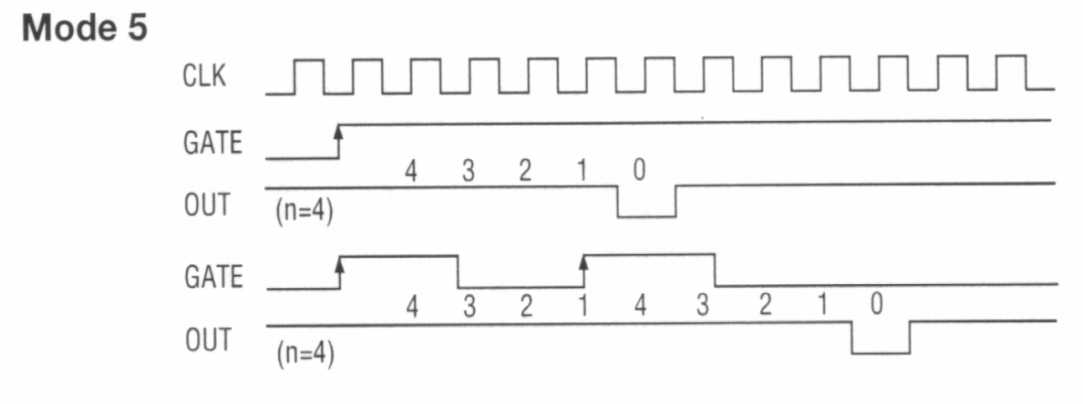
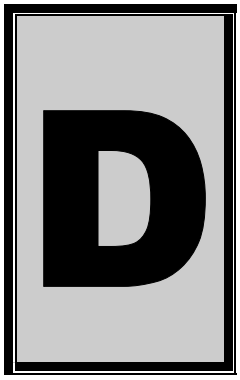
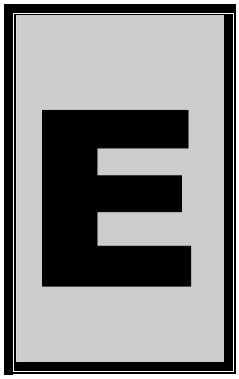


Figure C-6 Counter-Timer Mode 5



D.Layout Diagram



E. Ordering Information

For ordering information please contact Eagle Technology directly or visit our website www.eagledaq.com. They can also be emailed at eagle@eagle.co.za.

Board	Description
PCI 836A	24 channel digital I/O card
PCI 836C	40 channel digital I/O card
PCI 848A	48 channel digital I/O card
PCI 848C	48 channel digital I/O card and 3 counters
PCI 896A	96 channel digital I/O card
PCI 896C	96 channel digital I/O card and 3 counters
PCI 8192A	192 channel digital I/O card
PCI 8192C	192 channel digital I/O card and 3 counters

Table E-1 Ordering Information