Eagle Technologies

PCI-703S 16 Channel Simultaneous Sampling

DAQ Module

Technical Manual

Revision 3.00 April 2002

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1. Changes from previous revision

Applicable to Revision 3.0 of the PCB.

- A second calibration DAC, and associated control signals, was added. This added an additional control signal in the Global Status Register .

- Frequency OUT timer (pre-scaler)has been removed as this doesn't fit in the FPGA

2. Module Features

- Four, Eight or Sixteen fourteen bit resolution simultaneous sampling analogue input channels with independent programmable gain per channel.
- All input channels can be user configured for differential or single ended input.
- Two fourteen bit resolution analogue output channels –DA models only.
- PCI 2.2 compliant at 32 bits, 33 Mhz. 3.3V or 5V PCI slot compatible.
- Supports both master and target PCI functions with an integrated programmable DMA controller.
- Three PCI703S DAQ module option ranges are available. The modules vary only in the number of simultaneous channels supported.
  The ranges, data acquisition features and functions of each are defined in Table 1.

Feature	PCI703S-4	PCI703S-8DA	PCI703S-16DA
Number of Analogue Input Channels. (All channels can be user configured for differential or single ended operation.)	4	8	16
Number of Analogue Output Channels	2	2	2
A/D Resolution (bits) @ 400 Khz max.	14	14	14
A/D Sample FIFO Depth	4096	4096	4096
A/D Channel List FIFO Depth	4096	4096	4096
D/A Resolution (bits) @ 100 Khz	-	14	14
D/A FIFO Depth (programmable)	-	4096	4096
D/A waveform generation capability	-	YES	YES
Triggering Capability.	Internal, External. Analogue & Digital. Post Trigger.	Internal, External. Analogue & Digital. Post Trigger.	Internal, External. Analogue & Digital. Post Trigger.
Counter Timers – 16 bit.	3	3	3
Frequency Output Timer, or Counter Timer pre-scaler – 8 bit.	1	1	1
Number of Digital I/O Lines (TTL)	8	8	8
Number of programmable function I/O's	10	10	10

Table 1 PCI703S-4/8/16 Module Options

3. Hardware Overview

This chapter provides a hardware overview of the PCI-703S DAQ module. Figure 1 depicts a functional block diagram of the module.

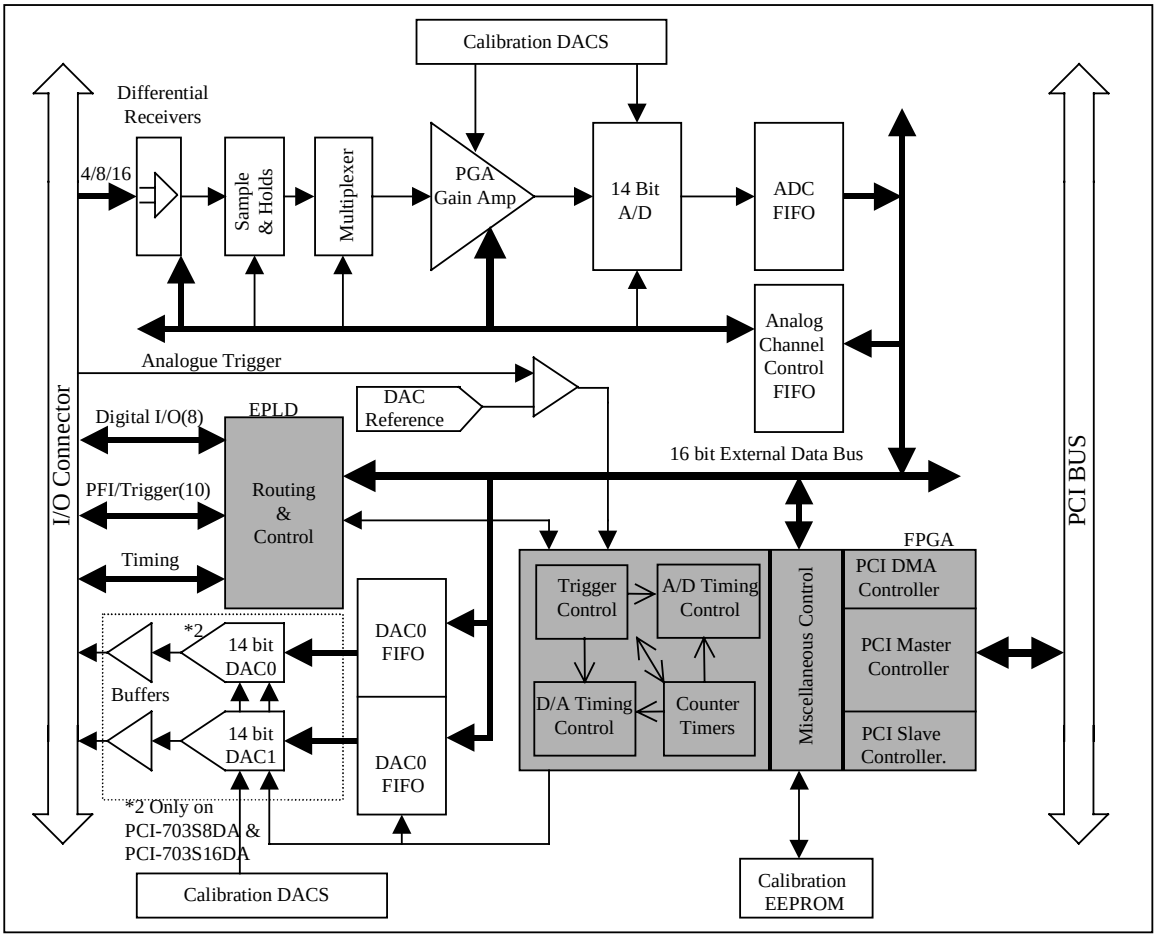

Figure 1 PCI-703Sxx Block Diagram

3.1 Module Address Map

The module uses the Actel Target + DMA PCI core to interface to the PCI bus. This core thus defines much of the software protocol used to access the module.

The PCI-703S module's control registers and FIFO' s are mapped as per Table 2.

Configuration register BAR0 used as the base.		
Offset Address (Hex)	**Register Name**	**Description**
00	A/D_FIFO_DATA	Read/Write. Contains the A/D conversion results. Only bits <13:0> are valid.

04	A/D_CHANNEL_LIST	Read/Write. Write data to A/D Channel List FIFO. Only bits <13:0> are valid.
08	DAC_FIFO(0)	Read/Write. Write data to D/A Channel 0 FIFO. Only bits <13:0> are valid.
0C	DAC_FIFO(1)	Read/Write. Write data to D/A Channel 1 FIFO. Only bits <13:0> are valid.
3C:20	GAIN_CALIBRATION_BUFFER	Read/Write. 8 words x 14 bits. Contains the gain calibration constants for the PGIA D/A. Only bits <13:0> are valid.
Configuration register BAR1 used as the base.		
Offset Address (Hex)	**Register Name**	**Description**
100	DAC_CNTRL(0)	DAC0 Control Register
104	DAC_CNTRL(1)	DAC1 Control Register
200	CNTR_CNTRL(0)	Counter 0 Control Register
208	CNTR_DIVR(0)	Counter 0 Divisor Register
210	CNTR_CNTRL(1)	Counter 1 Control Register
218	CNTR_DIVR(1)	Counter 1 Divisor Register
220	CNTR_CNTRL(2)	Counter 2 Control Register
228	CNTR_DIVR(2)	Counter 2 Divisor Register
230	Reserved	
238	Reserved	
300	A/D_CNTRL	A/D Control Register
400	DIO_CONFIG_REG	Controls the direction of the DIO pins.
410	DIO_DATA_REG	DIO write or read data register
420	PIO_CONFIG_REG	Controls the direction of the PIO pins.
430	PIO_DATA_REG	PIO write or read data register
500	GLOBAL_STATUS_REGISTER	Configuration, Interrupt and Status Flags register

Table 2 PCI-703S Register Address Map

3.2 Global Status Register

This read/write register defines bits used to configure and monitor the status of the module. With the exception of the data FIFO' s it is the only register that can be read by the host firmware – simplifying the FPGA interface.

The bit definitions are defined in Table 3.

Global Status Register bit configuration:		
Bit 0	Global Interrupt Enable	Enables or disables all interrupts from the module. “0” : Interrupts are disabled. No PCI INTA can be asserted. “1” : Interrupts are enabled. Note that the various interrupt sources are individually configured using the specific functions Control Register. However, the status of these individual interrupts can only be accessed via this register.
Bit 1	A/D FIFO_EMPTY_STAT	Reflects the status of the A/D Data FIFO’s Empty Flag. (Read only) “0” : The FIFO is not empty “1” : The FIFO is empty.
Bit 2	Channel_List_Done_STAT	Gets set to ‘1’ whenever the last command in the channel list has been executed. Used by the host to know when the number of A/D samples defined in the Channel List FIFO have been converted. The A/D result buffer can now be read. Cleared when the host write a ‘0’ to this bit.
Bit 3	A/D FIFO_EMPTY_INTR	Set whenever A/D FIFO_EMPTY_STAT changes to the NOT EMPTY state if the corresponding interrupt is enabled in the A/D Control Register. Cleared by writing a zero to this bit.
Bit 4	Channel_List_Done_INTR	Set whenever bit (2) is set and the corresponding interrupt is enabled in the A/D Control Register. Cleared when bit(2) or the Interrupt enable is cleared.
Bit 5	DAC(0) FIFO_EMPTY_STAT	Reflects the status of the DAC(0) Data FIFO’s Empty Flag. (Read only) “0” : The FIFO is not empty “1” : The FIFO is empty.
Bit 6	DAC(0) FIFO_HALF_STAT	Reflects the status of the DAC(0) Data FIFO’s Half Full Flag. (Read only) “0” : The FIFO level is less than half full. “1” : The FIFO level has reached at least half full
Bit 7	DAC(0) FIFO_EMPTY_INTR	Set whenever DAC(0) FIFO_EMPTY_STAT changes to the EMPTY state if the corresponding interrupt is enabled in the A/D Control Register. Cleared by writing a zero to this bit.
Bit 8	DAC(0) FIFO_HALF_INTR	Set whenever DAC(0) FIFO_HALF_STAT changes to the LESS THAN HALF EMPTY state if the corresponding interrupt is enabled in the A/D Control Register.

Global Status Register bit configuration:		
		Cleared by writing a zero to this bit.
Bit 9	DAC(1) FIFO_EMPTY_STAT	Reflects the status of the DAC(1) Data FIFO's Empty Flag. (Read only) "0" : The FIFO is not empty "1" : The FIFO is empty.
Bit 10	DAC(1) FIFO_HALF_STAT	Reflects the status of the DAC(1) Data FIFO's Half Full Flag. (Read only) "0" : The FIFO level is less than half full. "1" : The FIFO level has reached at least half full
Bit 11	DAC(1) FIFO_EMPTY_INTR	Set whenever DAC(1) FIFO_EMPTY_STAT changes to the EMPTY state if the corresponding interrupt is enabled in the A/D Control Register. Cleared by writing a zero to this bit.
Bit 12	DAC(1) FIFO_HALF_INTR	Set whenever DAC(1) FIFO_HALF_STAT changes to the LESS THAN HALF EMPTY state if the corresponding interrupt is enabled in the A/D Control Register. Cleared by writing a zero to this bit.
Bit 13	CNTR(0) EXPIRED	Set whenever Counter Register 0 has reached it's terminal count if the corresponding interrupt is enabled in the Counter Control Register. Cleared by writing a zero to this bit.
Bit 14	CNTR(1) EXPIRED	Set whenever Counter Register 1 has reached it's terminal count if the corresponding interrupt is enabled in the Counter Control Register. Cleared by writing a zero to this bit.
Bit 15	CNTR(2) EXPIRED	Set whenever Counter Register 2 has reached it's terminal count if the corresponding interrupt is enabled in the Counter Control Register. Cleared by writing a zero to this bit.
Bit 16	EEPROM_ClK	Maps directly to the EEPROM' s CLK pin. (Read/Write)
Bit 17	EEPROM_CS	Maps directly to the EEPROM' s CS pin. (Read/Write)
Bit 18	EEPROM_DI	Maps directly to the EEPROM' s DI pin. (Read/Write)
Bit 19	EEPROM_DO	Maps directly to the EEPROM' s DO pin. (Read/Write)
Bit 20	CAL_DAC_CLK	Maps directly to the Calibration DAC' s CLK pin. (Read/Write)
Bit 21	CAL_DAC_LD1	Maps directly to the Calibration DAC#1 LD pin. (Read/Write)
Bit 22	CAL_DAC_LD2	Maps directly to the Calibration DAC#2 LD pin. (Read/Write)

Global Status Register bit configuration:		
Bit 23	CAL_DAC_SDI	Maps directly to the Calibration DAC' s SDI pin. (Read/Write)

Table 3 Global Status Register Bit Definitions

3.3 DIO I/O Signals

The module supports eight programmable digital input/ output signals mapped to the I/O connector DIO(7:0) pins. These pins are configured as per Table 4 and Table 5.

DIO_CONFIG_REG:		
Bits (7:0)		Defines the bits as inputs or outputs. (Write Only) Bit Definition: "0" : The corresponding bit is an input. This is the reset state. "1" : The corresponding bit is an output.

Table 4 DIO Configuration Register bit definitions

DIO_DATA_REG:		
Bits (7:0)		WRITE: Provides output data for all bits configured as OUTPUTS READ: Provides the I/O state of all pins.

Table 5 DIO Data Register bit definitions

3.4 PIO I/O Signals

The module supports ten programmable digital multifunction input/output signals mapped to the I/O connector PIO(9:0) pins. From a software viewpoint these signals behave like normal I/O signals. Their multifunction nature occurs when other functions are configured. For example if PFI(2)/CONVERT is used in the A/D setupt then PFI(2) must be configured as an input. These pins are configured as per Table 6 and Table 7.

PIO_CONFIG_REG:		
Bits (9:0)		Defines the bits as inputs or outputs. (Write Only) Bit Definition: "0" : The corresponding bit is an input. This is the reset state. "1" : The corresponding bit is an output.

Table 6 PIO Configuration Register bit definitions

PIO_DATA_REG:		
Bits (9:0)		WRITE: Provides output data for all bits configured as OUTPUTS READ: Provides the I/O state of all pins.

Table 7 PIO Data Register bit definitions

3.5 Analogue Input

A block diagram of the analogue input configuration is presented in Figure 2.

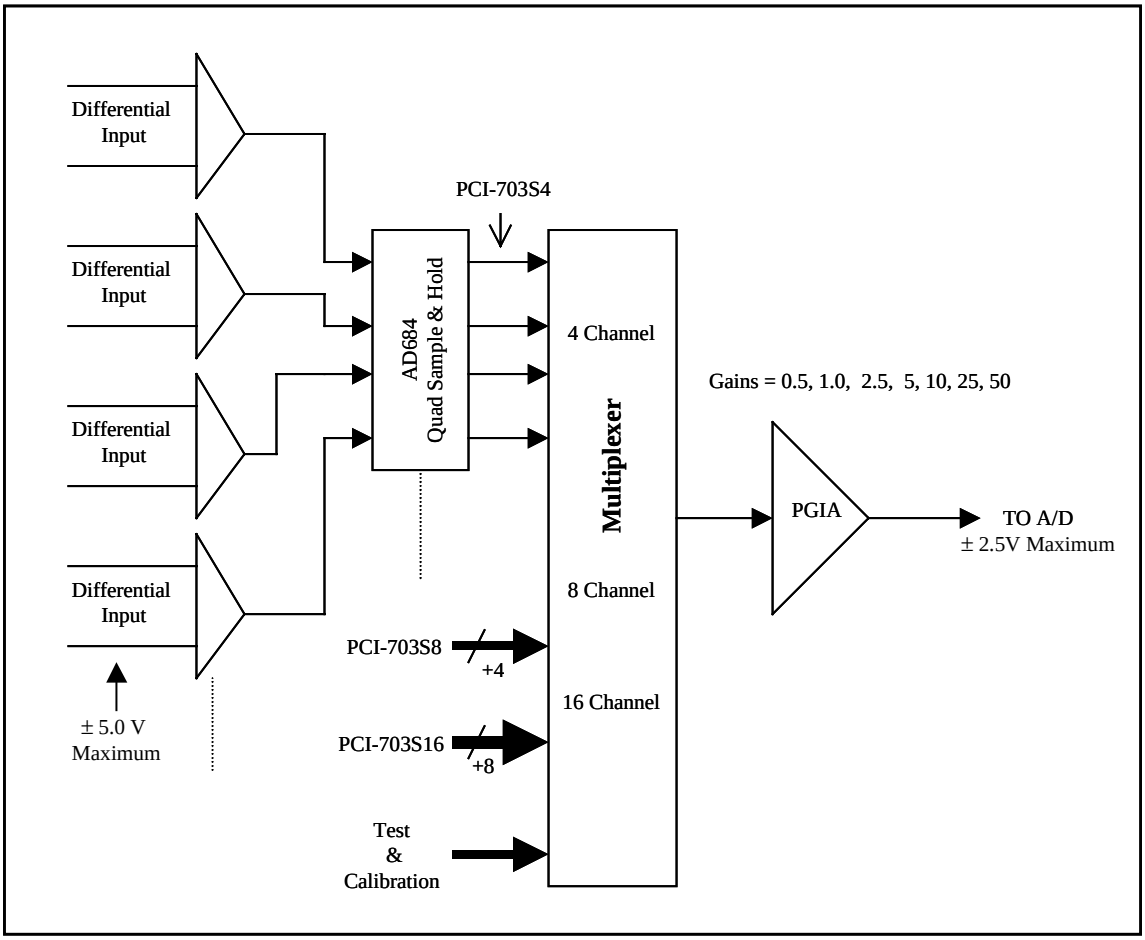

Figure 2 PCI-703S Analogue Input Configuration

All analogue inputs are always received as differential signals via the I/O connector. Single ended inputs should terminate the unused (–) input to analogue ground (AGND) at the I/O connector. The AD684 sample and hold component is limited to ± 5.0 volts thus restricting the maximum input analogue voltage range to ± 5.0 volts. The A/D itself is limited to a maximum input voltage of ± 2.5 volts. The PGIA must thus be used to appropriately scale the input voltage.

All channels are sampled simultaneously before being fed to the channel multiplexer and programmable gain amplifier. However, it is important to note that the switched multiplexer and PGIA introduces a settling time delay of at least 2.5 us before the selected channel is valid at the input to the A/D. Thus, from clocking the sample and hold circuitry a 2.5 us delay is required before the A/D data conversions can begin. The maximum sample and hold clock frequency is thus 400Khz/(N+1) where N is the number of A/D channels to be converted between each sampling clock. The channel list FIFO is used to define the channel sampling sequence.

3.5.1 Channel List FIFO

The PCI-703S module is a simultaneous sampling module with all analogue inputs sampled simultaneously with the selected sampling clock source (external or internal). 2.5us after this sampling clock all channels are available for multiplexing and conversion through the A/D at maximum rate 400 Khz (2.5us) per channel and stored in the A/D result FIFO.

Although the module supports upto 16 channels it may not always be desirable to include all 16 analogue input channels in the conversion list if say only the results of five channels are required. Reducing the number of channels in the sample list also increases the maximum sampling clock rate as the maximum input sampling rate is 400Khz (the maximum A/D conversion rate) divided by (N+1) where N is the number of channels to be converted per sampled input clock.

To support the variable number of channels feature, the channel list is defined using X number of sub-frames, each identified with a start of sub-frame marker, and each defining the channel number and associated channel gain of each of the channels to be converted as part of the current sub-frame. Note that only one sub-frame is executed per input sampling clock. Each sub-frame would also typically never consist of more channel definitions than that supported by the module.

The complete channel list would typically consist of a string of identical sub-frames (although it is not a requirement that these be identical). The number of sub-frames multiplied by the number of channel definitions in each sub-frame essentially defines the number of A/D samples stored in the A/D FIFO before and an A/D conversion complete interrupt is generated. As the A/D result FIFO depth is 4096 this number would typically not be more than 2048 although it depends on the system latency to unpack the FIFO and the A/D conversion rate.

The Channel List FIFO is implemented as programmable circular buffer with a depth equal to the number of entries. The A/D state controller in the FPGA repeatedly loops through this buffer converting the selected channel as per the setup configuration. This list must be configured and setup by the host software before the A/D scanning is enabled. The FIFO must be cleared before formatting the command structure as the number of written entries determines where the command chain wrap occurs.

Table 8 provides an example of the structure of the channel list with 512 entries defining 128 identical sub-frames that convert analogue input channels 1 to 5 on each sample clock.

Channel List Configuration			**Description**
Start Of Sub Frame #1	**Channel Gain**	**Channel Number**	
1	**1**	**1**	SOSF indicates wait for input sample clock + 2.5us before proceeding. Then Convert channel 1, Gain = 1. Then..
0	**2.5**	**2**	Convert channel 2, Gain = 2.5. Then..
0	**5**	**3**	Convert channel 3, Gain = 5.0 Then..
0	**5**	**4**	Convert channel 4, Gain = 5.0 Then..
0	**10**	**5**	Convert channel 5, Gain = 10 Then..
Start Of Sub Frame #2	**Channel Gain**	**Channel Number**	Next sub frame is a repeat of the last
1	**1**	**1**	SOSF indicates wait for input sample clock + 2.5us before proceeding. Then Convert channel 1, Gain = 1. Then..
0	**2.5**	**2**	Convert channel 2, Gain = 2.5. Then..
0	**5**	**3**	Convert channel 3, Gain = 5.0 Then..
0	**5**	**4**	Convert channel 4, Gain = 5.0 Then..
0	**10**	**5**	Convert channel 5, Gain = 10 Then..
Start Of Sub Frame #128	**Channel Gain**	**Channel Number**	Sub-frames 3 to 128 are the same as the last
1	**1**	**1**	SOSF indicates wait for input sample clock + 2.5us before proceeding. Then Convert channel 1, Gain = 1. Then..

0	**2.5**	**2**	Convert channel 2, Gain = 2.5. Then..
0	**5**	**3**	Convert channel 3, Gain = 5.0 Then..
0	**5**	**4**	Convert channel 4, Gain = 5.0 Then..
0	**10**	**5**	Convert channel 5, Gain = 10 Then..
No more entries in the channel list FIFO. Generate a Channel List Empty Interrupt and loop back to Sub Frame #1.			

Table 8 Channel List FIFO Structure Example

Table 9 provides the bit definitions of each entry in the channel list FIFO

Channel List FIFO Configuration		
Bits (5:0)	Selects the analogue channel for conversion as follows:	<u>Analogue Inputs</u> "000000" Analogue input channel 0 "000001" Analogue input channel 1 "000010" Analogue input channel 2 "000011" Analogue input channel 3 "000100" Analogue input channel 4 "000101" Analogue input channel 5 "000110" Analogue input channel 6 "000111" Analogue input channel 7 "001000" Analogue input channel 8 "001001" Analogue input channel 9 "001010" Analogue input channel 10 "001011" Analogue input channel 11 "001100" Analogue input channel 12 "001101" Analogue input channel 13 "001110" Analogue input channel 14 "001111" Analogue input channel 15 <u>Test Inputs</u> "1-0000" DAC0 Output (feedback signal for test) "1-0001" DAC1 Output (feedback signal for test) "1-0010" Calibration DAC Channel 1 Output "1-0011" Analogue ground
Bit 6	Start Of Sub Frame	This bit defines the beginning of a new sub-frame within the channel list. Any command with this bit set will **NOT** be scheduled for execution until the next A/D clock tick occurs. It is used by the FPGA controller to determine how many SSH channels are to be converted between each sample and hold clock tick.
Bit 10:9:8:7	RESERVED	
Bits(13:11)	Channel Gain	Select the required channel gain as follows:

Channel List FIFO Configuration		
		“000” : 0.5 “001” : 1 “010” : 2.5 “011” : 5 “100” : 10 “101” : 25 “110” : 50 “111” : 100

Table 9 Channel List FIFO Bit Definitions

3.6 A/D Channel

The A/D conversion process essentially consists of the following events:

1. The host initiates the state controller from it's idle to active mode by moving the A/D from it's disabled to it's enabled mode. After this the state controller will run autonomously until stopped.

2. Index the Channel List FIFO to select the first entry of the new command sub-frame. This is required as one of the analogue channels can be used as the trigger threshold and it needs to be selected. It is the post sampled data that is input to the trigger condition so the trigger will always be synchronous to the sample clock.

3. Wait for trigger event to be met.

4. Wait for the next simultaneous sample and hold clock tick.

5. Wait 2.5 us for the input data to settle

6. Convert the first sample, followed by each further command in the channel list until the next SOSF bit is detected – usually in the first command word of the next sub-frame.

7. Loop to 4.

The key requirements to configure in this process are the trigger event, the Channel List and the source input used to generate the simultaneous sample clock.

The trigger event can be generated from any one of the following sources:

1. Always triggered. (Does thus not require a sampling clock)

2. External input "PFI(0)/TRIG1". (Does thus not require a sampling clock)

3. A selected input analogue channel being greater or less than the trigger reference voltage set on DAC Channel 1. This mode includes triggering on LEVEL or EDGE conditions. **Note that for this trigger mode the first entry in the first sub-command of the Channel List FIFO must always be the entry that specifies the channel that is selected as the trigger source.** As this channel is selected after the sample and hold inputs the analogue comparison is only done 2.5 us after an input sample clock.

The sample clock can be generated from any of the following sources:

1. *Processor using a Programmed I/O bit*: In this mode the processor initiates each conversion by setting a bit in the A/D Control Register. The FIFO EMPTY flag can be used to poll the status of the result. This mode is primarily used for calibration.

2. *Using Counter 2*: In this mode counter two is used to generate the sample clock source. One conversion is performed at each terminal count point. The FIFO HALF FULL flag can be polled to determine when one scan buffer is full. The DMA controller can be programmed to read the FIFO and copy the results to system memory.

3. *Using external I/O pin PFI(2)/CONVERT*: In this mode each rising edge of the external CONVERT signal is used to trigger a conversion. If CONVERT is driven by a clock signal then the mode of operation is the same as that defined in (2).

A typical host interface flow could be defined as follows:

1. Reset the A/D FIFO' s as follows: Set bit 0 of the A/D control register to '1'. Reset bit 0 of the A/D control register to a '0' (the enable to disable condition triggers the FIFO reset). Wait for at least 10us for the FIFO' s to clear.

2. Write “N” sub-frames to the Channel List FIFO. Assuming each sub-frame contains eight analogue channels to be converted per tick.

3. Set the input sample clock to use counter 2 as the source.

4. Setup counter 2 to generate a sample clock frequency less than 400/(8+1) kHz. As we are converting 8 channels per clock. Note that this is the highest frequency allowed for eight channels. The actual frequency can be lower than this.

5. Set the trigger option to “Always Triggered”.

6. Enable the A/D

7. Poll (can be set to interrupt) Channel List Done STAT flag until set.

8. Programme the DMA to empty “Nx8” conversion results. Wait for the DMA to complete.

9. Loop to 7 OR stop the sampling by disabling the A/D.

3.6.1 Programming Information

The A/D channel is programmed using the registers as per Table 10.

The status of the FIFO control signals can be read via the GLOBAL_STATUS_REG.

REGISTER NAME	DESCRIPTION
A/D_CNTRL	**ADC CONTROL REGISTER**
BIT Definitions	
< 0 >	*A/D Operation Mode* : Write Only. < 0 > : Disables the A/D . This is the reset state. < 1 > : Enables Channel List Scan Mode Note: Moving this bit from a ‘1’ to a ‘0’ automatically resets the Data and Channel List FIFO’ s. The FIFO reset takes at least 10 us, so no FIFO commands should be issued before this period after a reset condition.
< 2:1 >	*A/D Scan Clock Source* : Sets the source for the scan clock. Each clock results in a data conversion cycle with a subsequent Channel List Pointer update. Note that the source is gated with the trigger event. < 0:0 > : A/D_CNTRL(10) is the source. < 0:1 > : Counter Timer 3 is the source. < 1:0 > : I/O pin PFI(2)/CONVERT is the source. < 1:1 > : Reserved

REGISTER NAME	DESCRIPTION
< 4:3 >	*A/D Trigger Source* : Sets the source for triggering the scanning. A trigger event is required before the selected scan source clock initiates conversion cycles. Once triggered the process loops until stopped. < 0:0 > : The trigger is always enabled. This is the reset state. < 0:1 > : The Analogue Compare Reference trigger is used. < 1:0 > : I/O pin TRIG1 is used. < 1:1 > : Reserved
< 7:5 >	*Analogue Trigger Mode* : Selects the mode in which the analogue trigger operates: Applicable only when AD_CNTRL < 4:3 > = < 0:1 > Write Only. < 000 > : LEVEL. Selected Ach(x) is > DAC(1) Reference. < 001 > : LEVEL. Selected Ach(x) is < DAC(1) Reference. < 010 > : EDGE. Selected Ach(x) rises above DAC(1) Reference. < 011 > : EDGE. Selected Ach(x) falls below DAC(1) Reference.
< 9:8 >	*A/D Channel FIFO Depth* : Write Only. FIFO Depth is always 4096.
< 10 >	*Initiate Sample* : Writing a '1' to this bit will initiate a single A/D conversion cycle if the trigger condition is satisfied. This is a "soft" bit and does not need to be cleared. Write Only.
< 11 >	*Enable FIFO_EMPTY Interrupts* : Write Only < 0 > : This interrupt is disabled. This is the reset value < 1 > : This interrupt is enabled.
< 12 >	*Enable End of Channel List Command Interrupts* : Write Only < 0 > : This interrupt is disabled. This is the reset value < 1 > : This interrupt is enabled.
A/D_FIFO	**ADC FIFO DATA REGISTER**
BIT Definitions	

REGISTER NAME	DESCRIPTION
< 13:0 >	Read Only: Reading this register (FIFO) passes the fourteen bits of A/D data from the results FIFO to the host. For BI-POLAR conversions the ideal A/D results are coded as follows: **CODE A/D Input Voltage** 01111111111111 = 2.5V – 1 LSB 00000000000000 = 0 10000000000000 = - (2.5V – 1 LSB). For UNI-POLAR conversions the ideal A/D results are coded as follows: **CODE A/D Input Voltage** 01111111111111 = 5V – 1 LSB 00000000000000 = 2,5V 10000000000000 = 0 + 1 LSB

Table 10 A/D Programming Register Definitions

3.7 D/A Channels

Each D/A channel has the following operational modes.

3.7.1 Disabled

The D/A channel is disabled.

The I/O controller, FIFO and FIFO status flags reset.

3.7.2 Programmed I/O Mode.

Under programmed I/O mode the host processor updates the D/A value by simply writing to the appropriate D/A Data Channel FIFO. Although the data is written to the FIFO it is moved to the D/A channel immediately without waiting for any timer ticks.

In this mode the associated timer can be used as a general purpose interrupt timer.

3.7.3 FIFO Non Loop Mode.

The FIFO and associated timer combine to update the D/A channel synchronously with the assertion of the Q output from the timer. If the FIFO is empty the scheduled D/A update cycle is ignored.

A programmable interrupt can be generated on either (or both) of the FIFO status signals: FIFO_EMPTY or FIFO_HALF_FULL..

The suggested host interface flow for this mode of operation is:

1. Reset the D/A FIFO' s as follows: Set bit 0 of the DAC control register to '1'. Reset bit 0 of the A/D control register to a '0' (the enable to disable condition triggers the FIFO reset). Wait for at least 10us for the FIFO' s to clear.

2. Disable the associated counter timer.

3. Load the D/A channel FIFO with at least 2048 + N words, where N *(Timer period) equals the latency of the host to respond to the half empty interrupt and reload more data. The DMA controller can be used.

4. Enable the D/A channel.

5. Enable a D/A channel interrupt on FIFO_HALF_FULL.

6. Setup and enable the associated counter timer.

7. On receipt of the D/A FIFO_HALF_FULL interrupt use the DMA controller to re-load new data to the FIFO.

Having a 4096 deep FIFO with an half full interrupt does not present a problem where the user's data set is smaller. Assuming the user wishes to initially pre-load 32 D/A samples and be interrupted after each 16 samples have been processed with a subsequent refill of 16 new samples. The flow would be as follows:

1. Reset the DAC FIFO' s as follows: Set bit 0 of the DAC control register to '1'. Reset bit 0 of the A/D control register to a '0' (the enable to disable condition triggers the FIFO reset). Wait for at least 10us for the FIFO' s to clear.

2. Disable the associated counter timer.

3. Load the D/A channel FIFO with 2048 "power-up" or default output conditions.

4. Load the D/A channel FIFO with the initial 32 D/A words.

5. Enable the D/A channel and the D/A channel interrupt on FIFO_HALF_FULL.

6. Setup and enable the associated counter timer.

7. On receipt of the D/A FIFO_HALF_FULL interrupt use the DMA controller to re-load 16 new D/A words to the FIFO.

8. Loop to 7.

3.7.4 FIFO Pattern Mode.

The FIFO and associated timer combine to update the D/A channel synchronously with the assertion of the Q output from the timer. If the FIFO is empty the FIFO pointer is reset and the data loop repeated.

Although a programmable interrupt can be generated on either (or both) of the FIFO status signals: FIFO_ EMPTY or FIFO_HALF_FULL. These are meaningless in this operational mode.

The suggested host interface flow for this mode of operation is:

1. Reset the DAC FIFO' s as follows: Set bit 0 of the DAC control register to '1'. Reset bit 0 of the A/D control register to a '0' (the enable to disable condition triggers the FIFO reset). Wait for at least 10us for the FIFO' s to clear.

2. Disable the associated counter timer.

3. Load the D/A channel FIFO with as many words as required by the pattern loop. The only restriction on the word count is that the maximum FIFO depth not be exceeded. The DMA controller can be used.

4. Enable the D/A channel.
5. Setup and enable the associated counter timer.
6. Stop the loop by disabling the D/A Channel or Timer.

3.7.5 Programming Information

Each D/A channel is programmed using the registers as per Table 11 .

The status of the FIFO control signals can be read via the GLOBAL_STATUS_REG.

REGISTER NAME	DESCRIPTION
DAC_CNTRL(X)	**DAC CONTROL REGISTER**
BIT Definitions	
< 1:0 >	*D/A Operation Mode* : Write Only. < 0:0 > : Disables the D/A . This is the reset state. < 0:1 > : Enables Programmed I/O mode. < 1:0 > : Enables FIFO Non Loop Mode < 1:1 > : Enables FIFO Pattern Mode Note: Moving the DAC from an enable to a disable state automatically resets the FIFO' s. This reset takes at least 10us after which the FIFO' s can be written.
< 3:2 >	*D/A Channel FIFO Depth* : Write Only. FIFO Depth is 4096 D/A words.
< 4 >	*Enable FIFO_EMPTY Interrupts* : Write Only < 0 > : This interrupt is disabled. This is the reset value < 1 > : This interrupt is enabled.
< 5 >	*Enable FIFO_HALF_FULL Interrupts* : Write Only < 0 > : This interrupt is disabled. This is the reset value < 1 > : This interrupt is enabled.
DAC_FIFO(X)	**DAC FIFO DATA REGISTER**
BIT Definitions	

REGISTER NAME	DESCRIPTION
< 13:0 >	Write Only: Writing to this register writes the fourteen bits of DAC data into the DAC Channel FIFO. The DAC is configured as a bipolar 14 bit ± 10V unit. The output bit definition is thus: **DAC CODE OUTPUT (V)** 11111111111111 = 10*(8191 / 8192) 10000000000001 = 10*(1 / 8192) 10000000000000 = 0 01111111111111 = -10*(1 / 8192) 00000000000000 = -10*(8191 / 8192)

Table 11 DAC Programming Register Definitions

3.8 Counter Timers

The PCI-703S module contains three identical twenty-four bit programmable down counters. These three resources are generally allocated (this is programmable) as follows:

CNTR_0: Always mapped to the I/O signal GPCTR0_OUT. Can also be selected to control D/A Channel 0 timing.

CNTR_1: Always mapped to the I/O signal GPCTR10_OUT. Can also be selected to control D/A Channel 1 timing.

CNTR_2: Simultaneous sampling clock.

Timers 0 and 1 can use one of three source clocks namely: Internal FPGA sources of 20 Mhz or 100 KHz or an externally generated TTL source – not exceeding 100 KHz. NOTE: The counters are always actually clocked at 20 Mhz with the rising edge of the selected clock source synchronised to the 20 MHz and used as a clock enable signal. Timer 3 can only use the internal FPGA sources of 20 Mhz or 100 KHz.

Each timer has a single Q output that has two programmable modes of operation. These are: 50% duty cycle mode or a single high level pulse equal in pulse width to the period of the selected clock source. The Q output changes state whenever the counter is about to wrap from a count of one back to it's pre-load count.

In single pulse mode the counter divides (Q) the input clock frequency by it's divider setting. In 50% mode the output pulse mode frequency is halved.

Any timer's Q output can also be configured to generate a PCI interrupt.

3.8.1 Programming Information

Each counter is programmed using the registers as per Table 12.

REGISTER NAME	DESCRIPTION
CNTR_CNTRL(X)	**COUNTER CONTROL REGISTER**
BIT Definitions	
< 0 >	Global counter enable bit. When set the counter is enabled to count down. Set to zero on reset . Write Only.
< 2:1 >	*Counter Source Clock Select* : Write Only. < 0:0 > : The source clock is 20Mhz. This is the reset value < 0:1 > : The source clock is 100 KHz < 1:X > : The source clock is the external clock. For Counters 0 & 1 only
< 3 >	*Q Output Mode* : Write Only < 0 > : The Q output is single pulse only. This is the reset value < 1 > : The Q output toggles at each terminal count.
<4 >	*Interrupt Mode* : Write Only < 0 > : Terminal counts do not set the Cntr(x)_INTR flag. This is the reset value < 1 > : Terminal counts set the Cntr(x)_INTR flag.
CNTR_DIVR(X)	**COUNTER DIVISOR REGISTER**
BIT Definitions	
< 15:0 >	Counter Divider: Write Only. This register contains the value that is automatically re-loaded into the down counter whenever the count is about to wrap below one. Whenever this register is written the actual counter is automatically also loaded with this value and the Q output set to zero. The counter will re-load continuously unless it is disabled. Assuming the counter is loaded with 10, the count sequence is: 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 10, 9……

Table 12 Counter Programming Registers

For predictable Q output behaviour the correct programming sequence should be: Disable the counter (the counter will stop, Q will freeze in it's current state. Programme a new divisor (Q will be reset to 0). Enable the counter.

3.9 FREQ OUT TIMER (PRESCALER)

No longer supported.

3.10 EEPROM and Calibration DAC's

Two eight channel eight bit serial DAC' s are used to calibrate out various offset errors as well as set the two output DAC' s –10V reference level. The calibration DAC can generate a bi-polar output of ± 2.5V. As this DAC is used to calibrate errors for fourteen bit A/D's and DAC's the output is generally resistively scaled down by a factor of 47 with each bit thus representing an offset adjustment of 415 uV.

The offset constants are derived during the modules calibration process and are stored in a calibration EEPROM. During module initialisation these constants need to be copied from the EEPROM to the calibration DACS. This same EEPROM also contains the 14 bit gain calibration constants that are copied to the Gain Calibration Buffer.

3.10.1 Calibration DAC #1 Configuration.

Calibration DAC #1 is programmed using the control signals, CAL_DAC_SDI, CAL_DAC_CLK and CAL_DAC_LD1 as defined in the Global Control register.

The mapping of this DAC' s channels to functions is as per

4	Adjusts the GAIN (full scale error) for DAC output channel #0.
5	Adjusts the OFFSET (zero scale error) for DAC output channel #0.
6	Provides a programmable reference voltage that can be measured and used to perform A/D gain calibration.
7	Adjusts the OFFSET (zero scale error) for ADC

Table 13.

Channel	Functional Description
0	Offsets the PGA when configured for GAIN = 1
1	Offsets the PGA when configured for GAIN greater than 10.
2	Adjusts the GAIN (full scale error) for DAC output channel #1.
3	Adjusts the OFFSET (zero scale error) for DAC output channel #1.
4	Adjusts the GAIN (full scale error) for DAC output channel #0.
5	Adjusts the OFFSET (zero scale error) for DAC output channel #0.
6	Provides a programmable reference voltage that can be measured and used to perform A/D gain calibration.
7	Adjusts the OFFSET (zero scale error) for ADC

Table 13 DAC #1 Channel Mapping

3.10.2 Calibration DAC #2 Configuration.

Calibration DAC #1 is programmed using the control signals, CAL_DAC_SDI, CAL_DAC_CLK and CAL_DAC_LD2 as defined in the Global Control register.

The mapping of this DAC' s channels to functions is as

Channel	Functional Description
0	Offsets the AD684 OFFSET for input channels 0 to 3.
1	Offsets the AD684 OFFSET for input channels 4 to 7.
2	Offsets the AD684 OFFSET for input channels 8 to 11.
3	Offsets the AD684 OFFSET for input channels 12 to 15.
4	Reserved
5	Reserved
6	Reserved
7	Reserved

Table 14 DAC #2 Channel Mapping

3.10.3 EEPROM Organisation

The EEPROM organised as 64 x 16 bit words with the organisational structure defined in Table 15 .

EEPROM Offset (Hex)	Stored Constant	Mapped to Calibration DAC#1 Channel No:	Nominal Value (ideal)	Valid Bit Range
0	PGA_GAINEQ1_OFFSET	0	128	8 bits (7:0).
1	PGA_GAINGT10_OFFSET	1	128	8 bits (7:0).
2	DAC(1)_REFERENCE	2	128	8 bits (7:0).
3	DAC(1)_OFFSET	3	128	8 bits (7:0).
4	DAC(0)_REFERENCE	4	128	8 bits (7:0).
5	DAC(0)_OFFSET	5	128	8 bits (7:0).
6	Test Voltage Input	6	128	8 bits (7:0).
7	ADC zero OFFSET	7	128	8 bits (7:0).
		Mapped to Calibration DAC#2 Channel No:		
10	AD684 Channel 0-3 OfFset	0	128	8 bits (7:0).
11	AD684 Channel 4-7 OfFset	1	128	8 bits (7:0).
12	AD684 Channel 8-11 OfFset	2	128	8 bits (7:0).
13	AD684 Channel 12-15 OfFset	3	128	8 bits (7:0).

		Gain Buffer Offset **(Mapped into 32 bit PCI space)**		
20	GAIN_0.5	0		14 bits (13:0).
21	GAIN_1	4		14 bits (13:0).
22	GAIN_2.5	8		14 bits (13:0).
23	GAIN_5	C		14 bits (13:0).
24	GAIN_10	10		14 bits (13:0).
25	GAIN_25	14		14 bits (13:0).
26	GAIN_50	18		14 bits (13:0).
27	GAIN_100	1C		14 bits (13:0).

Table 15 EEPROM Address Map

Both the EEPROM and Calibration DAC are accessed as serial devices. As these only need be accessed once during module initialisation this task needs to be performed by the host driver software by manipulating the serial control bits available in the GLOBAL_STATUS_REGISTER.

The EEPROM protocol and timing is defined in the data sheet for the device: MicroChip 93LC46B. To maintain compatibility with other manufacturers the suggested CLK rate should be limited to 1 Mhz.

The calibration DAC protocol is defined in the data sheet for the device : Analogue Devices AD8842.

4. Specifications

4.1 Maximum Transfer Bandwidth.

The A/D and D/A's share a data path to the FIFO interface. This limits the maximum bandwidth available to transfer data between the FIFO' s, the appropriate device and across PCI.

The maximum number of conversion cycles (14 bit A/D and D/A samples) is limited to 450 000 per second. This defines the maximum cycle clocking as per the following example:

(1) Assume A/D sampling clock set to 400 KHz.

(2) Assume D/A #1 sampling clock set to 40 KHz.

(3) Maximum D/A #2 sampling clock can be 10 KHz.

4.2 Analogue Input

4.3 Analogue Input

Differential Input Amplifier Characteristics (AD620BR)

Input Coupling	DC
Input Impedance	>1 G ohm, in parallel with 50 pF maximum.
Bandwidth	120 KHz at ± 5 V input voltage swing
Offset Voltage	± 500 uV.
Gain Error	± 0.02% (Gain = 1)
Maximum Safe Input Range	± 15V.
Maximum Operating Input Range	± 5V.

Sample and Hold Amplifier Characteristics (AD684)

Bandwidth	1 MHz at ± 5 V input voltage swing
Hold Mode Offset Voltage	± 1.2 mV
Gain Error	± 0.05%

Programmable Gain Amplifier Characteristics

Bandwidth	600 KHz at ± 5 V input voltage swing
Offset Voltage	± 200 uV
Gain Error	± 0.008%

Input Characteristics

Input signal ranges

Channel Gain (Programmable per channel)	**Input Signal Range (**Programmable per channel)
0.5	± 5 V
1	± 2.5 V
2.5	± 1 V
5	± 500 mV
10	± 250 mV
25	± 100 mV
50	± 50 mV
100	± 25 mV

Input Coupling	DC
Maximum working voltage	± 10 V relative to module ground.
Over voltage protection	± 25 V with power ON (relative to module ground)
	± 35 V with power OFF (relative to module ground)

FIFO Buffer Size	Maximum 4096 .
Channel List Buffer Size	Tracks FIFO buffer size. (Depends on number of entries)
Data Transfers	Triggered interrupts, DMA or programmed I/O.

Conversion Characteristics

Maximum Sampling Rate	400 KS/s. (For single channel)
Resolution	Fourteen bits
Relative Accuracy	± 1 LSB maximum
Gain error	± 0.02 % of reading max.

4.4 Analogue Output

Output Characteristics

Resolution	14 Bits
Maximum update rate	400 KHz to 0.02% full scale.
FIFO Buffer Size	4096 and Pattern Length. (Programmable)
Data Transfer:	Triggered interrupts, DMA or programmed IO

Conversion Characteristics (Calibrated)

Resolution	Fourteen bits
Relative Accuracy	± 1.0 LSB maximum
FULL Scale error	± 0. 9 LSB.
Zero Scale error	± 0.9 LSB.

Voltage Output Characteristics

Range	± 10 V
Output Settling Time	2.5 us to 0.02% Full scale.
Output Coupling DC	
Output Impedance	0.2 Ohm
Output Drive	± 5 mA
Power-on state	0 V

4.5 Digital I/O

Number of channels: Eight. Programmed as Input or Output per channel.

Compatibility: TTL

I/O Characteristics

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2.0 V	5.25 V
Low level input current		-100 uA
High level input current		100 uA
Output high voltage	2.40 V	
Output low voltage		0.6 V
Low level output current		-24 mA
High level output current		4 mA

4.6 Multifunction I/O (PFI)

Number of channels: Ten. Programmed as Input or Output per channel.

Can also be mapped to functions e.g. Timer output.

I/O Characteristics: As per Digital I/O

4.7 Timing I/O

Number of channels: Two : Up/Down counters/ timers

Resolution: twenty-four bits.

Base Clocks Available: 20 MHz, 100 KHz or External.

I/O Characteristics:	As per Digital I/O.

4.8 Triggers

Analogue Trigger

Trigger Source	Any of the analogue input channels.
Reference Source	Analogue Output Channel 1.
Resolution	12 bits
Level	± 10 V
Trigger Mode	Level or Edge. Greater than reference or less than reference.

Digital Trigger

Trigger Source	Two PFI inputs.
Compatibility	TTL
Pulse Width	100 ns.
Trigger Mode	Level or Edge (rising or falling) .

4.9 Bus Interface

Type	PCI 2.2. Master & Slave
	3.3V or 5.0 V compatible with auto-detect.

4.10 Power requirements

+5V (±5 %)	1.3 A

5. Installation and Configuration

5.1 Related Documentation

5.2 Software Installation

5.3 Hardware Installation