PCI-30F/G

100kHz/330kHz PCI Data Acquisition Boards

Quick Installation Manual

For PCI Compatible Computer Systems

First Edition

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CHAPTER 1: Installation

1.0) Connecting the PCI 30F/G to the PC Backplane

Requirements:
a) Any PCI Based Computer
b) Philips Screw Driver (or one to match screw on the computer cabinet and bracket)

Procedure:

a) Switch off the computer and all attached devices

b) Unplug power cord from the computer and all attached devices.

> ☞ **Warning**
>
> Failure to disconnect all power cables can result in harzardous conditions, as there may be dangerous voltage levels present in externally connected cables.

c) Remove the top cover from the PC. If you are not sure how to do this, consult the manual supplied with the system unit.

d) If you are using the PCI-30G/GA/G32/GA32 then decide on the Voltage Range you are going to use. If it is ±5V or 0-10V then no jumper changes is necessary (default setting is 10V span). However, should you decide to use ±10V then short 2-3 on Jumper LK1 on the PCI-30G/GA/G32/GA32 as illustrated in Figure 1.0a below.

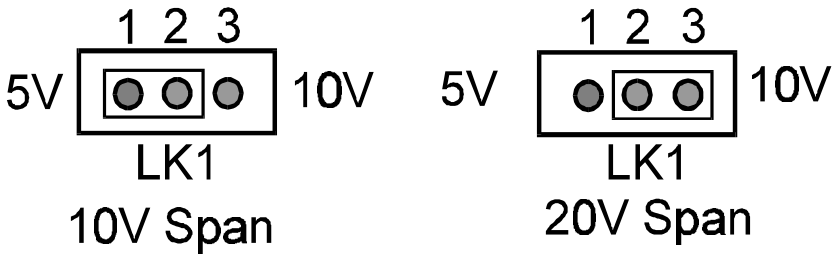


Figure 1.0a

e) Choose any PCI expansion slot and remove the screw from the metal bracket fixed corresponding to the chosen slot.

f) If you are using the Digital I/O and the optional counter timers then you must insert the Ribbon Cable into the IDC40 Header.

g) Align the gold plated edge connector with the edge socket and the rear adaptor slot with the board bracket. Firmly press the board down into the socket on the computer's system board. Ensure that the board's edge connector is in the socket and has not slipped sideways past the socket.

h) Move the Ribbon Cable [for Digital I/O] thru another empty slot on the computer.

i) Replace the screw on the bracket and tighten the screw to the back panel.

j) Replace the computer's cover. Plug in all cables and switch the computer power on. The PCI-30F/G is now installed.

CHAPTER 2: Interconnections

2.0) Introduction

The PCI-30F/G I/O board plugs into any PCI compatible slot at J1/J2. The board communicates to the User Circuit via Centronics SCSI 50 connector for the Analog Signals and an IDC40 Header for the digital signals. This chapter describes these connectors.

2.1) Connections to the PCI Bus

The PCI-30F/G board may be plugged into any PCI Compatible Slot. All data transfers to and from the host computer are channelled via these connectors (J1/J2).

2.1a) A/D Voltage Range Setting

On the 30G/GA/G32/GA32 models, can switch between ±5V and 0V to 10V. LK1 must be used to achieve the ±10V range (see below for jumper settings for the **30G/GA/G32/GA32** only). On the F and FA models, the range can be switched between ±5V and ±10V from software.

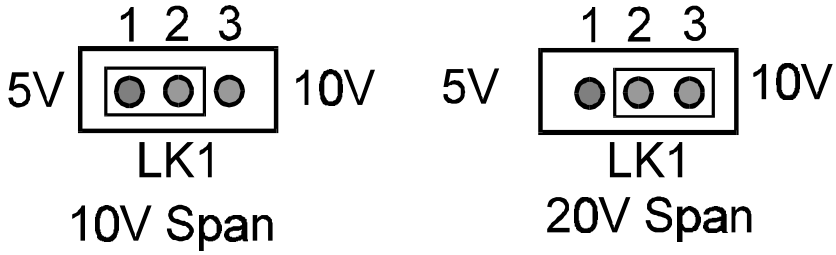


Figure 2 – 1A. PCI-30G/GA/G32/GA32 Span Jumper

On the PCI-30G/GA/G32/GA32 board, you can refer to the text written on the silk-screen layer with regard to jumper settings.

CHANGING JUMPER LK1 TO THE 20 V POSITION DOES NOT ENABLE YOU TO SELECT UNIPOLAR RANGE 0 TO 10 V.

Note that the default range setting is -5 to +5V.

2.2) PCI30F/G Analog Connector [Centronics SCSI50 Male Connector (P1)

The PCI-30F/G Analog Inputs/Outputs interfaces to the external world via an IDC40 Male Header.

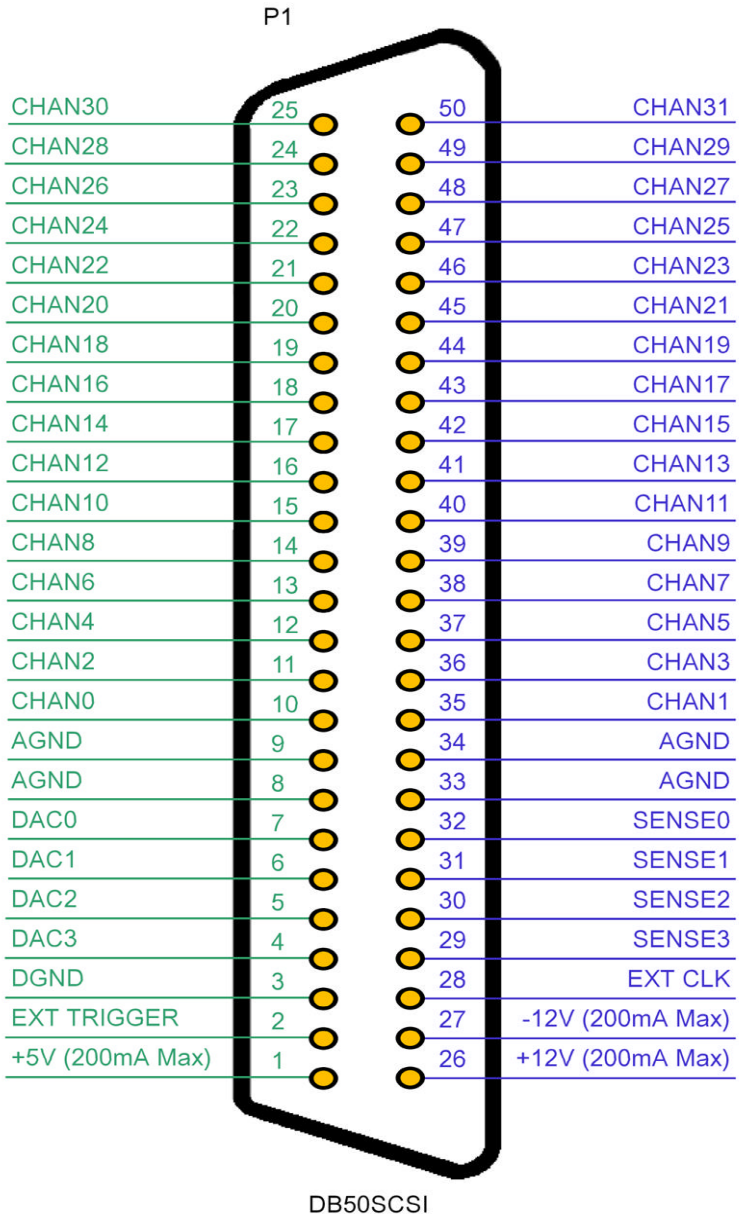


Figure 2.2: PCI-30F/G Analog Connector [P1]

Figure 2.2 graphically shows the connector together with their pin assignments. Note that the pin connections refer to the pin numbers when looking at the PCI-30F/G Analog Connector with the component side on the top.

a) **Analog Input Channels - CH0 to CH31:** CH0 to CH15 are the analog input channels in single ended mode. If differential mode is selected then CH0 thru CH7 acts as the +ve input Lines and CH8 thru CH15 acts as the –ve input lines

respectively. CH16 thru CH23 acts as the +ve Input Lines and CH24 thru CH31 acts as the –ve Input Lines.

b) **ANALOGUE GROUND:** Analogue ground lines are provided on Pins 8, 9, 33, 34 on the SCSI50 Connector [P1]. The analogue input lines are measured relative to AGND.

c) **SENSE0 to SENSE3:** These lines are the Remote Sense Lines for DAC0 thru DAC3. This lines can be used if the cables from the PCI-30GA/FA to the Load is far. Connect the DAC0 thru DAC3 outputs to the SENSE0 to SENSE3 lines @ the load Point. If the Remote Sense Input Lines are not used the you MUST short the SENSE Lines to the appropriate DAC output lines. Failure to do this will result in the DAC output voltage being permenantly set to about ±13V.

d) DAC0 to DAC3:
The Lines define the DAC Outputs of DAC0 thru DAC3 respectively.

e) **External Trigger{** XE "Signal Definitions:External Trigger" **}**. This line is jumper selectable to provide either a clock or trigger signal to the A/D, and may be read under software control. It is TTL compatible. This line can also be configured as an output to synchronise boards in master/slave modes.

f) **External Clock{** XE "Signal Definitions:External Clock" **}**. This line interfaces to the uncommitted counter/timer, and can be jumpered to perform a variety of functions, as described in the previous chapter. It may be configured either as an input or output and is also TTL compatible.

g) **+12V{** XE "Signal Definitions:+12V" **}.** This line provides a +12V power supply to the user's interface. Maximum permissible current draw is 200 mA.

h) **-12V{** XE "Signal Definitions:-12V" **}**. This line provides a -12V power supply to the user's interface. Maximum permissible current draw is 200 mA.

i) **+5V{** XE "Signal Definitions:Digital Ground/ +5V" **}**. This line provides the User to power external prototype circuitry. Maximum permissible current draw is 200 mA.

j) **Digital Ground:** Digital ground is the ground return line for External Trigger and External CLK Lines. It is internally connected to analogue ground

2.2.1) Recommended Analogue Input Schemes

Analogue signals are input into the PCI-30 either as single ended inputs or differential inputs (F, FA, F32, FA32, G, GA, G32, GA32 models only).

> ☞ **Warning**
>
> Overloading any analogue input by more than 10% may cause other input channels to become inaccurate or noisy. For PCI-30F/G inputs operating at maximum gain, this corresponds to an input voltage of 5.5 mv.

Single Ended Inputs

In single ended connections (see Figure 4 - 1), input signals share a common low side, which is analogue ground.
This has the advantage of giving the maximum number of inputs. Its major disadvantage is the loss of common mode rejection obtainable from differential mode. Single ended inputs are very sensitive to noise, and should not be used with lead lengths of greater than 18 inches, or for inputs with a gain of greater than 10.

Differential Inputs

In differential input mode (see Figure 4 - 2), two multiplexer switches per channel are used, and the A/D converter measures the difference between the high and low input lines of each channel.

In differential mode CH0 thru CH7 acts as the +ve input Lines and CH8 thru CH15 acts as the –ve input lines respectively. CH16 thru CH23 acts as the +ve Input Lines and CH24 thru CH31 acts as the –ve Input Lines.

Analogue inputs are limited to a voltage of between -10 and +10V.

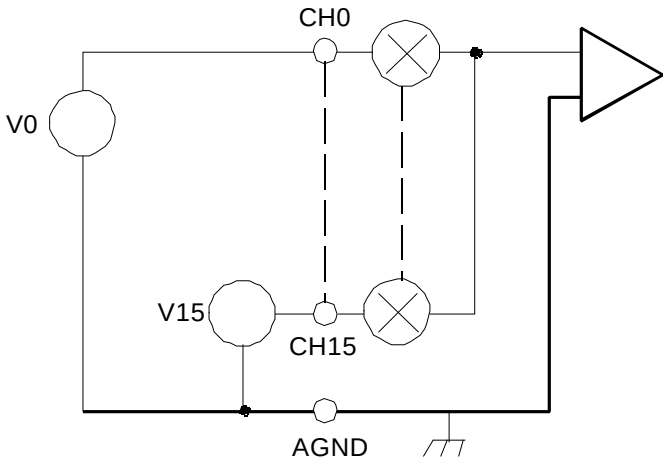


Figure 4 - 1. Single Ended Analogue Inputs

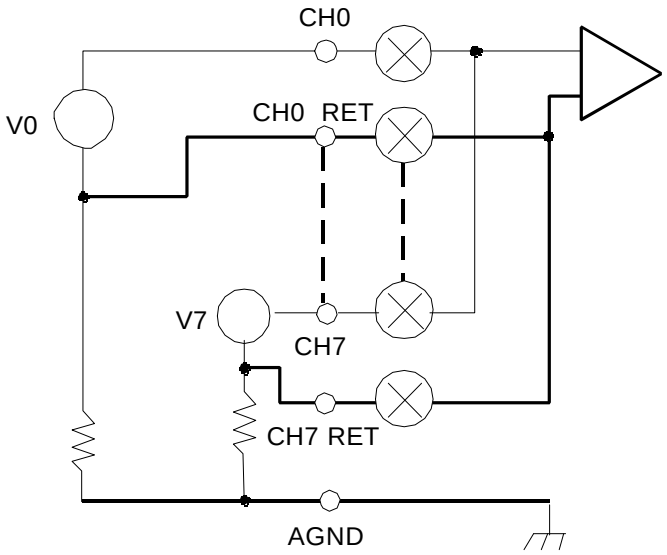


Figure 4 - 2. Differential Analogue Inputs

☞ Warning

In differential mode, all signal inputs to the PCI-30 must be referred to Analog Ground. This can be done by connecting a 1 to 10 kΩ resistor from the low end of each input to ground

Analogue Output

The analogue output lines are referenced to the analogue ground line and may be used to output either monopolar or bipolar voltages.

Connection Guidelines

The PCI-30F/G is a very high performance I/O subsystem, and was designed to have low input noise. It's performance may however be severely affected by incorrect connection techniques. This is especially true of noise levels.

Shielded Input Lines

Wherever possible, leads should be shielded. Optimally, each input line should be individually shielded. The shield should be tied to analogue ground at the instrument end of the connection only.

Grounding

If user circuitry is connected to the PCI-30 it is critical to keep the digital and analogue ground separate.

Input Voltages

To maintain the specified accuracy, all inputs to the PCI-30 must be within 110% of full scale.

Source Impedance

To maintain the specified accuracy, all devices connected to the analogue inputs of the PCI-30 must have a source impedance of less than l kΩ.

2.3) PCI-30F/G Digital I/O Male Header Connector [IDC40] (H1)

The PCI-30F/G Digital I/O interfaces to the external world via an IDC40 Male Header.

A logical Low is from 0 to 0.8V and a Logical High is from 2.0V to +5.1V. Although these are defined as TTL Levels it is recommended that a logical Low voltage is from 0V to 0.3V and a logical high is from 4.5V to 5.1V.

Connector Header (P1) details are shown below:

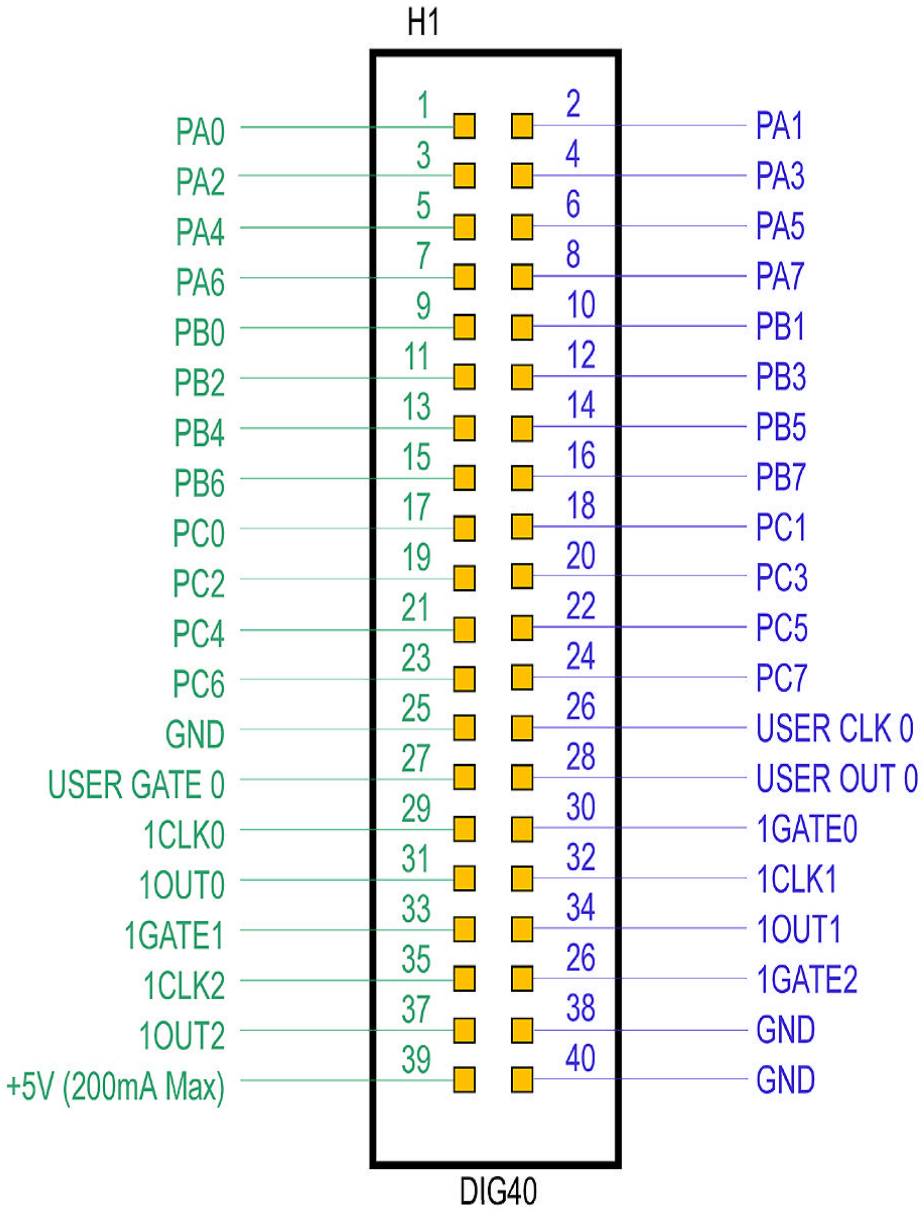


Figure 2.4a: Digital I/O Header (H1)

Note that the pin connections refer to the pin numbers when looking at the PCI-30F/G Digital I/O Header [H1] with the component side on the top.

Signal Definitions

a) **Digital Ground:** Digital ground is the ground return line for the digital inputs and outputs. Any digital circuitry tied to the digital lines should be referenced to these lines. It is internally connected to analogue ground.

b) **Port A0 - A7:-** The first digital I/O port, digital I/O port 0. It is configurable into a number of operating modes under software control.

c) **Port B0 - B7:** Digital I/O port 1. It is configurable into a number of operating modes under software control.

d) **Port C0 - C7:** Digital I/O port 2. It is configurable into a number of operating modes under software control.

e) **1CLK0:** This line is the input CLK Line to the User Counter Timer 0 (ie: Counter Timer 0 on the 2nd Counter Timer IC). It can be used to count events, measure period/frequency, etc. Note that this lie is TTL Compatible.

f) **1GATE0:** Gate Countrol Line of the User Counter Timer 0 (ie: Counter Timer 0 on 2nd Counter Timer IC). It can be used enable/disable the counting on the User Counter Timer.

g) **1OUT0:** Output Line of the User Counter Timer 0 (ie: Counter Timer 0). It can be used to generate a pulse on terminal count, output constant frequency pulses, etc.

h) **1CLK1:** This line is the input CLK Line to the User Counter Timer 1 (ie: Counter Timer 1). It can be used to count events, measure period/frequency, etc. Note that this lie is TTL Compatible.

i) **1GATE1:** Gate Countrol Line of the User Counter Timer 1(ie: Counter Timer 1). It can be used enable/disable the counting on the User Counter Timer.

j) **1OUT1:** Output Line of the User Counter Timer 1 (ie: Counter Timer 1). It can be used to generate a pulse on terminal count, output constant frequency pulses, etc.

k) **1CLK2:** This line is the input CLK Line to the User Counter Timer 2 (ie: Counter Timer 2). It can be used to count events, measure period/frequency, etc. Note that this lie is TTL Compatible.

l) **1GATE2:** Gate Countrol Line of the User Counter Timer 2 (ie: Counter Timer 2). It can be used enable/disable the counting on the User Counter Timer.

m) **1OUT2:** Output Line of the User Counter Timer 2 (ie: Counter Timer 2). It can be used to generate a pulse on terminal count, output constant frequency pulses, etc.

n) **0CLK2:** This line is the input CLK Line to the User Counter Timer 3 (ie: Counter Timer 3). It can be used to count events, measure period/frequency, etc. Note that this lie is TTL Compatible.

o) **0GATE2:** Gate Countrol Line of the User Counter Timer 3 (ie: Counter Timer2). It can be used enable/disable the counting on the User Counter Timer.

p) 0OUT2: Output Line of the User Counter Timer 3 (ie: Counter Timer2). It can be used to generate a pulse on terminal count, output constant frequency pulses, etc.

q) +5V: This line provides the User to power external prototype circuitry. Maximum permissible current draw is 500 mA. This line is protected from short circuits and overloads via a polyswitch.

> **Warning**
>
> DO NOT exceed 5.1V or fall below 0V on the I/O ports of the PCI-30F/G. Permanent damage will result if these thresholds are exceeded.

2.4) Power supply connections

The +5V power and digital ground are available on the IDC40 Male Header (H1). These are equipped with Polyswitches that will open circuit if the max permissible current of 500mA is exceeded. Connections to the power lines will be restored if the current falls below the max permissible current draw.

> **Warning**
>
> The maximum permissible current draw on the +5V lines on the I/O connectors is 500mA.

Chapter 3: Calibration

Introduction

This chapter contains information on the calibration procedures for the A/D and D/A sub-systems on the PC30 series of boards.
These procedures should be performed at six month intervals, or whenever the input or output range jumpers are changed.

Allow the host PC and the board to warm up for at least 15-30 minutes before calibration.

A/D Calibration

A/D calibration is performed by adjusting three trimpots. These trimpots are easily located on the PC30 board itself.

Requirements:

a. Calibration is done on channel 1. The recommended connector wiring is shown in Figure 3 - 1.
b. Calibration is performed with the board jumpered into its intended operating mode.
c. All cables should be as short as possible. Note that screened cable is preferable in order to minimise noise interference.

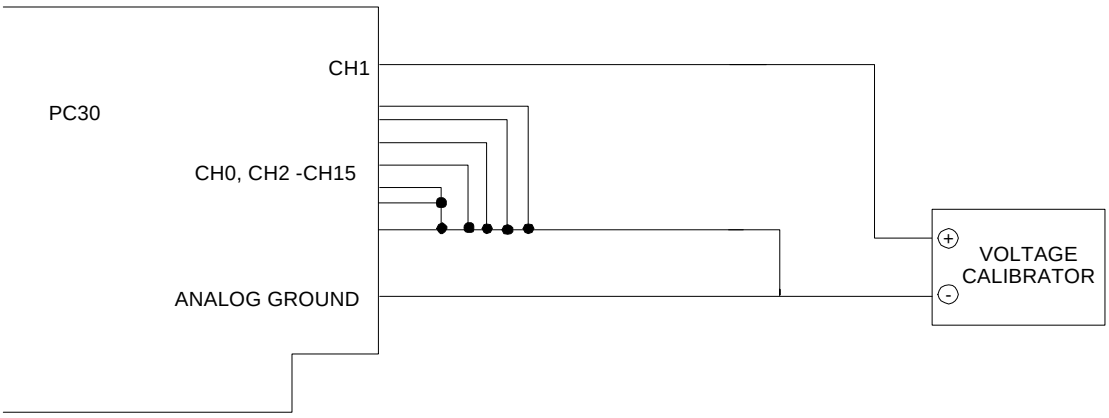


Figure 3 - 1. A/D Calibration Connections

Equipment Required

a. Precision voltage source. Range +10V to -10V, with an absolute accuracy better than 0.005%, resolution 100 nV or better.

b. Precision digital multimeter with ±10V range, absolute accuracy better than 0.0005%, resolution 100 nV or better.

Calibration Software

Run any of the following programs in the EDRE SubDir:

EDRE\Examples\VC\AD_Polled\Release\AD_Polled.exe	[Win '95/98/NT]
EDRE\Examples\VB\PCI30FG\ADPoll\ADPoll.exe	[Win '95/98/NT]
EDRE\Examples\VB\PCI30FG\Voltmeter\Voltmeter.exe	[Win '95/98/NT]
EDRE\Examples\VJ\PCI30FG\ADPoll\Simple.exe	[Win '95/98/NT]
EDRE\Examples\VJ\PCI30FG\Voltmeter\Simple.exe	[Win '95/98/NT]

A/D Calibration for the PCI-30G/GA/G32/GA32 Boards

Bipolar Mode

1. Adjust A/D for maximum gain (ie. 1000) and apply 0.00mV to Channel 1 (all other channels must be grounded to AGND). Adjust VR1, the instrumentation amplifier offset pot, for output 800H.
2. Set A/D for a gain of 1 and apply (-FS+2LSB) to channel 1 (ie. -4.9988V for ±5V or -9.9976V for ±10V). Adjust VR2 for an output code which flickers between 000H and 001H.
3. Set A/D for a gain of 1 and apply (+FS-3/2LSB) to channel 1 (ie. +4.9963V for ±5V range or +9.9927V for ±10V). Adjust VR5 for an output code which flickers between FFEH and FFFH.
4. Repeat the above steps until no further adjustment is required.

Monopolar Mode

1. Adjust A/D for maximum gain (ie. 1000) and apply 0.00mV to Channel 1 (all other channels must be grounded to AGND). Adjust VR1, the instrumentation amplifier offset pot, for output code 000H.
2. Set A/D for a gain of 1 and apply (FS+2LSB) to channel 1 (ie. for 0 to 10V range it should be +1.22mV). Adjust VR3 for an output code which flickers between 000H and 001H.
3. Set A/D for a gain of 1 and apply (+FS-3/2LSB) to channel 1 (ie. +9.9963V). Adjust VR6, gain pot for an output code which flickers between FFEH and FFFH.
4. Repeat the above steps until no further adjustment is required.

☞ Note [±10V Operation]

For ±10V, you must short 2-3 on LK1 [Span Jumper on the PCI-30G/GA/G32/GA32].

Bipolar Mode (±5V)

1. Adjust A/D for maximum gain (ie. 1000) and apply 0.00mV to Channel 1 (all other channels must be grounded to AGND). Adjust VR1, the instrumentation amplifier offset pot, for output code 800H.
2. Set A/D for a gain of 1 and apply (+FS-3/2LSB) to channel 1 (ie. +4.9963V). Adjust VR7, gain pot, for an output code which flickers between FFEH and FFFH.
3. Set A/D for a gain of 1 and apply (-FS+2LSB) to channel 1 (ie. -4.9988V). Adjust VR3, bipolar A/D offset, for an output code which flickers between 000H and 001H.
4. Repeat the above steps until no further adjustment is required.

   Note that steps 2 and 3 above are inter-related, and it therefore requires some expertise to enable ± Full Scale Convergence.

Bipolar Mode (±10V)

1. Adjust A/D for maximum gain (ie. 1000) and apply 0.00mV to Channel 1 (all other channels must be grounded to AGND). Adjust VR1, the instrumentation amplifier offset pot, for output code 800H.
2. Set A/D for a gain of 1 and apply (+FS-3/2 LSB) to channel 1 (ie. +9.9927V). Adjust VR8, gain pot, for an output code which flickers between FFEH and FFFH.
3. Set A/D for a gain of 1 and apply (-FS+2LSB) to channel 1 (ie. -9.9976V). Adjust VR9, bipolar A/D offset, for an output code which flickers between 000H and 001H.
4. Repeat the above steps until no further adjustment is required.

   Note that steps 2 and 3 above are inter-related, and it therefore requires some expertise to enable ± Full Scale Convergence.

☞ Warning

Ensure that the Simultaneous Sample/Hold PCI-30xx boards are powered (ie: switch computer on) before applying any signals to the analog input channels. Damage to the Sample Hold IC will result if analog signals (> 20mV) are fed into the analog input channels if the power is not applied to the PCI-30xx.

WHEN CONNECTING THE CALIBRATION SOURCE TO CHANNEL 1, ENSURE THAT YOU USE SHIELDED CABLE SO THAT NOISE INTERFERENCE IS KEPT TO A MINIMUM.

The input impedance on the sample/hold channels is 50 MΩ/pF. This makes it extremely sensitive to noise if improper cables/ connections are made.

You can decrease the input impedance by connecting a resistor from the input channel to AGND (eg. 100 kΩ resistor from CH1 to AGND). You should only decrease the input impedance if the noise levels exceed 22mV.

Bipolar Mode

1. Adjust A/D for maximum gain (ie. 1000) and apply 0.00mV to Channel 1 (all other channels must be grounded to AGND). Adjust VR1, the instrumentation amplifier offset pot, for output 800H.
2. Set A/D for a gain of 1 and apply (-FS+2LSB) to channel 1 (ie. -4.9988V for ±5V or -9.9976V for ±10V). Adjust VR2 for an output code which flickers between 000H and 001H.
3. Set A/D for a gain of 1 and apply (+FS-3/2LSB) to channel 1 (ie. +4.9963V for ±5V range or +9.9927V for ±10V). Adjust VR5 for an output code which flickers between FFEH and FFFH.
4. Repeat the above steps until no further adjustment is required.

☞ Warning

Ensure that the Simultaneous Sample/Hold PCI-30xx boards are powered (ie: switch computer on) before applying any signals to the analog input channels. Damage to the Sample Hold IC will result if analog signals (>20mV) are fed into the analog input channels if the power is not applied to the PCI-30xx.

WHEN CONNECTING THE CALIBRATION SOURCE TO CHANNEL 1, ENSURE THAT YOU USE SHIELDED CABLE SO THAT NOISE INTERFERENCE IS KEPT TO A MINIMUM.

The input impedance on the sample/hold channels is 50 MΩ/pF. This makes it extremely sensitive to noise if improper cables/ connections are made.

You can decrease the input impedance by connecting a resistor from the input channel to AGND (eg. 100 kΩ resistor from CH1 to AGND). You should only decrease the input impedance if the noise levels exceed 22mV.

Bipolar Mode (±5V)

1. Adjust A/D for maximum gain (ie. 1000) and apply 0.00mV to Channel 1 (all other channels must be grounded to AGND). Adjust VR1, the instrumentation amplifier offset pot, for output code 800H.
2. Set A/D for a gain of 1 and apply (+FS-3/2LSB) to channel 1 (ie. +4.9963V). Adjust VR7, gain pot, for an output code which flickers between FFEH and FFFH.
3. Set A/D for a gain of 1 and apply (-FS+2LSB) to channel 1 (ie. -4.9988V). Adjust VR3, bipolar A/D offset, for an output code which flickers between 000H and 001H.
4. Repeat the above steps until no further adjustment is required.
5. Note that steps 2 and 3 above are inter-related, and it therefore requires some expertise to enable ± Full Scale Convergence.

A/D Calibration Software

The calibration programs (listed below) supplied on the distribution disk, automates the above procedure. Note that for correct operation, the set-up information supplied in the first menu must be correct.

Run any of the following programs in the EDRE SubDir:

EDRE\Examples\VC\AD_Polled\Release\AD_Polled.exe
EDRE\Examples\VB\PCI30FG\ADPoll\ADPoll.exe
EDRE\Examples\VB\PCI30FG\Voltmeter\Voltmeter.exe
EDRE\Examples\VJ\PCI30FG\ADPoll\Simple.exe
EDRE\Examples\VJ\PCI30FG\Voltmeter\Simple.exe

DAC0 to DAC3 Calibration

Setting the Reference Voltage

The DAC reference voltage is set 10.000V (factory default). This is normally done during manufacturing, but if the voltage does not match, re-calibrate as follows:

+10V

Connect the multimeter to analogue ground and Pin 1 of U16 or the +ve side of C97. The voltage reading should be +10.0000V. If the voltage is out of specification, adjust VR4.

A convenient method is to set DACs to ±10V output. Set DAC output to +10V using Voltmetr. Measure the output voltage on the output of DAC0 (Short SENSE0 to DAC0) [ie. Pin 7 and Pin 32 of SCSI50 Connector]. Adjust VR4 until a voltage of 10.000V is reached.

In general, you do not need to calibrate the DACs at all, because it has already been done when adjusting the reference voltages (ie. usually during manufacturing). However, if you require a different full scale output on these DACs, proceed as follows:

1. Run the VOLTMETR.EXE program from the EDR sub-directory.
2. Select DAC calibration. Alternatively, you can run Waveview and set DAC0 to maximum full scale (ie. 10V).
3. Connect the multimeter to the output of DAC0 and analogue ground. Ensure you short SENSE0 to DAC0 if the sensing function is not used.
4. Adjust the Reference Pot VR4 until you obtain the required voltage output.

Chapter 4: Troubleshooting the PCI-30xx Boards

Introduction

If you are experiencing problems, first check the following:

1. Remove the PCI-30, and check that all ICs are firmly seated in their sockets, that there is no obvious damage to any components, and that the edge connector fingers on the PCI-30 are clean.
2. Check that the PCI-30 is jumpered correctly for your application. In this case only on Jumper [LK1] is applicable for the PCI30G/GA/G32/GA32.
3. Replace the PCI-30, and check that it seats firmly in the host PC's motherboard. Also check that no components are touching an adjacent board.
4. Check that the cable is securely plugged into the PCI-30.

The Diagnostics Function

The PCI-30 contains a very comprehensive diagnostics program. All of the supplied demo programs as well as the calibration program use this, and it can be used to diagnose malfunctions on the PCI-30. In fact, the only PCI-30 malfunctions which it will not detect are the following:

a. Damaged input multiplexer.
b. Damaged D/A output amplifier.
c. Damaged digital input or output lines.

Common Problems

PCI Diags cannot find board

Quite possibly the PCI-30 Board is not seated correctly in the PCI-Slot. Power the computer off and re-insert the PCI-30 Card. Rerun demo software. The proble mshould be solved.

If it still fails then the PCI-30 Board might be damaged. Return to distributor for repairs.

A/D Output Codes All Zeros or All Ones

This is typically as a result of floating inputs, or an overload. If you have exceeded the maximum input voltage (±35V with the computer switched ON, ±25V in an OFF state), you may have damaged the input multiplexers. If so, return the board to your dealer for repair.

Note that we NOT recommend that the A/D input voltage should go any near the max specified input voltage. It should be kept within ±10.5V.

A/D Readings Are Noisy

This can be caused by one of the following:

a. Long leads.
b. An electrically noisy environment.
c. Overloads on other input channels. Note also that if an input channels is overloaded it may saturate in such a way as to give a reading which appears to be in the normal range, but is very noisy.
d. Excessive source resistance. The source resistance of the devices connected to the inputs of the PCI-30 should not be greater than l K.

First Reading in a Series is Inaccurate

This is normally as a result of an overload on another input, or long leads, or a very high source impedance.

The Board Does Not Operate at Full Throughput

The PCI-30 is a very high performance board, and makes correspondingly high demands on the PC in which it is installed. If you find that your PCI-30 cannot operate at full throughput, here are some points to check.

a. To achieve full throughput, try running the minimal amount of programs in multitasking enviroments such as Win 95/98/NT/2000.
b. Ensure that you Computer is fast enough. A Pentium II or Higher is recommended.

Readings from Channel 0 through 15 are Erratic and Unstable

It is possible that the Multiplexer is faulty probably because the max voltage specification was exceedcd. Although the PCI-30 has Analog Input protection of ±35V (Power ON) and ±25V (Powered Off), it is possible that a spike > the above spec entered the analog input channels thereby destroying the Mux.

First check the operation of the board using the calibration program or demo program under the enviroment you are working in.

Go to the EDRE Control Panel Applet and check if the board is setup correctly. If it was detected, then close the EDRE Control Panel Applet and run a Demo prgram: EDRE\Examples\VB\PCI30FG\Voltmeter\Voltmeter.exe. The voltages should be displayed on the screen. If it is still erratic, then the MUXes might have blown. Return the Board to your nearest distributor for repairs.

Voltage readings are half the normal value on all the A/D channels

The span jumper LK1 on the PCI-30F/G Boards is used to select the voltage range of ±5V or ±10V. Ensure that you are using the correct range voltage.

Precautionary Statement on the PCI30GS4 / GAS4 / GS16 / GAS16 / FS4 / FAS4 / FS16 / FAS16 Boards

☞ Warning

Ensure that the Simultaneous Sample/Hold PCI-30xx boards are powered (ie: switch computer on) before applying any signals to the analog input channels. Damage to the Sample Hold IC will result if analog signals are fed into the analog input channels if the power is not applied to the PCI-30xx.

All analog input lines should have an input voltage of less than 20mV if no power is applied to the PCI-30xx Cards. In other words, it is extremely important that power is applied to the PCI-30xx card BEFORE applying any analog signals to the analog input channels.

If the analog inputs exceeds a voltage > 20mV when power to the PC is off, the Sample Hold Chip Input Transistor is turned on in the most unfortunate configuration. This will effectively degrade and damage the part.

The 1 year warranty on the PCI-30xx boards does not cover the Sample Hold ICs.

If there is any chance of the Power to the PC being off when the applied analog signals are > 20mV, we recommend an input buffering circuit powered by the PC's ±12V or +5Vsupply.

A simple Reed Relay for each channel powered by the +5V of the PC will do. If the Computer is ON then the relays are energised and the Analog Signals will be connected to the PCI-30xx Boards. If the computer is OFF for any reason then the relays will de-energise resulting in the analog signals being disconnected from the PCI-30xx Boards.

Note: PCI-30xx denotes any of the simultaneous S/H boards, viz: PCI-30GS16/ GAS16/ GS4/ GAS4/ FAS16/ FS16/ FAS4/ FS4

Pointers on the PCI30GS4 / GAS4 / GS16 / GAS16 / FS4 / FAS4 / FS16 / FAS16 Boards

Channel 0 thru 3 / 4 thru 15 Mismatch on the PCI30GS4/GAS4/FS4/FAS4 Boards

On the PCI30GS4/GAS4/FS4/and FAS4 boards, calibration is done for the simultaneous sample and hold channels (CH0 to CH3) in burst mode. The rest of the channels will be slightly offset from the first four channels because the sample and hold IC creates an offset of between 10mV to 50mV. For example, if 1.000V was applied to all the channels, then the first four will display 1.000V (after calibration) while the other channels will display 1.030V. This is approximately 30mV above (or below) the required level.

There are two ways to solve this problem:

1. Recalibrate the board for the last 12 channels only. This will level shift the first four channels by a factor of about 30mV.
2. Use software to null the 30mV offset on the last 12 channels.

Burst Mode and Polled I/O Voltage Mismatch

In certain clone computers, the voltages displayed using polled I/O might be slightly offset by about 10 to 20mV than when using normal/burst mode. This is normal since the calibration is done only in burst mode. The reason for the offset is that in Burst mode, the sample/hold ICs are more active (ie. strobes on the S/H line as a function of the CLK frequency). This shifts the AGND level by about 10 to 20mV.

To solve this problem, you should calibrate your board in one mode only. The demo program in the EDR\EXAMPLES\ Subdir calibrates these boards in burst mode only as it is assumed that the user will be using burst mode to simultaneously sample data. Any other method of data acquisition will make simultaneous sampling superfluous.

Sampled Data Indicates Excessive Noise Levels

The probable causes of this fault are:

1. **Improper Connections to the Channels, Analogue Ground**

   Ensure that each analogue channel is properly shielded and its return line connected to Analogue Ground (ie. at the SCSI50 connector pin 8 or 9 or 34 or 35). Military grade shielded cable can keep noise reduction to a minimum.

You can also decrease the input impedance by connecting a resistor from the input channel to AGND (eg. 100kΩ resistor from CH1 to AGND). Some experimentation will be required to determine the most suitable resistor.

Note that you should only decrease the input impedance if the noise levels exceed 22 mV.

2. **Maximum Voltage Inputs to the Simultaneous Sample and Hold ICs was Exceeded**

   In most cases spikes exceeding the maximum allowable input voltage (ie. ±5.004V) to the Sample and Hold ICs will result in degradation and subsequent unstable readings on its outputs. If this happens, you will have to replace the Sample and Hold ICs. Contact your distributor for more information about the replacement parts.

3. **Excessive Environmental Conditions Appear to Induce Noise on the Analogue Input Lines**

   If this problem occurs, it is very difficult to identify the exact noise source origin. The best solution is to use digital averaging to filter the noise.

   Since noise is often cyclic over a time period, the easiest way to filter it is to use digital averaging. For example, assuming you are sampling two channels at 10kHz in burst mode, try oversampling it five times and take five readings. In other words, set the burst frequency to 100kHz and take five samples for each channel. Next, add each of the five channels voltages together and divide by five. This will give you an accurate and stable result.

   This will be the easiest way to filter out the noise in extremely harsh environments.

DAC Outputs clips to ±13V irrespective of DAC Input Data

The probable causes of this fault is:

1. **DAC SENSE Lines are not connected to the appropriate DACS.**

   If the DAC Sense Lines are not used, you MUST short the SENSE Lines to the appropriate DACS. Table below lists the DACs and SENSE Lines together with their pin numbers.

DAC Number	DAC Pin	SENSE Line	SENSE Pin Number
DAC0	7	0	32
DAC1	6	1	31
DAC2	5	2	30
DAC3	4	3	29

If the SENSE Lines are connected to the appropriate DAC and the DAC Output Voltages does not reflect the input data written then the DAC might be faulty. Replace U55 (socketed) or return the Board to your distributor. If and only if you are a Professional Engineer/Technician, you may replace the U55 yourself. Contact your distributor for a replace DAC [AD664JP] or contact your nearest Analog Devices Distributor.

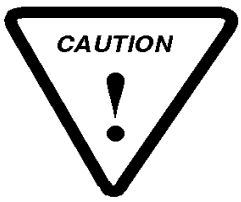
Parts replacement on the Board must only be done by a suitably TRAINED ENGINEER OR TECHNICIAN with the appropriate tools. Failing this, return the board to your distributors for repairs.

Digital I/O lines does not read the correct values on the Ports when configured as Inputs.

The probable causes of this fault is:

1. **I/O ports not are configured as Inputs or IC is faulty.**

   Use EDRE to configure the I/O Ports correctly. If EDRE is used and the problem persists then the PPI is faulty probably because the max input voltage specification was exceedcd. Ensure that the Inputs are TTL Compatible (Min Voltage: 0V, Max Voltage: 5.2V). Replace U5 (socketed) or return the Board to your distributor. If and only if you are a Professional Engineer/Technician, you may replace the U59 yourself. Contact your distributor for a replacement NEC 71055L or Intel I82C55-10 [All PLCC44 Version] or contact your nearest Intel, NEC, UMC or Tundra Distributor.



Parts replacement on the Board must only be done by a suitably TRAINED ENGINEER OR TECHNICIAN with the appropriate tools. Failing this, return the board to your distributors for repairs.

Pushbutton Interface to Digital Port gives random readings.
Detailed Description:

I connected a push button to one of the port lines. When it is closed it is set to +5V (yield a logical 1) and the program reads a logical 1. However, when it is open, random numbers are read by the program on port A.

Solution:

1. **'PullDown' Resistor required when switch is in an open state.**

   When the push button is not connected, it seems that the port line is floating (not connected). You must connect a 'pulldown' resistor (experiment from 330R to 1k) to the port line in order to ensure that it is in a defined state. Also note that if a port is configured as an input then all unused lines MUST be grounded to Digital Ground.

Chapter 5: Testing the PCI-30F/G

Before attempting to interface the PCI-30F/G with your application, it is essential that you test the board first. This is done using the following procedure:

5.1) Testing the PCI-30F/G Board

a) Install the PCI-30F/G hardware as explained above.

b) Switch the Computer on and boot from an OS [DOS, Win ’95/98 or NT] of your choice.

b) Insert the EDR CD and run Setup under Win ‘95/98 or NT in order to install the all the files.

c) For Windows NT: Run Install.bat in EDRE\WinNT\PCIXX\ directory.
Copy edrapi.dll and edrecfg.cpl from EDRE\UTILS\ to WINNT\SYSTEM32.

d) Reboot Computer

e) Test card by running the **EAGLEDAQ control panel applet**. Check if the board was detected.

f) Apply a voltage onto any of the A/D channels (Eg: CH0) and ground all the used A/D channels to AGND.

g) Run any of the following A/D programs depending on the enviroment you are in:

EDRE\Examples\VC\AD_Polled\Release\AD_Polled.exe	[Win ‘95/98/NT]
EDRE\Examples\VB\PCI30FG\ADPoll\ADPoll.exe	[Win ‘95/98/NT]
EDRE\Examples\VB\PCI30FG\Voltmeter\Voltmeter.exe	[Win ‘95/98/NT]
EDRE\Examples\VJ\PCI30FG\ADPoll\Simple.exe	[Win ‘95/98/NT]
EDRE\Examples\VJ\PCI30FG\Voltmeter\Simple.exe	[Win ‘95/98/NT]

Check of the voltages displayed on the screen corresponds to the input voltage feed into the inputs. If so then the A/D is functioning normally.

The PCI-30F/G is now ready for use.

5.2) EDRE Functions for PCI-30F/G

Function List:

void __stdcall EDRE_GetAPIInfo(long *Major, long *Minor, long *Build, long *NumDev, long *OS);
long __stdcall EDRE_GetBoardInfo(unsigned long Sn, EDRE_BoardInfo *Bboardinfo);
long __stdcall EDRE_GetSerialNo(unsigned long DevNum, unsigned long *SerialNo);
long __stdcall EDRE_DioWrite(unsigned long Sn, unsigned long Port, unsigned long Value);
long __stdcall EDRE_DioRead(unsigned long Sn, unsigned long Port, unsigned long *Value);
long __stdcall EDRE_CTWrite(unsigned long Sn, unsigned long Ct, unsigned long Value);
long __stdcall EDRE_CTRead(unsigned long Sn, unsigned long Ct, unsigned long *Value);
long __stdcall EDRE_CTSoftGate(unsigned long Sn, unsigned long Ct, unsigned long Gate);
long __stdcall EDRE_CTCfg(unsigned long Sn, unsigned long Ct, unsigned long Mode,
unsigned long Src, unsigned long BCD, unsigned long CTIsr);

long __stdcall EDRE_StrBoardType(unsigned long Sn, char *StrBoardType);
long __stdcall EDRE_StrError(unsigned long Error, char *StrError);
long __stdcall EDRE_DAWrite(unsigned long Sn, unsigned long Channel, long uVoltage);
long __stdcall EDRE_ADSingle(unsigned long Sn, unsigned long Channel, unsigned long Gain, unsigned long Bip, unsigned long Diff, long *uVoltage);

long __stdcall EDRE_ADConfig(unsigned long Sn, unsigned long *Freq, unsigned long Mode, unsigned long Burst, unsigned long Bip, unsigned long Dif,

unsigned long *ChanList, unsigned long *GainList, unsigned long ListSize);
long __stdcall EDRE_ADStart(unsigned long Sn);
long __stdcall EDRE_ADStop(unsigned long Sn);
long __stdcall EDRE_ADGetData(unsigned long Sn, long *Buf, unsigned long *BufSize);
long __stdcall EDRE_ADStatus(unsigned long Sn, unsigned long StatusMode, unsigned long *Status);

A detailed installation procedure is given in the EDRE Software Manual.