Eagle Technologies

PCI-14B/C DIO and Counter Module

Technical Manual

Revision 1.00 August 2000

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1. Module Features

- The PCI-14B/C Digital I/O and Counter module is PCI 2.2 compliant at 33 Mhz.
- The modules are 3.3V PCI slot compatible.
- Includes six (Option B) or two (Option C) 24 bit counter timers. Compatible with 82C54 modes. Configurable for external Gate and Clock signals to 8 Mhz. or internal Gate and Clock signals to 40 Mhz.
- 50mA sink, 20mA source digital outputs with short circuit protection. High impedance on power up/loss.
- Overvoltage protection on all digital inputs.
- Overvoltage protection on digital outputs (Option B only).
- Programmable Interrupt generation on Counter Timers as well as eight digital inputs.
- Serial EEPROM for module Identification etc.

There are two PCI-14B DAQ module option ranges. The ranges and features of each are defined in Table 1.

Feature	**PCI14B**	**PCI14C**
Number of Digital Input Channels	24	24
Number of Digital Output Channels	24	24
Number of 24 Bit Timer Counters	6	2
High Voltage Digital Input Protection (see I/O specs.)	Yes	Yes
High Voltage Digital Output Protection	Yes	No

Table 1 PCI14B-X Module Options

2. Functional Overview

This chapter provides a functional overview of the PCI14B-X module.

2.1 Module Configuration and Address Map

The module uses the Actel PCI Core in Target only mode to interface to the PCI bus. This core thus defines much of the software protocol used to access the module.

The PCI14B module's control registers are mapped as per Table 2. All registers are memory mapped and 32 bit aligned. Base Address Register 0 defines the module's base address.

Vendor ID		**EA01 (hex)**
Device ID		**014B (hex) Six Timer Option** **014C (hex) Two Timer Option**
Configuration Register BAR0 used as the base.		
Offset Address (Hex)	**Register Name**	**Description**
000	COUNTER 0 MODE	Mode Control Register .
004	COUNTER 0 COUNT	Writes the Initial count and reads the current count.
008	COUNTER 0 CONFIG	Defines the Internal/External counter configuration.
010	COUNTER 1 MODE	Mode Control Register
014	COUNTER 1 COUNT	Writes the Initial count and reads the current count.
018	COUNTER 1 CONFIG	Defines the Internal/External counter configuration
020	COUNTER 2 MODE	Mode Control Register
024	COUNTER 2 COUNT	Writes the Initial count and reads the current count.
028	COUNTER 2 CONFIG	Defines the Internal/External counter configuration
030	COUNTER 3 MODE	Mode Control Register
034	COUNTER 3 COUNT	Writes the Initial count and reads the current count.
038	COUNTER 3 CONFIG	Defines the Internal/External counter configuration
040	COUNTER 4 MODE	Mode Control Register
044	COUNTER 4 COUNT	Writes the Initial count and reads the current count.
048	COUNTER 5 CONFIG	Defines the Internal/External counter configuration
050	COUNTER 5 MODE	Mode Control Register

054	COUNTER 5 COUNT	Writes the Initial count and reads the current count.
058	COUNTER 5 CONFIG	Defines the Internal/External counter configuration
080	INTERRUPT MASK	Defines interrupt mask bits for the 14 interrupt sources
084	INTERRUPT CONTROL	Defines edge/level configurations for the interrupt sources
088	INTERRUPT STATUS	Defines the status of the current interrupting source
08C	OUTPUT CONTROL	Configures DIO or Counter TC outputs for OUTPUT<5:0>. Provides a global output enable signal.
090	OUTPUT REGISTER	Defines source bits for the 14 discrete outputs.
0A0	INPUT REGISTER	Returns the status of the 24 discrete input signals
0B0	EEPROM CONTROL	EEPROM Output and Input Bits.

Table 2 PCI-14B Register Address Map

2.2 Control Register Bit Definition

2.2.1 Counter Timer Registers

Each counter timer has a set of associated registers with the following control definitions:

2.2.1.1 COUNTER MODE REGISTER (Write Only)

A three bit register defining the operating mode of the counter. These modes are compatible with the modes provided by the 82C54. Bits < 2 : 0 > of this register select the mode as follows:

< 2 : 1 : 0 >

0 : 0 : 0	Mode 0
0 : 0 : 1	Mode 1
0 : 1 : 0	Mode 2
0 : 1 : 1	Mode 3
1 : 0 : 0	Mode 4
1 : 0 : 1	Mode 5

Writing this register always forces an initialisation of the Terminal Count (TC) output of the associated timer.

2.2.1.2 COUNTER COUNT REGISTER (Write: Initial Count. Read: Current Count)

Each counter is twenty four bits wide.

On WRITES , this register defines the initial count value. Depending on the MODE this value is automatically re-loaded at each terminal count

On READS, the current value of the counter is returned. The current counter value is always returned as a 32 bit result with the top eight bits set to “0”.

Writing this register always forces an initialisation of the Terminal Count (TC) output of the associated timer.

2.2.1.3 COUNTER CONFIG REGISTER (Write only)

A three bit register defining the configuration of the counter as follows:

Bit < 0 > Specifies the clock source

0 Clock source is the Internal 40 Mhz clock. This is the reset value.

1 Clock source is the external clock

Bit < 2 : 1 > Specifies the counter GATE

0 : 0	GATE is always ‘0’.
0 : 1	GATE is always ‘1’.
1 : 0	GATE will follow the associated counter’s external GATE signal.

Writing this register always forces an initialisation of the Terminal Count (TC) output of the associated timer.

2.2.2 Interrupt Configuration Registers

Fourteen programmable interrupts are supported. Six from the counter timer terminal count (TC) outputs and eight from the bottom eight input discretes. The interrupt architecture, using Input(0) as an example, is shown in Figure 1.

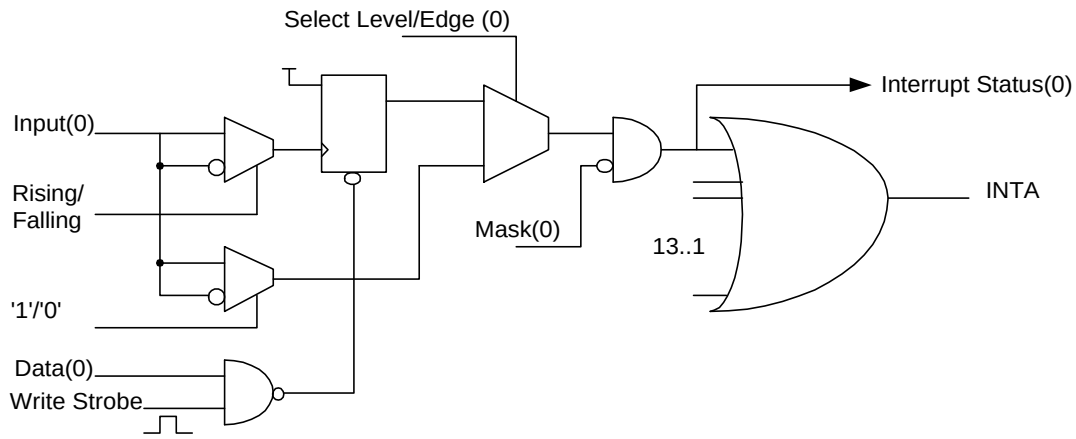

Figure 1 Programmable Interrupt Architecture

The configuration is defined by three control registers as defined below.

2.2.2.1 Interrupt Mask Register (Write only)

The PCI-14 module supports fourteen programmable interrupts. Six derived from the six counter timer terminal count (TC) outputs and eight from discrete inputs INPUT<7:0>.

This register provides a bit for each interrupt source. Each bit defines whether the associated source participates in the interrupt generation logic. A ‘1’ masks out the corresponding interrupt while a ‘0’ enable the corresponding interrupt. This register is set to all ‘1’s on reset.

The bit/source allocation is as follows:

Bit(0): Input(0)
Bit(1): Input(1)
Bit(2): Input(2)
Bit(3): Input(3)
Bit(4): Input(4)
Bit(5): Input(5)
Bit(6): Input(6)
Bit(7): Input(7)
Bit(8): Timer Counter 0 Terminal Count - TC(0)
Bit(9): Timer Counter 1 Terminal Count - TC(1)
Bit(10): Timer Counter 2 Terminal Count - TC(2)
Bit(11): Timer Counter 3 Terminal Count - TC(3)
Bit(12): Timer Counter 4 Terminal Count - TC(4)
Bit(13): Timer Counter 5 Terminal Count - TC(5).

Note that the interrupt mask bit is applied after the edge/level control logic.

2.2.2.2 Interrupt Control Register (Write only)

Each of the fourteen interrupt sources can be programmed to be edge/level and polarity sensitive. The interrupt control register provides two bits for each associated interrupt source defining the configuration for each source. Each bit couple is encode as follows:

Edge/Level Bit Encoding: BIT < N : N-1 >

0 : 0	Rising Edge
0 : 1	Falling Edge
1 : 0	Level = '1'
1 : 1	Level = '0'.

This register thus has twenty eight control bits mapped to interrupt sources as follows:

Bit(1:0):	Input(0)
Bit(3:2):	Input(1)
Bit(5:4):	Input(2)
Bit(7:6):	Input(3)
Bit(9:8):	Input(4)
Bit(11:10):	Input(5)
Bit(13:12):	Input(6)
Bit(15:14):	Input(7)
Bit(17:16):	Timer Counter 0 Terminal Count - TC(0)
Bit(19:18):	Timer Counter 1 Terminal Count - TC(1)
Bit(21:20):	Timer Counter 2 Terminal Count - TC(2)
Bit(23:22:	Timer Counter 3 Terminal Count - TC(3)
Bit(25:24):	Timer Counter 4 Terminal Count - TC(4)
Bit(27:26):	Timer Counter 5 Terminal Count - TC(5)

2.2.2.3 Interrupt Status Register (Read/Write)

The interrupt status register reflects the status of all fourteen interrupt request signals after the masking bits have been applied. A logic '1' in a bit position indicates and interrupt request from the associated source.

Writing to the Interrupt Status Register with a '1' in the corresponding bit position will clear the associated interrupt request bit.

All fourteen interrupt request bits are logically OR'ed together to generate the interrupt to the PCI core. This global interrupt, INTA, can be disabled and manipulated using the PCI cores interrupt support functions (see Actel PCI data sheet).

2.2.3 Output Control Register (Write Only)

All output drivers power up in the high impedance. This active or high impedance state is also controlled by Bit(6) in this control register as follows:

Bit(6): '1' = Outputs active, '0' = Outputs are high impedance.

Digital output signals OUTPUT(5:0) are multifunction outputs. Each bit can be mapped either as a digital output or as an associated counter timer terminal count (TC) output.

This function multiplexing is defined by six control bits in this control register as follows:

Bit(0): '1' = TC(0), '0' = Output(0)
Bit(2): '1' = TC(1), '0' = Output(1)
Bit(3): '1' = TC(2), '0' = Output(2)
Bit(4): '1' = TC(3), '0' = Output(3)
Bit(5): '1' = TC(4), '0' = Output(4)

2.2.4 Output Register (Read/Write)

This twenty four bit register provides one bit for each digital output. The bits are mapped as follows:

Bit(0): Output(0)
Bit(1): Output(1)
:
:
Bit(23): Output(23).

A logical '1' equates to + 5V on the output driver.

A logical '0' equates to + 0V on the output driver.

This register operates independently of the output control register.

2.2.5 Input Register (Read only)

This twenty four bit register provides the input status of the twenty four digital input signals as follows:

Bit(0): Input(0)
Bit(1): Input(1)
:
:
Bit(23): Input(23).

A logical '1' equates to < 1.8V at the input receiver. NOTE THE BIT INVERSION.

A logical '0' equates to > 2.5V at the input receiver.

2.2.6 EEPROM Control Register (Read/Write) Offset 0x00b0

A four bit register used by the host to control access to the EEPROM. This four bit register is mapped to the 93LC46B EEPROM as per the following:

Bit 0: Mapped to the EEPROM CS (Chip Select) pin. Must be high to access the device. Defaults to '0' on reset. This bit can be written to and read back by the host.

Bit 1: Mapped to the EEPROM CLK (Clock). Defaults to '0' on reset. This bit can be written to and read back by the host.

Bit 2: Mapped to the EEPROM DI (Data In). Defaults to '0' on reset. This bit can be written to and read back by the host.

Bit 3: Mapped to the EEPROM DO (Data Out). This bit is read only.

2.3 Counter Operating Modes

The counters are 82C54 mode compatible with the following noted differences:

1. Each counter is 24 bits wide. There is this no need to manipulate high/low bytes or issue “latch count” commands.

2. Each counter actually always clocks synchronously with the internal 40 Mhz clock irrespective of the clock source chosen. For external clock sources, the external source is synchronised to the 40 Mhz internal clock, the rising edges detected and the counters clocked down at each edge detection. Synchronisation jitter is removed from terminal clock (TC) output of each counter by re-clocking the TC output with the actual rising edge of the source clock.

3. All counters clock on the rising edge of the clock source.

4. External GATE signals are also synchronised to the rising edge of the 40 Mhz internal clock. As such these signals should meet a 40 ns setup time prior to the rising edge of it’s clock source to ensure that it’s effect is visible on the same clock edge.

5. Because of the synchronisation/de-synchronisation nature of the design, there is an additional one clock period latency between the counter condition and the terminal count (TC) output when compared to the 82C54. Note that this DOES NOT effect the period count of any repetitive output but merely the delay from the setup condition to the first TC effect.

2.3.1 Mode 0 – Interrupt on terminal count.

Mode 0 operation is shown in Figure 2.

TC will be initialised to ‘0’ two clocks after the counter is loaded with an initial count. TC will toggle to a ‘1’ one clock after the counter has reached zero. This state is maintained until the initial count is re-loaded.

Gate = ‘1’ enables counting. Gate = ‘0’ disable counting.

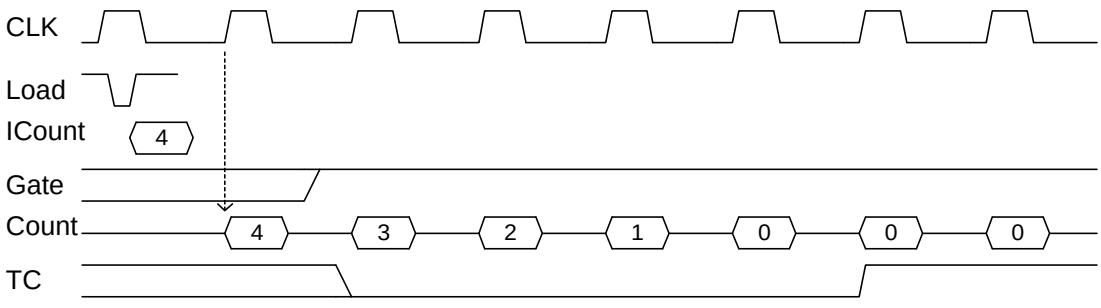

Figure 2 Interrupt on Terminal Count

Only the rising edge of Gate is significant.

2.3.2 Mode 1 – Hardware re-triggerable one-shot

Mode 1 operation is shown in Figure 3.

The rising edge of GATE reloads the counter with the initial count, initialises TC to '1' and starts the down-count sequence. Further rising edges of GATE will re-initialise this state.

TC will toggle to '0' whenever the counter reaches the count of two. This state is maintained until a new GATE trigger event is detected.

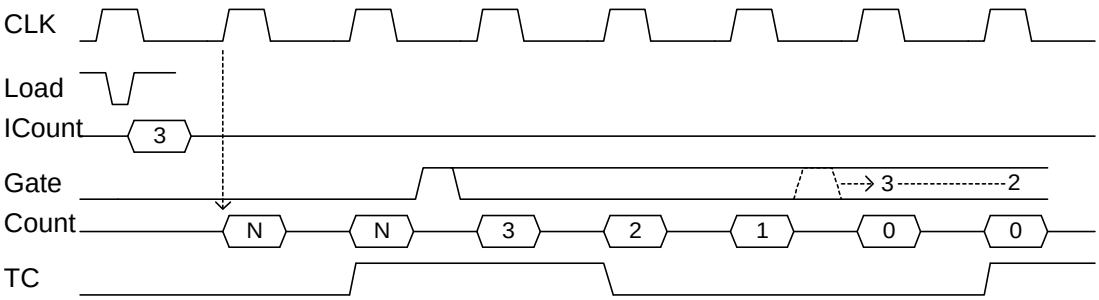

Figure 3 Hardware Re-triggerable One-Shot

2.3.3 Mode 2 – Rate Generator

Mode 2 operation is shown in Figure 4.

TC will be initialised to '1' two clocks after the counter is loaded with an initial count and the counter enabled to count down(GATE = '1'). On the clock following the count of ONE, the counter will be reloaded with the initial count and TC toggled to a '0'. TC will toggle back to a '1' on the next clock. This sequence is maintained.

Gate = '1' enables counting. Gate = '0' disable counting.

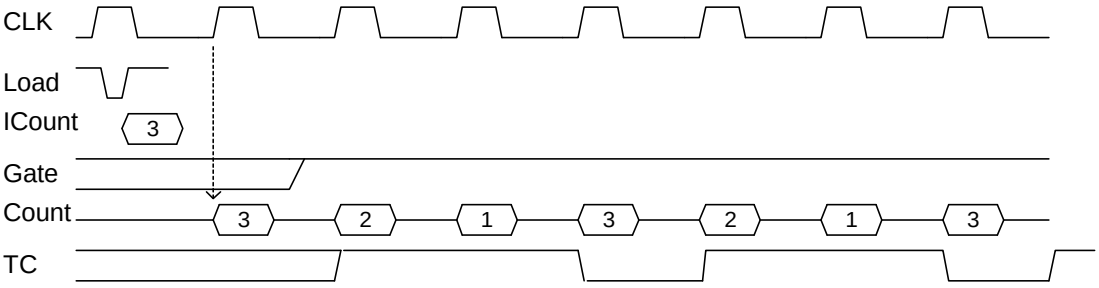

Figure 4 Rate Generator

2.3.4 Mode 3 – Square Wave Generator

Mode 3 operation is shown Figure 5.

This is the similar to mode 2 except that TC has a 50% duty cycle signal.

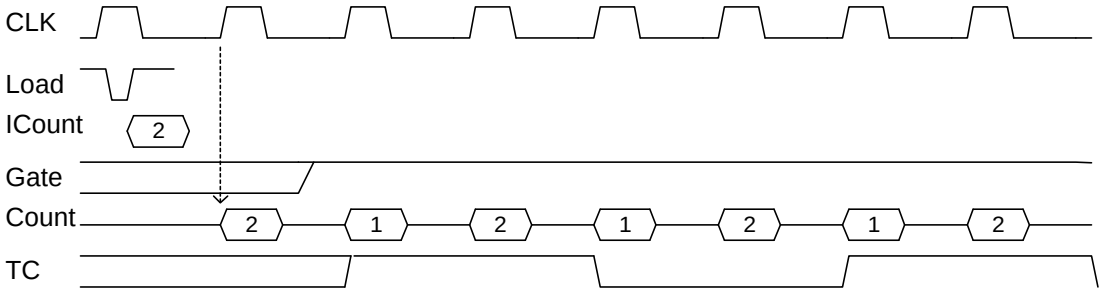

Figure 5 Square Wave Generator

2.3.5 Mode 4 – Software Triggered Strobe

Mode 4 operation is shown

Figure 6.

TC and the counter are initialised whenever the software writes the initial count register. TC will pulse low for one clock period after the counter has reached zero. Note that is sequence is re-triggerable if the initial count is written before the terminal count condition is reached.

Gate = ‘1’ enables counting. Gate = ‘0’ disable counting.

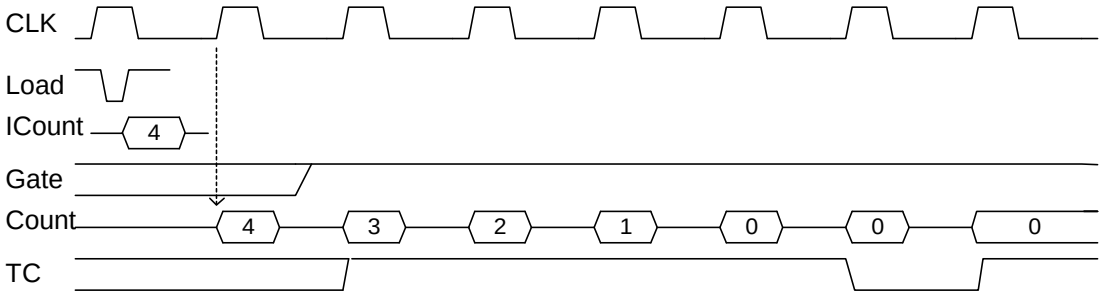

Figure 6 Software Triggered Strobe

2.3.6 Mode 5 – Hardware Triggered Strobe

Mode 5 operation is shown Figure 7.

Similar to mode four with the exception that the rising edge of GATE is used to re-trigger the initial counter and TC conditions.

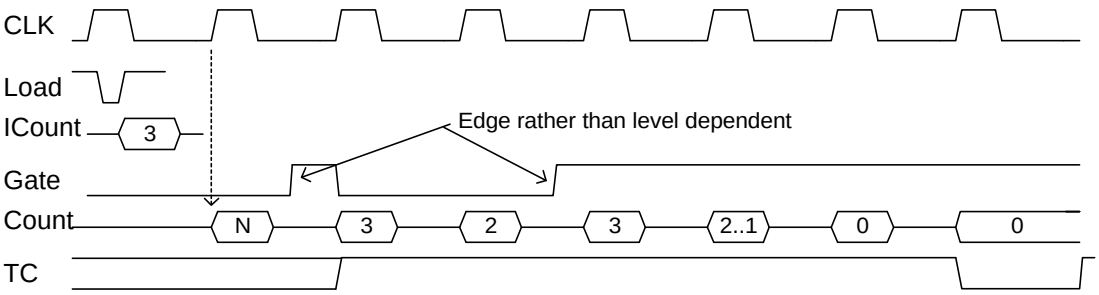

Figure 7 Hardware Triggered Strobe

2.3.7 Minimum Initial Counter Limits

The minimum initial counter values are mode dependent and defined in Table 3

Mode	Minimum initial count value
0	1
1	1
2	2
3	2
4	1
5	1

Table 3 Mode and Initial Count Limits

3. I/O Connector Pin-Out and Definition

Table 4 Defines the I/O connector pin-out and signal definition.

Name	Pin Number	Definition
INPUT_1	36	Digital Input #1
INPUT_2	2	Digital Input #2
INPUT_3	37	Digital Input #3
INPUT_4	3	Digital Input #4
INPUT_5	38	Digital Input #5
INPUT_6	4	Digital Input #6
INPUT_7	39	Digital Input #7
INPUT_8	5	Digital Input #8
INPUT_9	40	Digital Input #9
INPUT_10	6	Digital Input #10
INPUT_11	41	Digital Input #11
INPUT_12	7	Digital Input #12
INPUT_13	42	Digital Input #13
INPUT_14	8	Digital Input #14
INPUT_15	43	Digital Input #15
INPUT_16	9	Digital Input #16
INPUT_17	44	Digital Input #17
INPUT_18	10	Digital Input #18
INPUT_19	45	Digital Input #19
INPUT_20	11	Digital Input #20
INPUT_21	46	Digital Input #21
INPUT_22	12	Digital Input #22
INPUT_23	47	Digital Input #23
INPUT_24	13	Digital Input #24
		(Note: For Option C, Outputs 3, 4, 5, 6 are not multiplexed)
OUTPUT_1 OR TC_0	22	Digital Output #1 or Multiplexed with Counter #0 TC output
OUTPUT_2 OR TC_1	56	Digital Output #2 or Multiplexed with Counter #1 TC output
OUTPUT_3 OR TC_2	23	Digital Output #3 or Multiplexed with Counter #2 TC output
OUTPUT_4 OR TC_3	57	Digital Output #4 or Multiplexed with Counter #3 TC output
OUTPUT_5 OR TC_4	24	Digital Output #5 or Multiplexed with Counter #4 TC output
OUTPUT_6 OR TC_5	58	Digital Output #6 or Multiplexed with Counter #5 TC output
OUTPUT_7	25	Digital Output #7
OUTPUT_8	59	Digital Output #8

Name	Pin Number	Definition
OUTPUT_9	26	Digital Output #9
OUTPUT_10	60	Digital Output #10
OUTPUT_11	27	Digital Output #11
OUTPUT_12	61	Digital Output #12
OUTPUT_13	28	Digital Output #13
OUTPUT_14	62	Digital Output #14
OUTPUT_15	29	Digital Output #15
OUTPUT_16	63	Digital Output #16
OUTPUT_17	30	Digital Output #17
OUTPUT_18	64	Digital Output #18
OUTPUT_19	31	Digital Output #19
OUTPUT_20	65	Digital Output #20
OUTPUT_21	32	Digital Output #21
OUTPUT_22	66	Digital Output #22
OUTPUT_23	33	Digital Output #23
OUTPUT_24	67	Digital Output #24
CNTR0_CLK	15	External Clock for Counter 0
CNTR1_CLK	16	External Clock for Counter 1
CNTR2_CLK	17	External Clock for Counter 2 (Not used for Option C)
CNTR3_CLK	18	External Clock for Counter 3 (Not used for Option C)
CNTR4_CLK	19	External Clock for Counter 4 (Not used for Option C)
CNTR5_CLK	20	External Clock for Counter 5 (Not used for Option C)
CNTR0_GATE	49	External GATE for Counter 0
CNTR1_GATE	50	External GATE for Counter 1
CNTR2_GATE	51	External GATE for Counter 2 (Not used for Option C)
CNTR3_GATE	52	External GATE for Counter 3 (Not used for Option C)
CNTR4_GATE	53	External GATE for Counter 4 (Not used for Option C)
CNTR5_GATE	54	External GATE for Counter 5 (Not used for Option C)
+5V_F	1 , 35	+5V Fused (200 mA)
DGND	14 , 48 34 , 68	Digital Ground

Table 4 I/O Connector Pin-Out and Definition

4. I/O Electrical Specifications

SPECIFICATION	PCI-14 B	PCI-14 C
Digital Inputs		
Minimum input voltage (Relative to DGND) to register a logic '1'	+ 2.5 V	+2.5 V
Maximum input voltage (Relative to DGND) to register a logic '0'	+ 1.0 V	+1.0 V
Maximum Input Frequency	8 MHz	8 MHz
Maximum Continuous Input Voltage (Relative to DGND)	± 32 V	± 32 V
Maximum Input Voltage Spike < 100 ms (Relative to DGND)	± 80 V	± 80 V
Maximum Input Voltage Spike < 100 ms (Relative to DGND)	± 80 V	± 80 V
Counter Clock and Gate Control Inputs		
Minimum input voltage (Relative to DGND) to register a logic '1'	+ 2.5 V	+2.5 V
Maximum input voltage (Relative to DGND) to register a logic '0'	+ 1.0 V	+1.0 V
Maximum Input Frequency	8 MHz	8 MHz
Maximum Continuous Input Voltage (Relative to DGND)	± 32 V	± 32 V
Maximum Input Voltage Spike < 50 ms (Relative to DGND)	± 80 V	± 80 V
Maximum Input Voltage Spike < 50 ms (Relative to DGND)	± 80 V	± 80 V
Digital Outputs & Counter Timer Outputs		
Number of Digital Outputs (Multiplexed with counter TC outputs.)	24	24
Sink current (Output voltage =< 0.5V)	-48 mA	-48 mA
Source current (Output voltage >= 2.5V)	+18 mA	+18 mA
Maximum Output Frequency	8 MHz	8 MHz
Short Circuit protection	-40 to -140 mA	-40 to –140 mA
Maximum Continuous Over Voltage Stress (Note 1)	+ 32 V	+ 5.5 V
Maximum Continuous Under Voltage Stress (Note 1)	- 32 V	- 0. 8 V
Maximum Output Voltage Spike < 50 ms (Relative to DGND)	± 80 V	-

Note 1. For Option B, the outputs are protected by 100 mA ± 20 mA (at 25 °) polyfuses and 5.6V transorbs. Over or under voltage stress levels longer than 50 ms will activate the fuse protecting the driver. Note also that once activated such fuses have a fairly long recovery time.