PC104-30H

PC104 DAQ Boards
User's Manual for
PC104-30H Analog Input Board

Eagle Technology – Cape Town, South Africa
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Analog Input Boards

Data Acquisition and Process Control

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1. Introduction

The PC104-30H is single channel high-speed analog input board. It has a PC104 bus architecture and has a 12-bit resolution.

Features

- 16-bit PC104/ISA bus compatible.
- 12-bit ADC single channel.
- 833 KHz sampling speed.
- High accuracy and low noise.
- Fully programmable DMA and interrupt system.

Applications

The PC104-30H can be used in the following applications:

- Automation test equipment.
- Vibration monitoring.
- Plant/Factory process control.
- Remote sensing.

Key Specifications

- 833 KHz @ 12-bits
- Data transfer via Slave DMA, interrupts or polled I/O.

Software Support

The PC104-30H is supported by EDR Enhanced and comes with an extensive range of examples. The software will help you to get your hardware going very quickly. It also makes it easy to develop complicated control applications. All operating system drivers, utility and test software are supplied on the EDR Enhanced CD-Rom. The latest drivers can also be downloaded from the Eagle Technology website. For further support information see the Contact Details section.

Contact Details

Below are the contact details of Eagle Technology.

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2. Installation

This chapter describes how to install and configure the PC104-30H for the first time. Minimal configuration is necessary; almost all settings are done through software. The base address needs to be set before first time operation.

Package

PCI104-30H package will contain the following:

- PCI104-30H PC104 based board
- Eagle Technology Software CD-Rom.

Operating System Support

The PCI104-30H series support the Windows NT and Windows Driver Models (WDM) driver types. The operating systems are listed in the table below.

Board Type	Revision	Operating Systems	Driver Type
PC104-30H	Revision 1	Windows NT/2000/98/ME	NT Sys, WDM PnP

Table 2-1 Operating System Support

Hardware Installation

This section will describe how to install your PCI board into your computer.

- Switch off the computer and disconnect from power socket.

Failure to disconnect all power cables can result in hazardous conditions, as there may be dangerous voltage levels present in externally connected cables.

- Remove the cover of the PC.
- Choose any open PCI slot and insert PCI board
- Insert bracket screw and ensure that the board sits firmly in the PCI socket.
- Replace the cover of the PC.
- Reconnect all power cables and switch the power on.
- The hardware installation is now completed.

Jumper Settings – (I/O Base Address)

The table below shows all possible jumper settings. The jumper is located on LK2.

LK3	LK2	LK1	Description
IN	IN	IN	0x0C00 -> 0x0FFF
IN	IN	OUT	0x1C00 -> 0x1FFF
IN	OUT	IN	0x2C00 -> 0x2FFF
IN	OUT	OUT	0x3C00 -> 0x3FFF
OUT	IN	IN	0x4C00 -> 0x4FFF
OUT	IN	OUT	0x5C00 -> 0x5FFF
OUT	OUT	IN	0x6C00 -> 0x6FFF
OUT	OUT	OUT	0x7C00 -> 0x7FFF

Table 2-2 Jumper Settings

Software Installation

Windows 98/2000/ME

Installing the Windows 98/2000 device driver is a very straightforward task. The board does support plug and play so Windows needs to be told that a new device was installed. The *Add New Hardware Wizard* will be used for this task.
Click ***Start-> Settings-> Control Panel-> Add New/Remove Hardware***.

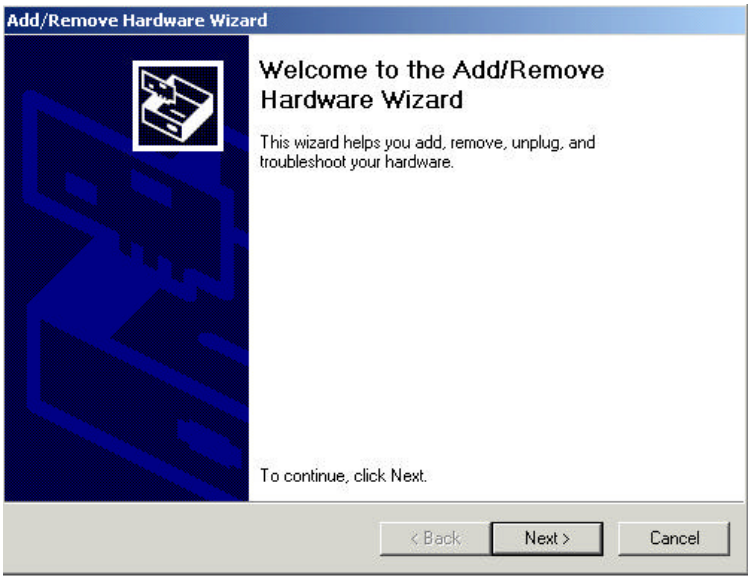

Figure 2-1 Step 1

Select *Add a device.*

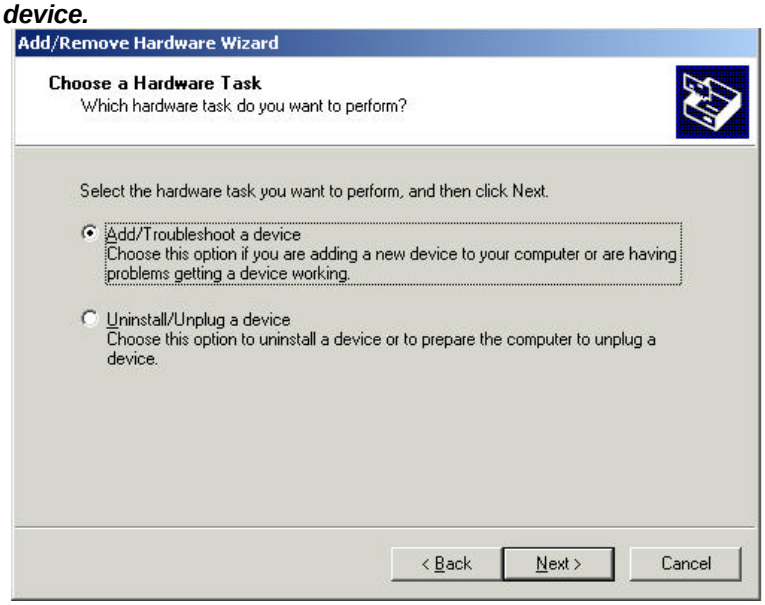

Figure 2-2 Step 2

Select *Add a new device.*

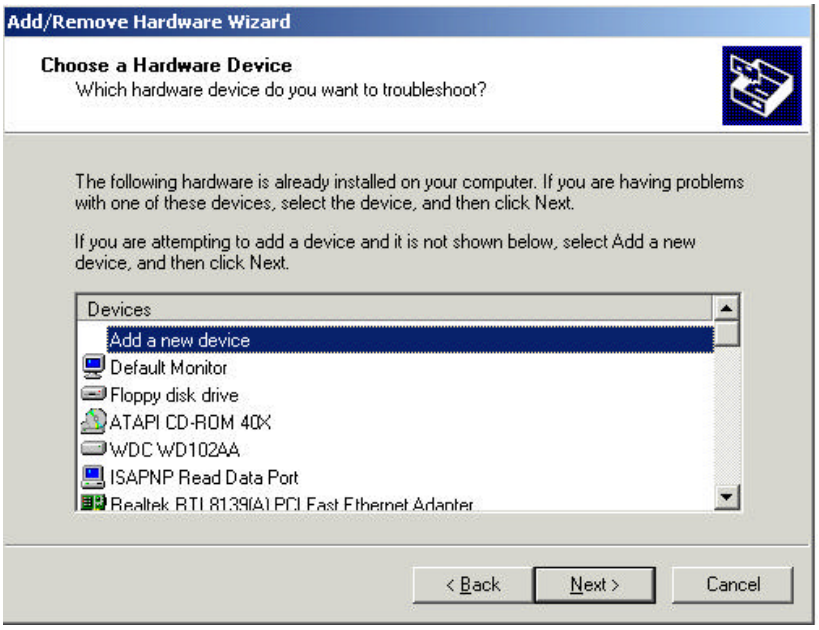

Figure 2-3 Step 3

Select *No, I want to select the hardware from a list*

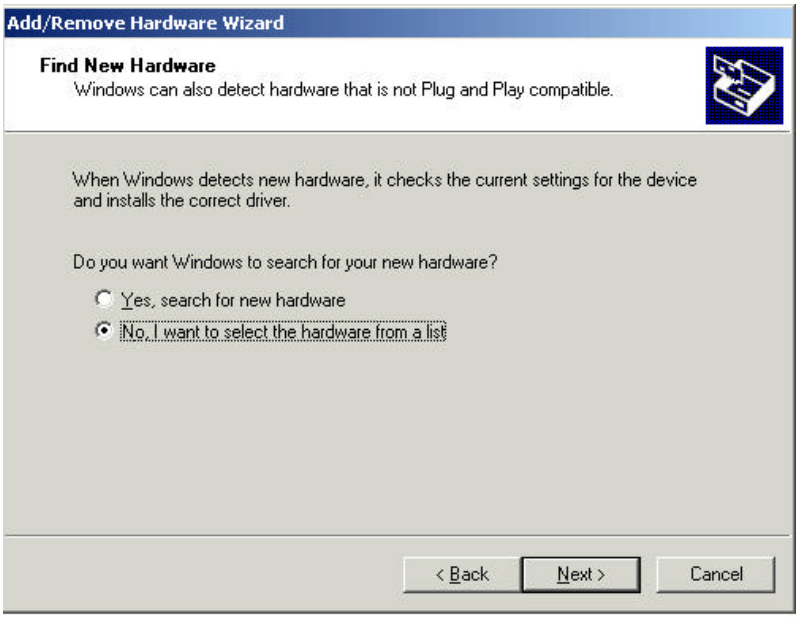

Figure 2-4 Step 4

Select *Other Device or Eagle Data Acquisition* if it exists.

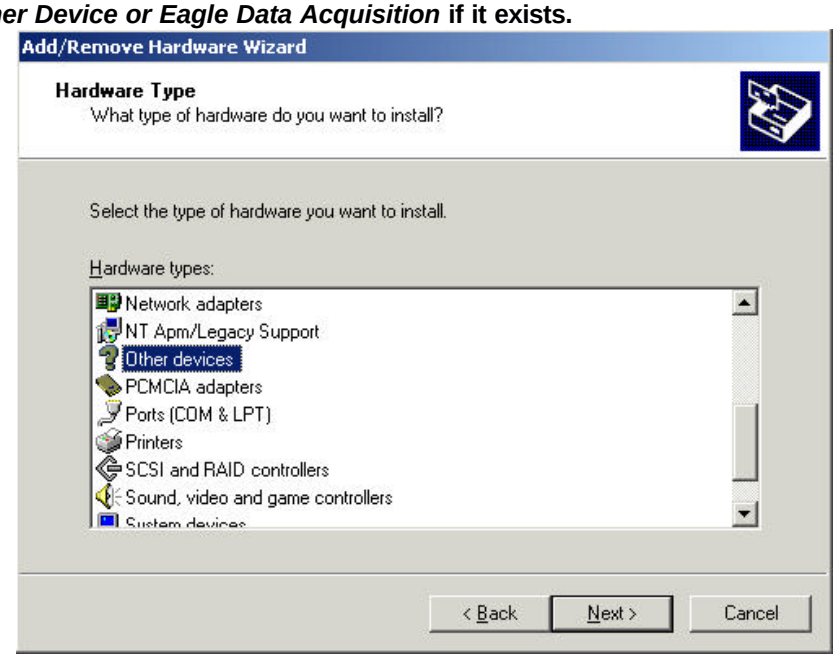

Figure 2-5 Step 5

Select *Have Disk.*

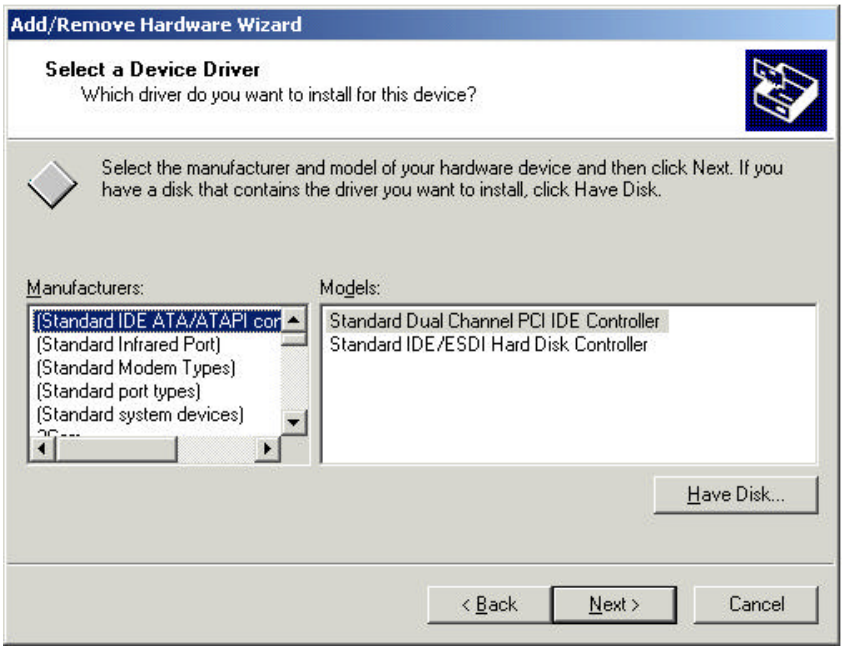

Figure 2-6 Step 6

Use the browse dialog to search for the file *pc10430h.inf.*

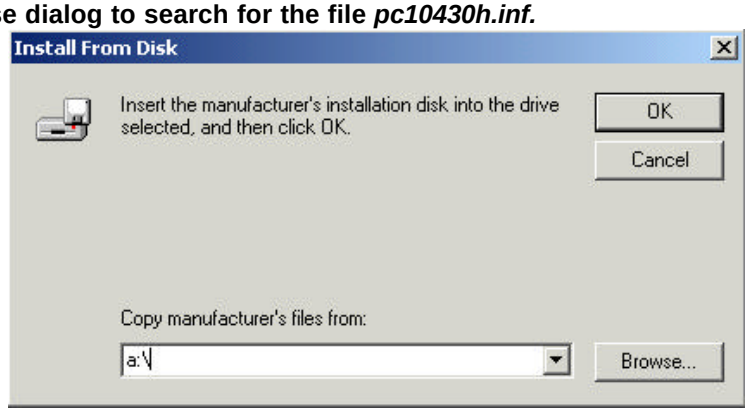

Figure 2-7 Step 7

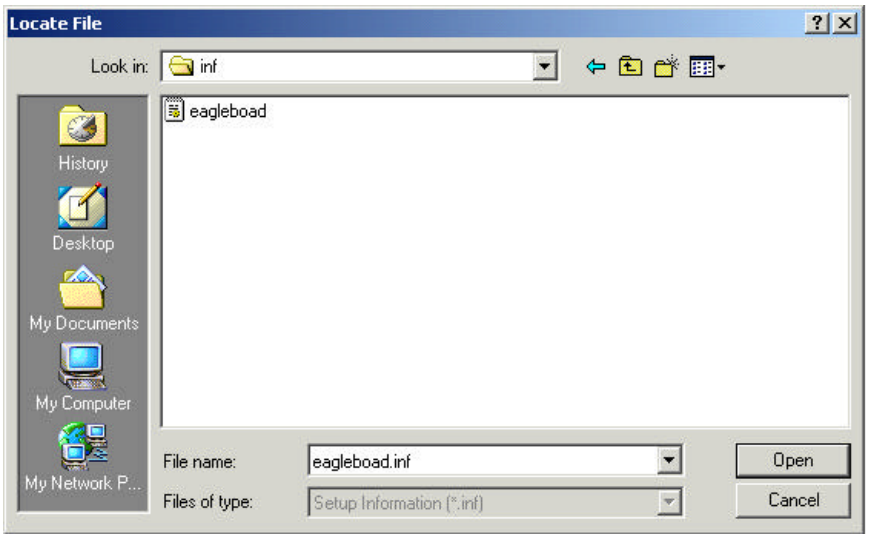

Figure 2-8 Step 8

The next dialog will display the model name of the board you are trying to install.

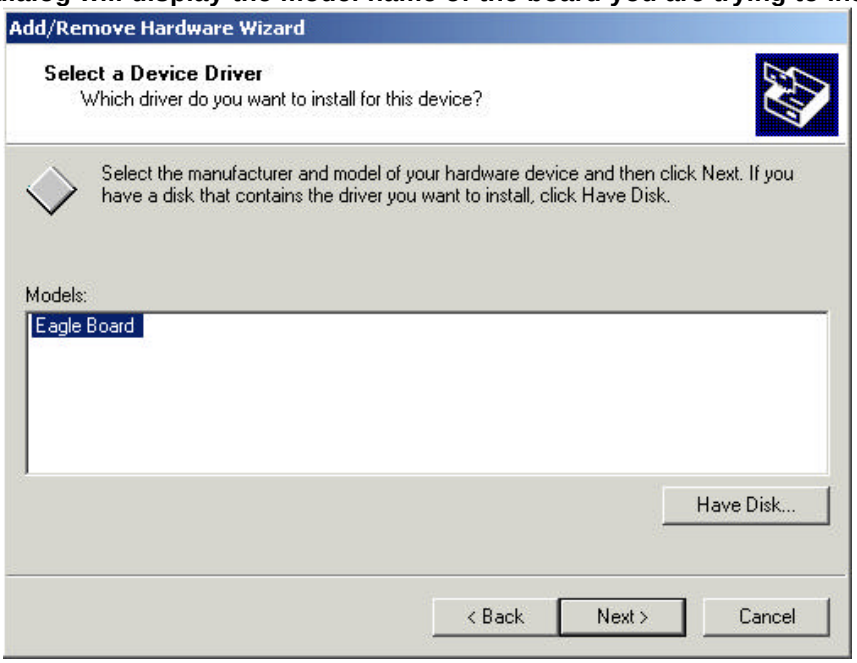

Figure 2-9 Step 9

Select the *Next* button.

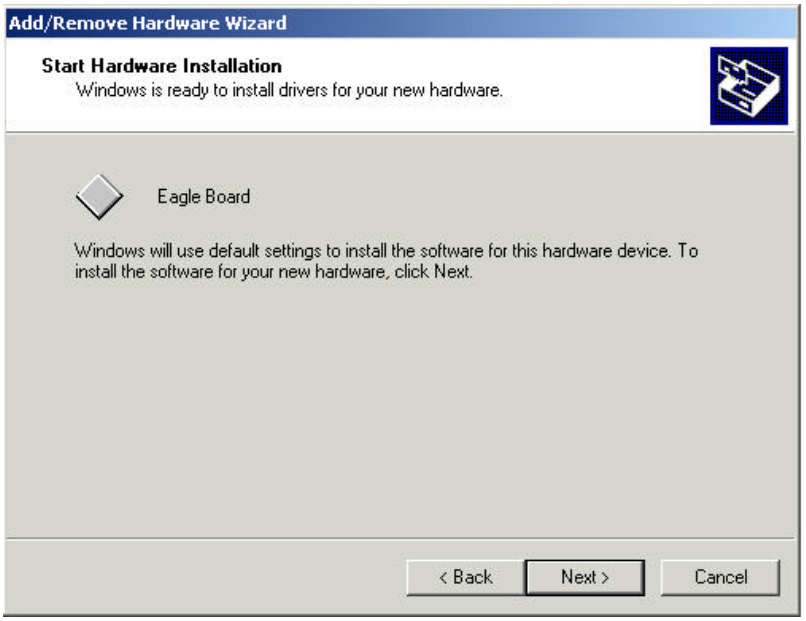

Figure 2-10 Step 10

Select the *Finish* button to complete the installation.

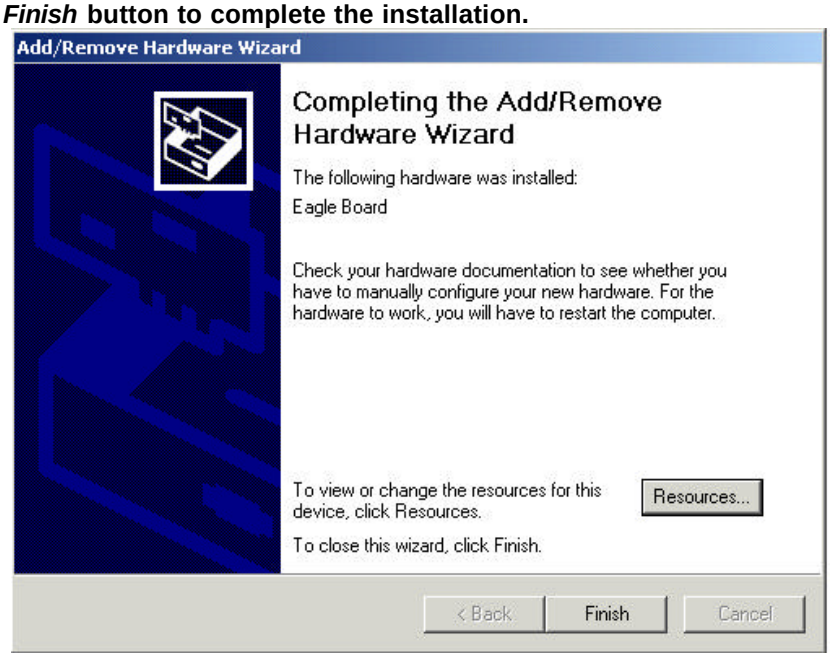

Figure 2-11 Step 11

Post installation

When done with the driver installation the device manager can be open to make sure the installation was a success.

- First make sure that the driver is working properly by opening the *Device Manager*.
- Check under the Eagle Data Acquisition list if your board is listed and working properly. The picture below shows a typical board that is installed.

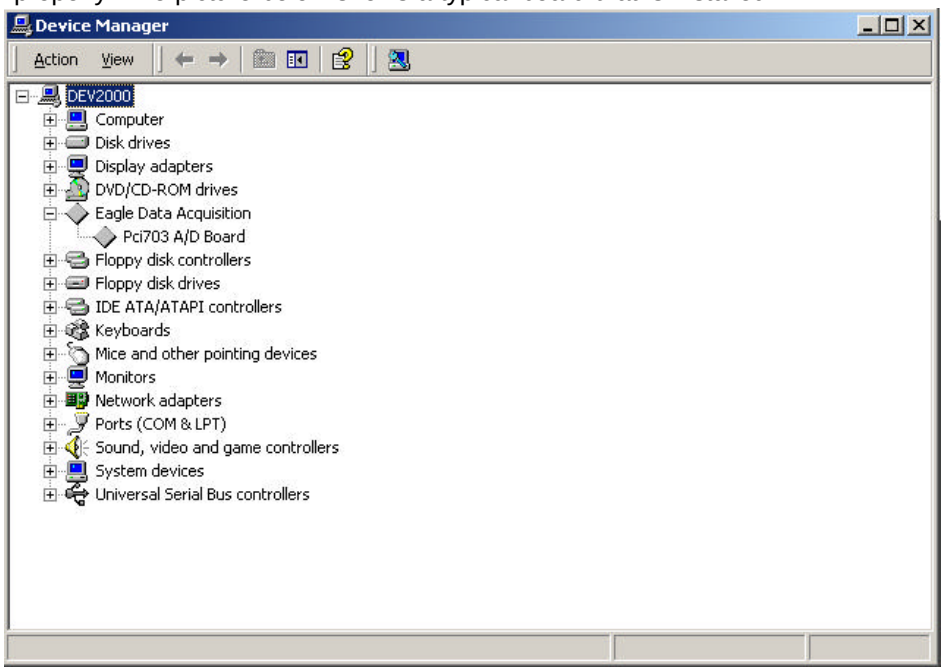

Figure 2-12 Device Manager

- Clearly you can see that the PCI device is listed and working properly.
- Further open the control panel and then the *EagleDAQ* folder. This dialog should list all installed hardware. Verify your board's properties on this dialog. See picture below

Figure 2-13 EAGLE DAQ Dialog

Now the first part of your installation has been completed and ready to install the EDR Enhanced Software Development Kit.

- Run ***edreapi.exe*** found on the Eagle CD-Rom and follow the on screen instructions

Windows NT

The Windows NT driver supports both Windows NT4.0 and Windows 2000. It does not require any special setup. To install the Windows NT drivers simply run ***edrewinnt.exe*** on the Eagle CD-Rom. This will automatically install the device drivers. Restart your computer when done. Open the *EagleDAQ* folder in the control panel to check if your installation was successful.

If you are running on Windows 2000 and it detects a new device simply install a default driver, or so called placeholder. This will disable the device in the plug and play manager. The NT driver will take control of the device.

Changing your resources

The plug and play manager manages the board's resources. To change a resource settings simply open the device manager and select the device. Select the properties and then the resource TAB of the properties dialog. Now you can change the settings. The picture below shows the resources of a typical device.

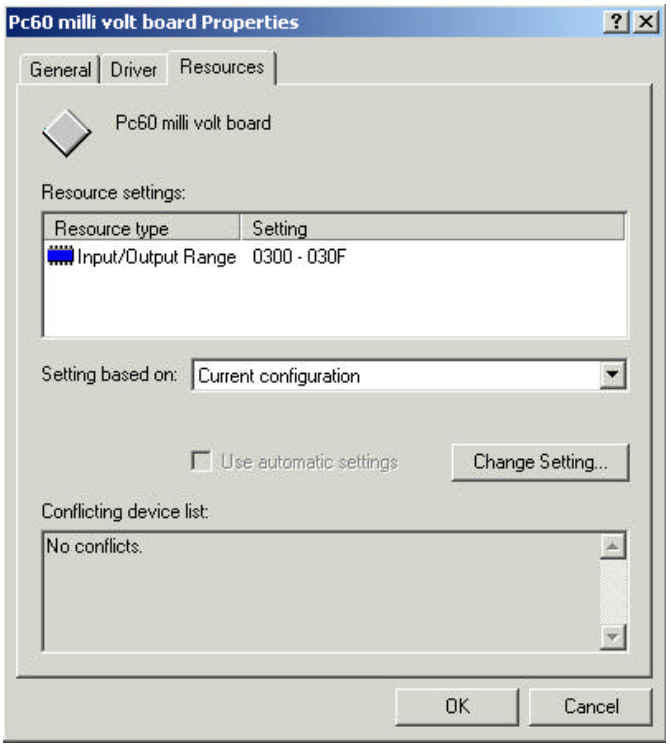

Figure 2-14 Device Properties

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3. Architecture

The PC104-30H is PC104/ISA based and has an analog input subsystem. The board has an onboard clock and a scaler. The scaler is used to select an appropriate sampling frequency. Two sampling mode is supported, timer triggered and programmed I/O. The PC104-30H has a 16K x 12-bit FIFO implement in a SRAM. Interrupt and DMA channel selection are done via software. Interrupts can be generate from FIFO not empty, a programmable FIFO water level and DMA done.

Register Structure

OFFSET (HEX 16-bit)	Name	Description	Access
0x0000	CONFIG	System configuration register	W
0x0002	STATUS	Status register	R/W
0x0004	WATER_LEVEL	Interrupt water level register	W
0x0006	FIFO_DATA	FIFO data register	R/W
0x0008	FIFO_CLEAR	FIFO control register	W
0x000A	CONTROL	System control register	W
0x000C	CONVERT	ADC convert register	W
0x000E	COUNT	FIFO count register	R

Table 3-1 Pc104-30H Register Structure

Register Descriptions

CONFIG Register (0x0000)

BIT	Name	Description
<1:0>	INT_CONFIG	Select the interrupt level 00: IRQ10 01: IRQ11 10: IRQ12 11: IRQ14
<2>	NE_INT_EN	Not empty interrupt enable. This will generate an interrupt when the FIFO is not empty. 1: Enable 0: Disable
<3>	WL_INT_EN	Water level interrupt enable. This will enable the an interrupt on condition where the FIFO level is one more than the water level 1: Enable 0: Disable
<5:4>	DMA_CONFIG	Select the DMA channel 00: DRQ5 01: DRQ6 1X: DRQ7
<6>	DMA_EN	0: DMA disable

<7>	DMA_INTR_EN	1: DMA enabled Enables the TC (terminal count) interrupt from the ISA bus to generate an interrupt. 0: DMA TC interrupt disabled 1: DMA TC interrupt enabled

Table 3-2 CONFIG Register

STATUS Register (0x0002)

BIT	Name	Description
<0>	FIFO_NE	FIFO not empty status 0: Empty
<1>	WATER_LEVEL	Status on water level 1: At least one more sample in FIFO than water level. 0: FIFO below or equal to water level 1: FIFO above water level
<2>	FIFO_NE_IRQ	Set whenever an interrupt is pending on FIFO not empty.
<3>	WATER_LEVEL_IRQ	Set whenever an interrupt is pending on the water level.
<4>	EEPROM_CS	EEPROM chip select
<5>	EEPROM_DI	EEPROM data input
<6>	EEPROM_CLK	EEPROM clock
<7>	EEPROM_DO	EEPROM data output
<8>	DMA_TC_FLAG	Set whenever ISA TC is reached. This needs to be reset via software by writing a 0.
<9>	DMA_TC_IRQ	Set whenever DMA_TC_FLAG is set and DMA_INTR_EN is set.

Table 3-3 STATUS Register

WATER_LEVEL Register (0x0004)

BIT	Name	Description
<11:0>	WATER_LEVEL	This register is used to program an interrupt level for the FIFO. As soon as there is one more sample in the FIFO than the waterlevel, the FIFO_WATER_LEVEL flag will be set.

Table 3-4 WATER_LEVEL Register

FIFO_DATA Register (0x0006)

BIT	Name	Description
<11:0>	FIFO_DATA	This register is used to access the ADC FIFO.

Table 3-5 FIFO_DATA Register

FIFO_CLEAR Register (0x0008)

BIT	Name	Description
<0>	FIFO_CLEAR	Writing to this register reset the FIFO pointers. This does not stop the ADC process.

Table 3-6 FIFO_CLEAR Register

CONTROL Register (0x000A)

BIT	Name	Description
<0>	AD_ENABLE	Controls the ADC process. 0: Disabled 1: Enabled
<1>	AD_MODE	Set the trigger mode. 0: Trigger is programmed I/O 1: Trigger is timer events

Table 3-7 CONTROL Register

CONVERT Register (0x000C)

BIT	Name	Description
<0>	CONVERT	Writing to this register triggers a programmed I/O conversion. The MODE must be 0 for this.

Table 3-8 CONTROL Register

COUNT Register (0x000E)

BIT	Name	Description
<11:0>	COUNT	Supplies the bottom 12 bits of the 14-bit FIFO count register.

Table 3-9 COUNT Register

Programming Examples

Programmed I/O and Single Read

1. Reset FIFO and flags.
2. Set mode to 0 (programmed I/O) and enabled ADC.
3. Write to CONVERT register.
4. Wait until the FIFO flag get set.
5. Read data from FIFO_DATA register.
6. Loop to 3

Programmed I/O and Burst Data

1. Reset FIFO and flags.
2. Program water level to 4096 (4K).
3. Set clock to 400 KHz.
4. Set mode to 1(timer triggered) and enable ADC.
5. Wait for water level flag to be set.
6. Read 4096 samples from FIFO.
7. Disable ADC process.

DMA/Interrupt and Burst Data

1. Reset FIFO and flags.
2. Program water level to 4096 (4K).
3. Set clock to 400 KHz.
4. Enable water level interrupt
5. Set mode to 1 (timer triggered) and enable ADC.
6. Wait for interrupt.
7. Disable ADC process
8. Program PC-DMA controller to transfer 4K samples.
9. Enable TC interrupt and enable DMA process.
10. Wait for TC interrupt
11. Disable all interrupts

4. Interconnections

The PC104-30H has one connector used to interface to the analog input system. It is a 3-pin header containing a pin for analog ground and a pair of pins for a differential channel.

Pin Assignments

Pin	Name	Description
1	AIN -	Analog input negative.
2	AGND	Analog ground.
3	AIN +	Analog input positive.

Table 4-1 PC104-30H - 3 PIN HEADER(M)

Pin Descriptions

AIN +

This is the positive input of the board's analog channel.

AGND

This line connects to analog ground on the board.

AIN –

This is the negative input of the board's analog channel.

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5. Programming Guide

The PC104-30H is supplied with a complete software development kit. EDR Enhanced (EDRE SDK) comes with drivers for many operating systems and a common application program interface (API). The API also serves as a hardware abstraction layer (HAL) between the control application and the hardware. The EDRE API makes it possible to write an application that can be used on all hardware with common sub-systems.

The PC104-30H can also be programmed at register level, but it is not recommended. A detailed knowledge of the PC104-30H is needed and some knowledge about programming ISA devices. We recommend that you only make use of the software provided by Eagle Technology.

EDR Enhanced API

The EDR Enhanced SDK comes with both ActiveX controls and a Windows DLL API. Examples are provided in many different languages and serve as tutorials. EDRE is also supplied with a software manual and user's guide.

The EDRE API hides the complexity of the hardware and makes it really easy to program the PCI800 board. It has got functions for each basic sub-system and is real easy to learn.

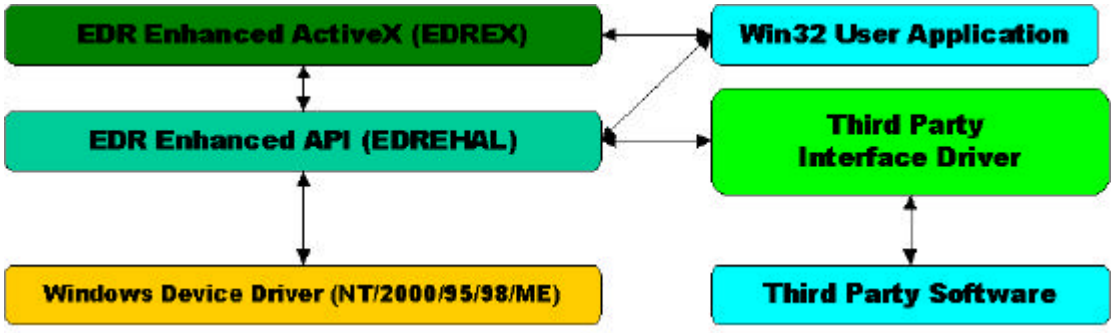


Figure 5-1 EDR Enhanced Design

Analog Input

The PC104-30H has only one analog input channel. It supports two mode, programmed I/O and timer triggered. The timer goes trough an 8-bit scaler fed by a 40MHz clock. The minimum scaler count is 47 or 833KHz and the maximum 255 or 156KHz.

Reading a single voltage from a channel

A single call is necessary to read the analog input.

API-CALL

Long EDRE_ADSingle (ulng Sn, ulng Channel, ulng Gain, ulng Range, plong uVoltage)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
Channel	Unsigned long	Ignored
Gain	Unsigned long	Ignored
Range	Unsigned long	Ignored
uVoltage	Pointer to a long	Voltage read from channel
Return	Long	Error Code

ACTIVEX CALL

Long EDREADX.SingleRead (long Channel)

Parameter	Type	Description
Channel	Long	ADC Channel
Return	Long	Error Code

Configuring the ADC subsystem for scanning

This is the most complicated part of configuring the PCI703 for auto scanning. Make sure that you use the correct format when applying the channel list configuration. There are many loopholes and care should be taken when implementing code to configure the PCI703.

API-CALL

Long EDRE_ADConfig (ulng Sn, pulng Freq, ulng ClkSrc, ulng Burst, ulng Range, pulng ChanList, pulng GainList, ulng ListSize)

The following parameters must be specified when configuring the ADC sub-system.

Parameter	Type	Description
Sn	Unsigned long	Board's serial number.
Freq	Pointer to an unsigned long	Sampling frequency. This is the 8-bit value for the scaler. The minimum is 47 or 833KHz. The maximum is 255 or 156KHz.
ClkSrc	Unsigned long	Ignored
Burst	Unsigned long	Ignored
Range	Unsigned long	Ignored
ChanList	Pointer to an unsigned long	Ignored
GainList	Pointer to an unsigned long	Ignored
ListSize	Unsigned long	Ignored

ACTIVEX CALL
Long EDREADX.Configure (plong Channels, plong Gains, long ListSize)

Parameter	Type	Description
Channels	Pointer to a long	Ignored
Gains	Pointer to a long	Ignored
ListSize	Unsigned long	Ignored

The *Frequency* and *ClockSource* ADC ActiveX control must be setup before calling the configure function.

EDREADX.Frequency

Frequency	Sampling frequency. This is the 8-bit value for the scaler. The minimum is 47 or 833KHz. The maximum is 255 or 156KHz.

EDREADX.ClockSource

ClockSource	Ignored

Starting and Stopping the ADC process

A single call is necessary to start or stop the ADC process

API-CALL
Long EDRE_ADStart (ulng Sn)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
Return	Long	Error Code

ACTIVEX CALL
Long EDREADX.Start ()

Parameter	Type	Description
Return	Long	Error Code

API-CALL
Long EDRE_ADStop (ulng Sn)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
Return	Long	Error Code

ACTIVEX CALL
Long EDREADX.Stop ()

Parameter	Type	Description
Return	Long	Error Code

Getting data from the driver buffer

A single call is necessary copy data from the driver buffer to the user buffer.

API-CALL
Long EDRE_ADGetDatat (ulng Sn, plong Buf, pulng BufSize)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
Buf	Pointer to a long buffer.	Buffer to copy micro voltages too.
BufSize	Pointer to an unsigned long	Size of buffer must be passed or number of samples requested. The returned value will indicate the number of actual samples copied to the buffer.
Return	Long	Error Code

ACTIVEX CALL
Long EDREADX.Start (plong Buffer, plong Size)

Parameter	Type	Description
Buf	Pointer to a long buffer.	Buffer to copy micro voltages too.
BufSize	Pointer to a long	Size of buffer must be passed or number of samples requested. The returned value will indicate the number of actual samples copied to the buffer.
Return	Long	Error Code

Querying the ADC subsystem

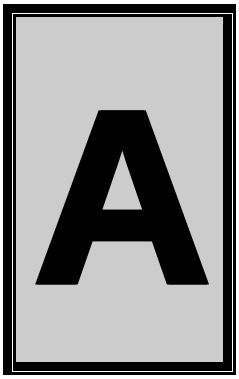
The driver can be queried to check the status of the ADC subsystem. The number of unread samples is one example.

API-CALL
Long EDRE_Query (ulng Sn, ulng QueryCode, ulng Param)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
QueryCode	Unsigned long	Query code. See appendix Example: ADUNREAD: This will tell you the number of available samples. ADBUSY: Is the ADC subsystem busy?
Param	Unsigned long	Extra parameter.
Return	Long	Returned query code

ACTIVEX CALL
Long EDREADX.GetUnread ()

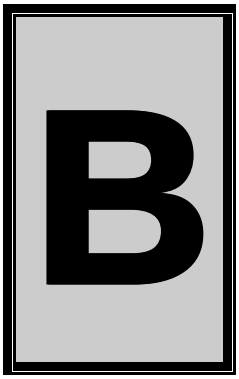
Parameter	Type	Description
Return	Long	Number of samples available in the driver.



A.Specifications

Hardware Characteristics

Number of Channels:	One
ADC Resolution:	12-bit
Input Voltage Range:	±5.0V Maximum
Input Bandwidth:	3MHz
Input Impedance:	Differential 24KΩ, Common Mode 18KΩ
Maximum Sampling Frequency:	833 KHz
Minimum Sampling Frequency:	156 KHz
Accuracy (after calibration):	±1 LSB
Power Consumption:	5V @ 100 mA maximum
PC104/ISA Clock Frequency:	8 MHz ±10%



B.Configuration Constants

Query Codes

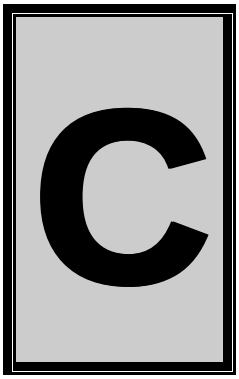
Name	Value	Description
APIMAJOR	1	Query EDRE API major version number.
APIMINOR	2	Query EDRE API minor version number.
APIBUILD	3	Query EDRE API build version number.
APIOS	4	Query EDRE API OS type.
APINUMDEV	5	Query number of devices installed.
BRDTYPE	10	Query a board's type.
BRDREV	11	Query a board's revision.
BRDYEAR	12	Query a board's manufactured year.
BRDMONTH	13	Query a board's manufactured month.
BRDDAY	14	Query a board's manufactured day.
BRDSERIALNO	15	Query a board's serial number.
DRVMAJOR	20	Query a driver's major version number.
DRVMINOR	21	Query a driver's minor version number.
DRVBUILD	22	Query a driver's build version number.
ADNUMCHAN	100	Query number of ADC channel.
ADNUMSH	101	Query number of samples-and-hold channels.
ADMAXFREQ	102	Query maximum sampling frequency.
ADBUSY	103	Check if ADC system is busy.
ADFIFOSIZE	104	Get ADC hardware FIFO size.
ADFIFOOVER	105	Check for FIFO overrun condition.
ADBUFFSIZE	106	Check software buffer size.
ADBUFFOVER	107	Check for circular buffer overrun.
ADBUFFALLOC	108	Check if software buffer is allocated.
ADUNREAD	109	Get number of samples available.
ADEXTCLK	110	Get status of external clock line – PCI30FG.
ADEXTTRIG	111	Get status of external trigger line – PCI30FG.
ADBURST	112	Check if burst mode is enabled.
ADRANGE	113	Get ADC range.
DANUMCHAN	200	Query number of DAC channels.
DAMAXFREQ	201	Query maximum DAC output frequency.
DABUSY	202	Check if DAC system is busy.
DAFIFOSZ	203	Get DAC FIFO size.
CTNUM	300	Query number of counter-timer channels.
CTBUSY	301	Check if counter-timer system is busy.
DIONUMPORT	400	Query number of digital I/O ports.
DIOQRYPORT	401	Query a specific port for capabilities.
DIOPORTWIDTH	402	Get a specific port's width.
INTNUMSRC	500	Query number of interrupts sources.
INTSTATUS	501	Queries interrupt system's status.
INTBUSCONNECT	502	Connect interrupt system to bus.
INTISAVAILABLE	503	Check if an interrupt is available.
INTNUMTRIG	504	Check number times interrupted

Error Codes

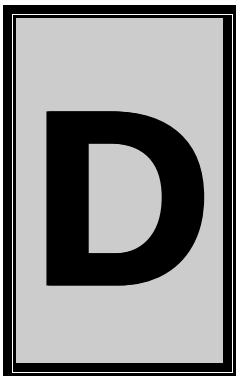
Name	Value	Description
EDRE_OK	0	Function successfully.
EDRE_FAIL	-1	Function call failed.
EDRE_BAD_FN	-2	Invalid function call.
EDRE_BAD_SN	-3	Invalid serial number.
EDRE_BAD_DEVICE	-4	Invalid device.
EDRE_BAD_OS	-5	Function not supported by operating system.
EDRE_EVENT_FAILED	-6	Wait on event failed.
EDRE_EVENT_TIMEOUT	-7	Event timed out.
EDRE_INT_SET	-8	Interrupt in use.
EDRE_DA_BAD_RANGE	-9	DAC value out of range.
EDRE_AD_BAD_CHANLIST	-10	Channel list size out of range.
EDRE_BAD_FREQUECY	-11	Frequency out of range.
EDRE_BAD_BUFFER_SIZE	-12	Data passed by buffer incorrectly sized
EDRE_BAD_PORT	-13	Port value out of range.
EDRE_BAD_PARAMETER	-14	Invalid parameter value specified.
EDRE_BUSY	-15	System busy.
EDRE_IO_FAIL	-16	IO call failed.
EDRE_BAD_ADGAIN	-17	ADC-gain out of range.
EDRE_BAD_QUERY	-18	Query value not supported.
EDRE_BAD_CHAN	-19	Channel number out of range.
EDRE_BAD_VALUE	-20	Configuration value specified out of range.
EDRE_BAD_CT	-21	Counter-timer channel out of range.
EDRE_BAD_CHANLIST	-22	Channel list invalid.
EDRE_BAD_CONFIG	-23	Configuration invalid.
EDRE_BAD_MODE	-24	Mode not valid.
EDRE_HW_ERROR	-25	Hardware error occurred.
EDRE_HW_BUSY	-26	Hardware busy.
EDRE_BAD_BUFFER	-27	Buffer invalid.
EDRE_REG_ERROR	-28	Registry error occurred.
EDRE_OUT_RES	-29	Out of resources.
EDRE_IO_PENDING	-30	Waiting on I/O completion

Digital I/O Codes

Name	Value	Description
DIOOUT	0	Port is an output.
DIOIN	1	Port is an input.
DIOINOROUT	2	Port can be configured as in or out.
DIOINANDOUT	3	Port is an input and an output.



C.Layout Diagram



D.Ordering Information

For ordering information please contact Eagle Technology directly or visit our website www.eagle.co.za. They can also be emailed at eagle@eagle.co.za.

Board	Description
PC104-30H	PC104 800 KHz analog input board.

Table D-1 Ordering Information