PC 62C

Enhanced IRQ 16 / 64 Channel Optically Isolated Input Card with Digital I/O

User's Manual

For the IBM AT, PS/2, 386, 486, Pentium, Pentium Pro, ISA and EISA computers

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Introduction

The PC 62C is an enhanced IRQ Optical Isolated Input Board for the IBM PC/XT/AT, 486, Pentuim, ISA and EISA Computers. It provides 16 / 64 Optically Isolated Inputs in either single ended or differential mode.

16 Digital Inputs and 16 Digital Outputs (with open collector outputs) are also provided on the PC62C.

The PC 62C fits into one of the IBM PC/AT, ISA, EISA expansion slot.

Typical applications

Industrial control
Process Control
Laboratory Automation
Energy management
Product testing

Key Features

- 16 channel Optically isolated inputs expandable to 48
- Background readback of Isolated Input lines via Interrupt Mode
- IRQ Mode via shared interrupts or individual interrupt lines
- Ideal Card for multitasking environments
- Status of isolated lines is only read when there is a state change in IRQ Mode
- Host CPU time kept to a minimum
- 16 Bit Reads/Writes supported to provide higher thruputs
- Interrupt selection IRQ2 thru IRQ15 can be automatically changed via software
- Isolated inputs can be fed directly into the IRQ Bus system or toggled via Global Register System
- Pin for Pin compatible with PC 62B Optically Isolated Input Card
- 450V RMS Min / 2kV Max Isolation Voltage
- Built-in Wait state generation for fast Bus clock speeds
- Frequency response up to 10kHz
- Address selectable
- 16 Digital Inputs and 16 Digital Outputs are available
- ID Status readback register available in order to ensure that the PC 62C is operating correctly
- TTL compatible address, data and control signals
- Occupies 16 Word or 32 Byte locations in the I/O memory
- Fuse protected +5V and +12V power available at the connector to drive User circuits
- Driver libraries for DOS, Windows V3.11, Win ‘95 and Windows NT are supplied
- Drivers for TestPoint, DasyLab, LabView, HP VEE are supplied

- Autodetection and comprehensive Diagnostics Software provided to ensure proper operation of the PC62C
- Demonstration examples supplied
- Latest Software Update Drivers can be downloaded from our WebSite

PC 62C Package

The PC 62C package consists of:

PC 62C Interface Card
PC 62C User's Manual
EDR Developers Toolkit User Manual + EDR Software on 3½diskettes
One 5¼ OR 3½diskette (if applicable) containing the demonstration software

If any of the items is missing, contact your dealer immediately specifying which components are missing.

Chapter 1: Installation

There are two aspects of the PC 62C that must be configured using Jumpers. All other configurations are done via software:

1.1) Setting the base address

This address determines where the board is accessed. This can be set by a 8-way DIP switch found on the PC 62C Board. The address range are from 0 to 1fffh.

The PC 62C occupy a block of 32 consecutive Byte I/O addresses or 16 consecutive Word I/O addresses. The base address setting controls where the block starts. This base address must be unique to the PC 62C only and no other card must occupy this address. If multiple PC 62C boards are installed in one computer then each board must have a different base address.

The base address can be assigned to any location from 0 to 1fffh in 16 Word boundaries. Table 1 shows the I/O addresses occupied by standard interface cards. Refer to the Base Address Setting Table in Appendix A for a list of the various base address settings that the PC 62C can occupy.

The base address setting can be set by adjusting the 8-way Dip Switch on the PC 62C. Each line on the DIP switch compares an address line in I/O space. Switch number 1 compares address line A12; switch number 2: address A11 while switch number 8 compares address line A5. Factory default setting is 700h.

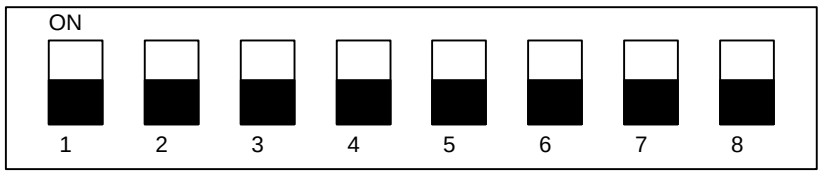
If one of the switches is OFF, then it contributes to the base address. An example is as follows:

```
Base Address    =    Switch 5(A8) + Switch 4 (A9) + Switch 3 (A10)
                =    100 + 200 + 300
                =    700h
```

Table 1: Addresses for standard I/O devices

Address	Standard device
000-1FF	Internal system board
200-20F	Games port
210-217	Expansion unit
220-24F	Reserved
250-257	Not assigned
258-25F	Intel 'Above Board'
260-277	Not assigned
278-26F	Reserved
280-2EF	Not assigned
2F0-2F7	LPT2
2F8-2FF	COM2
300-31F	Prototype Board
320-32F	Hard Disk
330-377	Not assigned
378-37F	LPT1
380-38F	SDLC communications
390-39F	Not assigned
3A0-3AF	Binary comms
3B0-3BF	Mono Display Adaptor
3C0-3CF	Reserved
3D0-3DF	CGA
3E0-3E7	Reserved
3E3-3EF	Not assigned
3F0-3F7	Floppy disk
3F8-3FF	COM1
400-FFF	Not used see below

Table 1: Standard I/O Addresses



1000	800	400	200	100	80	40	20	Hex Weight when OFF
A12	A11	A10	A9	A8	A7	A6	A5	Corresponding Address line

Figure 1: Dip Switch Address Weight (in Hex)

Note that addresses from 400h-7FFh cannot normally be used because these y are not normally decoded by some cards and I/O devices in the 0h to 3FFh range.

The PC 62C (and most other members of the PC-XX family) can use these address, if and only if the board at address 400h less than the address of the PC 62C also decodes the extra address.

For example, a PC 62C can be installed at address 300h and another one at address 700h (400h locations apart). However, it would not be advisable to install a PC 62C at address 7F8h. This is because communications port COM1 is installed at 3F8h and does not normally decode these extra addresses.

If your computer has boards not listed in Table 1 (such as LAN adaptors, back-up boards or other engineering boards), you should consult the User's Manual for these boards for information on the address ranges used.

In most cases, base address of 300h is a good choice. Address 300h is also the factory default base address setting.

1.2) Wait State Generation on the PC 62C

Some computers have very high I/O bus cycles. In this case it is neccessary to slow down these cycles when the computer accesses the PC 62C Board. Additional wait states can be set by means of a jumper on the PC 62C Board.

Additional wait states can be inserted in the I/O bus cycle by changing the jumper setting on JP1 on the PC 62C. This jumper is marked 'Wait State Jumper' on the PC 62C board. Refer to figure 1.2 for the Wait State Jumper settings. Note that the factory default setting is zero wait states.

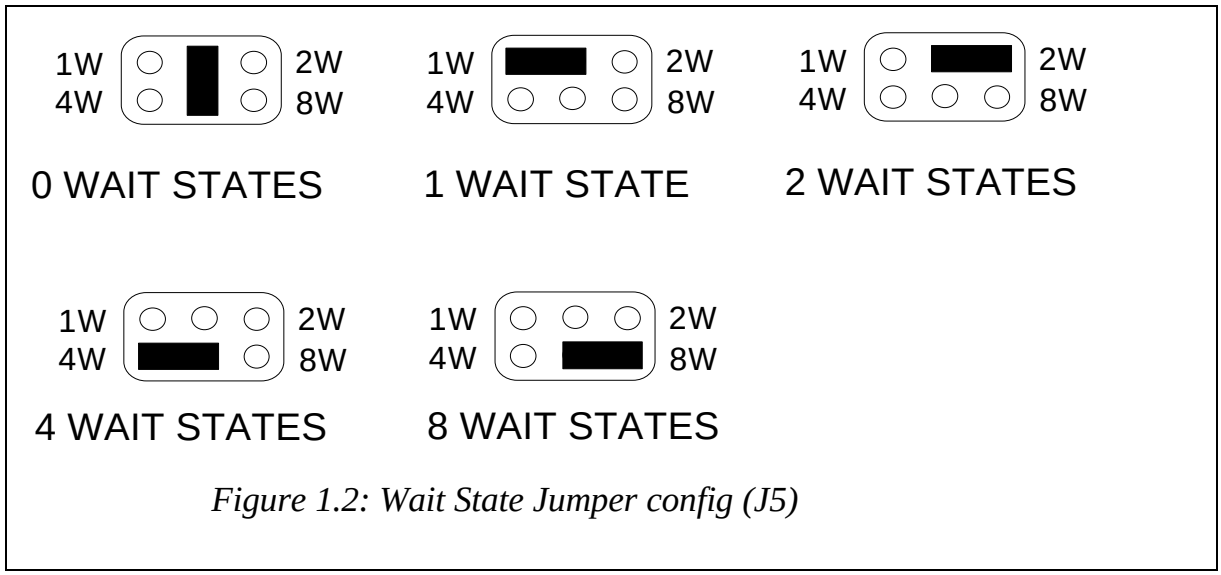


Figure 1.2: Wait State Jumper config (J5)

In most cases, only a very small number of computers require additional wait states. If the PC 62C seems to be giving incorrect results then try increasing the wait states until correct results are obtained. If the board still does not produce correct results even after the maximum number of wait states has been inserted then the PC 62C or the host computer are defective and should be serviced.

In a standard PC, the interrupt levels are allocated as follows:

Level Level	Allocation
IRQ0	System timer
IRQ1	Keyboard
IRQ2/IRQ9	Display Adaptor
IRQ3	COM1 (if installed)
IRQ4	COM2 (if installed)
IRQ5	LPT2 (if installed)
IRQ6	Floppy disk controller
IRQ7	LPT1 (if installed)
IRQ10	Not used
IRQ11	Not used
IRQ12	Used by PS/2 Mouse (if installed)
IRQ13	Coprocessor
IRQ14	Primary IDE Harddisk (if installed)
IRQ15	Secondary IDE Harddisk (if installed)

Table 1.3b: Standard Interrupt Settings

On PC ATs, IRQ2 is used by the system board and any interrupt requests on IRQ2 is transparently rerouted to IRQ9.

The default IRQ setting on the PC 62C is none. Note that unless the interrupt line is specifically enabled by software, the interrupt output from the PC 62C is tri-stated (ie: not connected). It is also tri-stated upon power-up.

1.3) Differential/Single-ended External Interrupt Jumper Setting

Each of the Input lines may be configured for differential of single-ended mode. In differential mode, each bit of two input lines has an input line and a corresponding return line. In single-ended mode, the return lines are connected to a single common return line on the DB37 connector. They are COMA (pin 17) for the Returns of Opto-isolator 0 to 7 and COMB (Pin 36) for the Returns of Opto-Isolator 8 to 15. Differential mode is useful where inputs of opposite polarity are to be sampled.

The optically isolated input lines can be connected differentially or single ended. Figure 1.5 illustrates this graphically:

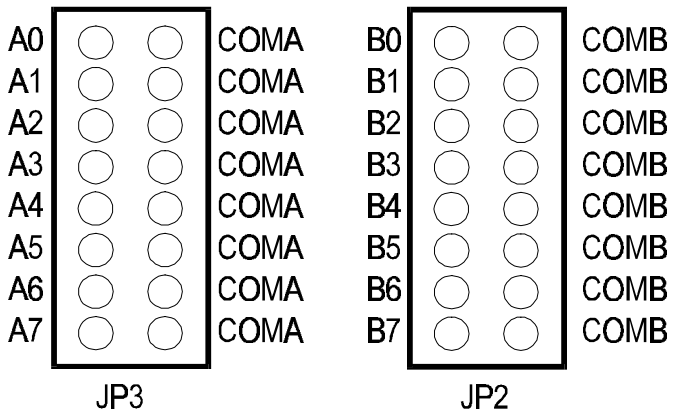


Figure 1.5a: Optically Isolated Input Diff/Single-ended Jumper Setting

Jumper JP3 - A0 is shorted to COMA, it simply shorts the Optically Isolated Line Return to COMA on the DB37 Connector. You can connect COMA (or COMB) to Digital Ground (Pin 37) if you want to ground the Return Lines.

1.4) Interrupt Enable/Disable Jumpers

The IRQ lines on the PC 62C Board are active high but are tri-stated upon powerup. Certain non-compatible computer cards does not like this type of configuration. In certain cases, some IRQ lines are already occupied by certain Plug and Play Cards. Provision was hence made to disconnect the unused IRQ lines from the ISA BUS completely. By removing the jumper, you automatically disconnect the IRQ line from the BUS. Examples of jumper settings are as follows:

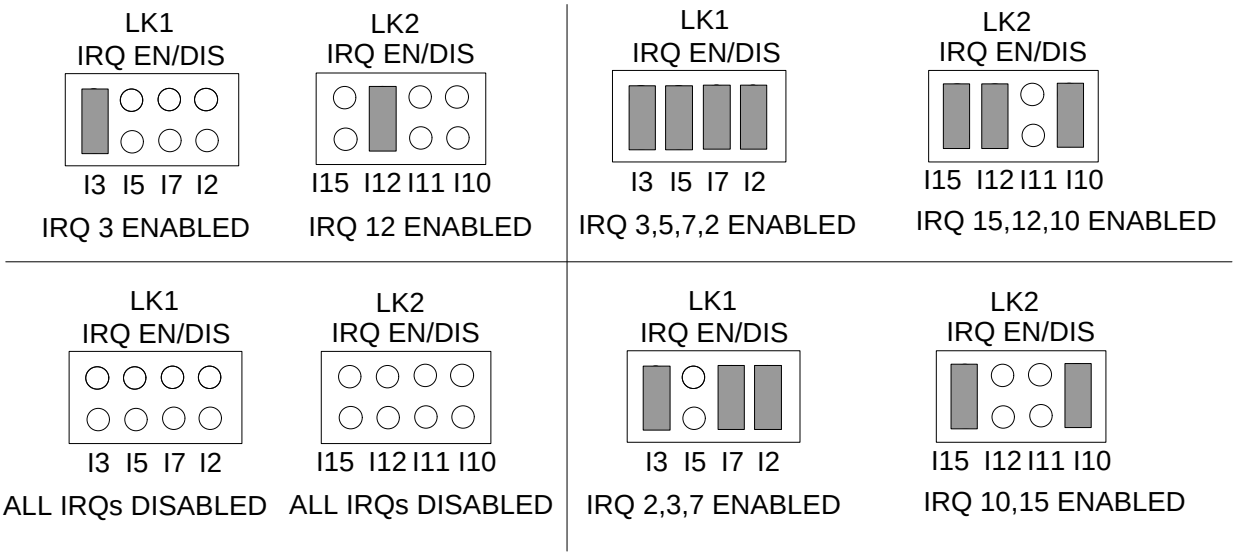


Figure 3a: IRQ Enable/Disable Jumper Settings

1.5) Connecting the PC 62C to the PC Backplane

Requirements: AT/286/386/486, ISA, EISA, Pentium, Pentium Pro Computer
Phillips Screw Driver (or one to match screw on the computer cabinet and bracket)
16 bit bus slot

Procedure:

a) Switch off the computer and all attached devices
b) Unplug power cord from the computer and all attached devices.

> **+ Warning**
>
> Failure to disconnect all power cables can result in harzardous conditions, as there may be dangerous voltage levels present in externally connected cables.

c) Remove the top cover from the PC. If you are not sure how to do this, consult the manual supplied with the system unit.

d) Choose any 16 bit expansion slot and remove the screw from the metal bracket fixed corresponding to the chosen slot.

e) Align the gold plated edge connector with the edge socket and the rear adaptor slot with the board bracket. Firmly press the board down into the socket on the computer's system board. Ensure that the board's edge connector is in the socket and has not slipped sideways past the socket.

f) Replace the screw on the bracket and tighten the screw to the back panel.

g) Replace the computer's cover. Plug in all cables and switch the computer power on. The PC 62C is now installed.

CHAPTER 2: Interconnections

2.0) Introduction

The PC 62C 16 Digital I/O board plugs into any ISA expansion slot at the gold finger edge connectors J1/J2 and J3/J4. The board communicates to the user circuit via IDE connectors mounted on the PC board. This chapter describes these connectors.

2.1) Connections to the IBM AT Bus

The PC 62C board may be plugged into any 16 bit slot of the AT computer's backplane. All data transfers to and from the host computer are channelled via these connectors.

2.2) PC 62C DB37 User Connector (P1)

The PC 62C optically isolated inputs interfaces to the external world via a D-Type 37 way male connector.

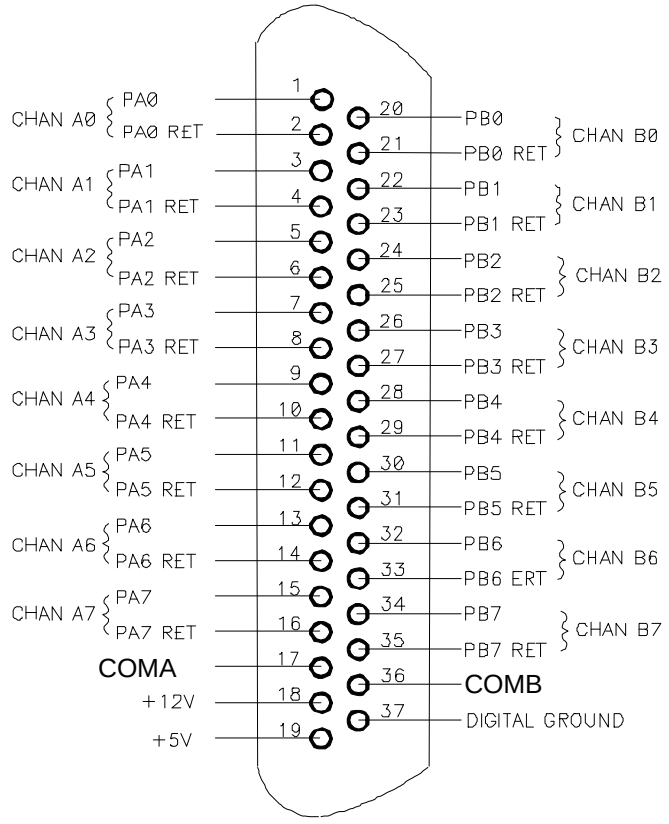


Figure 2.2: PC 62C Interface Connector (as seen from the rear of the PC)

Figure 4 graphically shows the connector together with their pin assignments. Note that the pin connections refer to the pin numbers of the connector when looking into the

connector from the rear of the computer. Also note that the pin numbers are embossed on the connector itself.

The +5V, +12V power lines are available on the connector. Precautionary measures should be taken when using these supplies.

> **Warning**
>
> The maximum permissible current drawn on the I/O connector (P1) for the +5V and +12V supplies are 250mA. Exceeding this can cause irreparable damage to the PC 62C and your computer.

2.3) Description of Operation

Looking into a single bit of input port, the external signal sees a diode. If the forward voltage applied is greater than about 3.1V, the diode will conduct and the corresponding bitin the port will reflect a 1 to the host computer. A logical high is defined from 3.1V to a max of 24V. If the voltage applied between the input lines is less than 3.1V the computer will interpret the input as a 0. A logical low pulse into the opto-isolator is defined from 0 to 2.9V. Figure 2.3a illustrates the optically isolated connections.

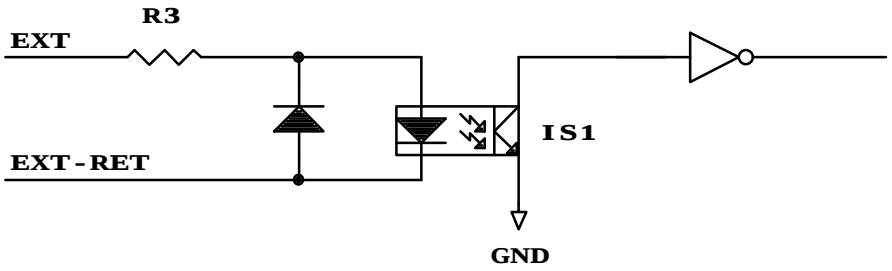


Figure 2.3a: Optically Isolated Input Line

From the above diagram, the minimum operating current for the input diode is about 6mA. Inputs are protected against reverse voltages up to 400V and are current limited. If a reverse voltage is applied, the protection diode will clamp the reverse voltage to 0.7V.

The output is connected to the interrupt line of the IBM bus via associated circuitry and is configured and controlled via software. Pulses above 3.1V to 24V will trigger the opto-isolator in generating a TTL pulse to enable an IRQ. A voltage greater than 3.1V can also trigger an interrupt in order to determine a status change in the inputs. This is useful in multitasking enviroments such as Windows V3.11, Win ’95 and Win NT because the PC62C will be accessed if an only if a status change in one of the port lines has occurred.

The status of the optically isolated inputs is kept in a register. This register can be read as a single 16 bit word or two 8 bit bytes. 16 bit accesses are much faster and is recommended in multitasking enviroments.

, Useful Tip

The status of the optically isolated inputs is kept in a 16 bit Register. This register can be read as a single 16 bit word or two 8 bit bytes. 16 bit accesses are much faster and is recommended in multitasking enviroments.

2.4) Digital I/O Interface

There are 16 digital Inputs and 16 Digital Outputs available on the PC62C via Header J6. The digital I/O lines on the PC 62C are directly compatible with most forms of TTL and CMOS logic operating from +5V supplies. Detailed specifications on the digital I/O lines are found in Appendix A: Specifications.

A logical Low is from 0 to 0.8V and a Logical High is from 2.0V to +5.1V. Although these are defined as TTL Levels it is recommended that a logical Low voltage is from 0V to 0.3V and a logical high is from 4.5V to 5.1V.

The digital Inputs and Outputs can be read and written as a single 16 Bit Word (recommended) or alternatively two 8 bit Bytes.

Connector Header (J6) details are shown below:

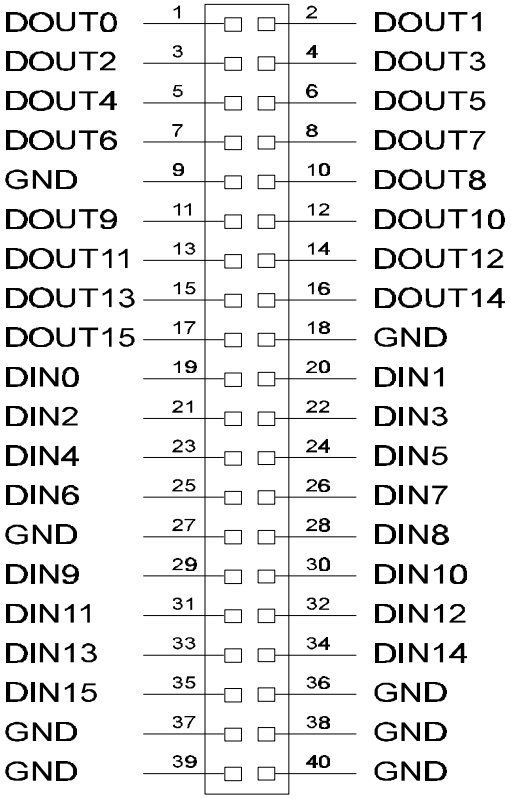


Figure 2.4a: Digital I/O Header (J6)

All unused digital inputs should be grounded. The digital Outputs are open collector outputs and are capable of driving 20mA in a Low State.

> **Warning**
>
> DO NOT exceed 5.1V or fall below 0V on the I/O ports of the PC 62C. Permanent damage will result if these thresholds are exceeded.

2.5) Power supply connections

The +12V and +5V power and digital ground are available on the DB37 Male Connector (P1). These are equipped with Polyswitches that will open circuit if the max permissible current of 250mA is exceeded. Connections to the power lines will be restored if the current falls below the max permissible current draw.

> **Warning**
>
> The maximum permissible current draw on the +5V and the +12V lines on the I/O connector is 250mA.

CHAPTER 3: Register Structure

3.0) Introduction

At the lowest level, the PC 62C can be programmed using I/O input and output instructions. This chapter contains the information on all the PC 62C registers. Although programming the board is not difficult, it is time consuming and requires detailed knowledge of the PC 62C as well as the operation of the host PC and its operating system. In order to simplify the process, a set of driver libraries is provided. The use of these libraries allows access to all the board's functions and is described in Chapter 5: Programming guide.

The PC 62C occupies 32 consecutive Word addresses in the computer's I/O space. The layout of these registers is shown in Table 4: PC 62C Register Structure. The offset of the registers is given as offset addresses from the base address of the board. This base address is set with the DIP Switch as detailed in Chapter 2: Installation. It is important that 16 bit reads and writes are initiated in order to minimize host CPU time. In multitasking enviroments two 8 bit reads and writes will take much more host CPU time than a single 16 bit read or write.

Offset	Read	Write
0	Opto Isolator 0 Status (OPTORD0)	Reserved
2	Global Status Register (GLOBAL)	Global Status Register (GLOBAL)
4	Global Control Register (GLCNTRL)	Global Control Register (GLCNTRL)
6	IRQ Gate Control Register (IGATE)	IRQ Gate Control Register (IGATE)
8	Global Buffer Status Register (GBUF)	Reserved
10	Local Mux IRQ Register 0 (IMUXP0)	Local Mux IRQ Register 0 (IMUXP0)
12	Local Mux IRQ Register 1 (IMUXP1)	Local Mux IRQ Register 1 (IMUXP1)
14	Local Mux IRQ Register 2 (IMUXP2)	Local Mux IRQ Register 2 (IMUXP2)
16	Reserved	Reserved
18	IRQ Set/Reset Status Register (ISETX)	Interrupt Set/Reset Register (ISETX)
20	Digital I/O Read Register (DIO)	Digital I/O Write Register (DIO)
22	Opto Isolator 1 Status (OPTORD1)	Reserved
24	Opto Isolator 2 Status (OPTORD2)	Reserved
26	Opto Isolator 3 Status (OPTORD3)	Reserved
28	Reserved	Reserved
30	Reserved	Reserved
	Reserved	Reserved

Table 4: PC 62C Register Structure

3.1) OPTORD0 - Optically Isolated Input Port Register (offset 0, read only)

The register allows one to read the status of all 16 Optically Isolated Input Lines. The Register structure is described below.

OPTORD0 Register (read)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

Bit 0 to 7: The bits PA7 down to PA0 reflect the status of the first 8 optically isolated inputs.

Bit 8 to 15: The bits PB7 down to PB0 reflect the status of the second 8 optically isolated inputs.

It is recommended that a 16 bit read is initiated when reading the status of the Port. Note, however, that two 8 bit reads can also be performed. This feature was included in order to maintain compatibility with the PC62B.

3.2) GLOBAL – Global Status Register (offset 2, read/write)

This register is used to monitor and reset the Global IRQ Set Register. GRES0/1 is used to reset the Register while GIRQTOG0/1 is used to check if any bit in the OPTORD Register (Offset 0) was set.

GLOBAL Register (write mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0	0	0	0	0	0	0	0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	GRES1	GRES0

Global Register (read mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
x	x	x	x	x	x	x	x

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
x	x	GIRQTOG1	GIRQTOG0	GIRQEN1	GIRQEN0	GRES1	GRES0

Bit 0: This bit is used to reset the first 8 flip-flops [B0 thru B7] of the global register. Writing a 0 and then a 1 will reset all 8 low bit flip-flops [B0 to B7] to 0.

Reading this bit gives the status of the GRES0 bit.

Bit 1: This bit is used to reset the second set of 8 flip-flops [B8 thru B15] of the global register. Writing a 0 and then a 1 will reset all 8 high bit flip-flops [B8 to B15] to 0.

Reading this bit gives the status of the GRES1 bit.

Bit 2: Reserved for Future use. Write a 0 to this bit. Reading this bit is undefined.

Bit 3: Reserved for Future use. Write a 0 to this bit. Reading this bit is undefined.

Bit 4: This bit provides the status of the first 8 flip-flops of the Global Buffer Register (GBUF). If this bit is set then one of the flip-flops in the Low Order GBUF Register (ie: PAX0 to PAX7] was enabled. This means that one of the Opto Isolator was set. If this bit is 0 then none of the GBUF flip-flops [Low Order] is set.

Bit 5: This bit provides the status of the high 8 bit flip-flops of the Global Buffer Register (GBUF). If this bit is set the one of the high 8 bit flip-flops in the GBUF Register was enabled. This means that one of the last 8 Opto Isolator was set. If this bit is 0 then none of the High Order GBUF flip-flops is set.

Bits 6-15: Reserved for Future use. Write a 0 to these bits. Reading these bits are undefined.

3.3) GLCNTRL – Global Control Register (offset 4, read/write)

This register is used to enable the Mux that sets the Global Buffer to a specific IRQ. If any one of the Opto-isolators was enabled, the pulse is set up and vectored to the Multiplexor to a specific IRQ. This register enables and configures this line to any of 8 IRQs lines.

GLCNTRL Register (write mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0	0	0	0	0	0	0	0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IGATEG1	IGATEG0	IMUXG5	IMUXG4	IMUXG3	IMUXG2	IMUXG1	IMUXG0

GLCNTRL Register (read mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
x	x	x	x	x	x	x	x

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IGATEG1	IGATEG0	IMUXG5	IMUXG4	IMUXG3	IMUXG2	IMUXG1	IMUXG0

Bits 0-2: IMUXG0 to IMUXG3 - These bits are used to set up a global IRQ line for the first 8 opto-isolators. The status of any opto-isolator can be checked using the Global Register GBUF (Offset 8) using a 16 bit read.

Reading back these bits determines the status of IMUXG0 to IMUXG2 Control lines.

IMUXG2	IMUXG1	IMUXG0	IGATE0	IRQ
0	0	0	1	10
0	0	1	1	11
0	1	0	1	12
0	1	1	1	15
1	0	0	1	2
1	0	1	1	7
1	1	0	1	5
1	1	1	1	3

Table 3.3a: Mux Table for setting IRQs

Bits 3-5: IMUXG3 to IMUXG5 - These bits are used to set up a global IRQ line for the last 8 opto-isolators. The status of any opto-isolator can be checked using the Global Register GBUF (Offset 8) using a 16 bit read.

Reading back these bits determines the status of the IMUXG3 to IMUXG5 Control lines.

Bits 6: IGATEG0 – This bit is used to enable/disable Global Interrupts. Setting this bit to 1 enables one to select any one of 8 IRQ on the ISA Bus. Setting this bit to 0 disables Interrupts vectored from a pulse generated if any one of the first 8 opto-isolators goes high.

Reading this bit determines the status of the IGATE0 bit.

Bits 7: IGATEG1 – This bit is used to enable/disable Global Interrupts. Setting this bit to 1 enables one to select any one of 8 IRQ on the ISA Bus. Setting this bit to 0

disables Interrupts vectored from a pulse generated if any one of the last 8 opto-isolators goes high.

Reading this bit determines the status of the IGATE1 bit.

Bits 8-15: Reserved for Future use. Write a 0 to these bits. Reading these bits is undefined.

3.4) IGATE – IRQ Gate Control Register (offset 6, read/write)

This register is used to enable the Gate controlling the Muxes that map each opto-isolator input to a specific IRQ line. The MUX Control Registers (3 lines per Opto-Isolator Input) is found in the IMUX0 (offset 10), IMUX1 (offset 12), IMUX2 (offset 14), IMUX3 (offset 16) Control Registers. For example: In the IMUX0 Control Register, bits 0 to 2 set the IRQ Line of the 1st Opto-isolator. If the IGATE0 bit is 1 then a rising edge on the first Opto-isolator will be mapped to an IRQ Line set via Bits 0 to 2 in the IMUX0 Register. If IGATE0 bit is 0 then the IRQ Lines are effectively disconnected from the IRQ Bus. This means that a rising edge on the first Opto-isolator will NOT be mapped to an IRQ Line set via Bits 0 to 2 in the IMUX0 Register.

IGATE Register (write mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IGATE15	IGATE14	IGATE13	IGATE12	IGATE11	IGATE10	IGATE9	IGATE8

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IGATE7	IGATE6	IGATE5	IGATE4	IGATE3	IGATE2	IGATE1	IGATE0

IGATE Register (read mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IGATE15	IGATE14	IGATE13	IGATE12	IGATE11	IGATE10	IGATE9	IGATE8

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IGATE7	IGATE6	IGATE5	IGATE4	IGATE3	IGATE2	IGATE1	IGATE0

Bit0: IGATE0 – This bit is used to enable/disable Interrupt support for Opto-isolator input 0. Setting this bit to 1 enables one to select any one of 8 IRQ on the ISA Bus. The actual IRQ selection is determined by the IMUXP0 Register (offset 10). For example, bits 0 to 2 sets the IRQ selection for Opto-Isolator 0, with IGATE0 enabling/disable interrupt support. Table 3.4a determines the IRQ selection. Setting the IGATE0 bit to 0 disables Interrupts support for Opto-isolator 0.

Reading this bit determines the status of the IGATE0 bit.

IMUX2	IMUX1	IMUX0	IGATE0	IRQ
Bit 2	**Bit 1**	**Bit 0**	**IGATE0**	**IRQ**
0	0	0	1	10
0	0	1	1	11
0	1	0	1	12
0	1	1	1	15
1	0	0	1	2
1	0	1	1	7
1	1	0	1	5
1	1	1	1	3

Table 3.4a: Mux Table for setting IRQs

Bit1: IGATE1 – This bit is used to enable/disable Interrupt support for Opto-isolator input 1 (PA1). Setting this bit to 1 enables one to select any one of 8 IRQ on the ISA Bus. The actual IRQ selection is determined by the IMUXP0 Register (offset 10). For example, bits 3 (low) to 5 (high) sets the IRQ selection on Opto-Isolator 1, with IGATE0 enabling/disabling interrupt support. Table 3.4a gives an example of how the IRQ selection is determined. Setting the IGATE1 bit to 0 disables Interrupts support for Opto-isolator 1.

Reading this bit determines the status of the IGATE1 bit.

Bit2: IGATE2 – This bit is used to enable/disable Interrupt support for Opto-isolator input 2 (PA2). Setting this bit to 1 enables one to select any one of 8 IRQs on the ISA Bus. The actual IRQ selection is determined by the IMUXP0 Register (offset 10). For example, bits 6 (low) to 8 (high) set the IRQ selection for Opto-Isolator 2, with IGATE0 enabling/disabling interrupt support. Table 3.4a gives an example of how the IRQ selection is determined. Setting the IGATE2 bit to 0 disables Interrupts support for Opto-isolator 2.

Reading this bit determines the status of the IGATE2 bit.

Bit3: IGATE3 – This bit is used to enable/disable Interrupt support for Opto-isolator input 3 (PA3). Setting this bit to 1 enables one to select any one of 8 IRQs on the ISA Bus. The actual IRQ selection is determined by the IMUXP0 Register (offset 10). For example, bits 9 (low) to 11 (high) set the IRQ selection for Opto-Isolator 3, with IGATE3 enabling/disabling interrupt support. Table 3.4a gives an example of how the IRQ selection is determined. Setting the IGATE3 bit to 0 disables Interrupts support for Opto-isolator 3.

Reading this bit determines the status of the IGATE3 bit.

Bit4: IGATE4 – This bit is used to enable/disable Interrupt support for Opto-isolator input 4 (PA4). Setting this bit to 1 enables one to select any one of 8 IRQs on the ISA Bus. The actual IRQ selection is determined by the IMUXP0 Register (offset 10). For example, bits 12 (low) to 14 (high) set the IRQ selection for Opto-Isolator 4, with IGATE4 enabling/disabling interrupt support. Table 3.4a gives an example of how the IRQ selection is determined. Setting the IGATE4 bit to 0 disables Interrupts support for Opto-isolator 4.

Reading this bit determines the status of the IGATE4 bit.

Bit5: IGATE5 – This bit is used to enable/disable Interrupt support for Opto-isolator input 5 (PA5). Setting this bit to 1 enables one to select any one of 8 IRQs on the ISA Bus. The actual IRQ selection are determined by the IMUXP0 and IMUXP1 Registers (offset 12). For example, bit 15 (A0) in the IMUXP0 Register is the low bit in the decoder and Bit1 in the IMUXP1 Register is the high bit in the decoder. These bits set the IRQ selection for Opto-Isolator 5, with IGATE5 enabling/disabling interrupt support. Table 3.4b gives an example of how the IRQ selection is determined. Setting the IGATE5 bit to 0 disables Interrupts support for Opto-isolator 5.

Reading this bit determines the status of the IGATE5 bit.

1IMUX1	1IMUX0	0IMUX15	IGATE5	IRQ
Bit 1	**Bit 0**	**Bit 15**	**Bit 5**	**IRQ**
0	0	0	1	10
0	0	1	1	11
0	1	0	1	12
0	1	1	1	15
1	0	0	1	2
1	0	1	1	7
1	1	0	1	5
1	1	1	1	3

Table 3.4b: Mux Table for setting IRQs on Opto-isolator 6

Bit6: IGATE6 – This bit is used to enable/disable Interrupt support for Opto-isolator input 6 (PA6). Setting this bit to 1 enables one to select any one of 8 IRQs on the ISA Bus. The actual IRQ selection is determined by the IMUXP1 Register (offset 12). For example, bits 2 (low) to 4 (high) set the IRQ selection for Opto-Isolator 6, with IGATE6 enabling/disabling interrupt support. Table 3.4a gives an example of how the IRQ selection is determined. Setting the IGATE6 bit to 0 disables Interrupts support for Opto-isolator 6.

Reading this bit determines the status of the IGATE6 bit.

Bit7: IGATE7 – This bit is used to enable/disable Interrupt support for Opto-isolator input 7 (PA7). Setting this bit to 1 enables one to select any one of 8 IRQs on the ISA Bus. The actual IRQ selection is determined by the IMUXP1 Register (offset 12). For example, bits 5 (low) to 7 (high) set the IRQ selection for Opto-Isolator 7, with IGATE7 enabling/disabling interrupt support. Table 3.4a gives an example of how the IRQ selection is determined. Setting the IGATE7 bit to 0 disables Interrupts support for Opto-isolator 7.

Reading this bit determines the status of the IGATE7 bit.

Bit8: IGATE8 – This bit is used to enable/disable Interrupt support for Opto-isolator input 8 (PA8). Setting this bit to 1 enables one to select any one of 8 IRQs on the ISA Bus. The actual IRQ selection is determined by the IMUXP1 Register (offset 12). For example, bits 8 (low) to 10 (high) set the IRQ selection for Opto-Isolator 8, with IGATE8 enabling/disabling interrupt support. Table 3.4a gives an example of how the IRQ selection is determined. Setting the IGATE8 bit to 0 disables Interrupts support for Opto-isolator 8.

Reading this bit determines the status of the IGATE8 bit.

Bit9: IGATE9 – This bit is used to enable/disable Interrupt support for Opto-isolator input 9 (PA9). Setting this bit to 1 enables one to select any one of 8 IRQs on the ISA Bus. The actual IRQ selection is determined by the IMUXP1 Register (offset 12). For example, bits 11 (low) to 13 (high) set the IRQ selection for Opto-Isolator 9, with IGATE9 enabling/disabling interrupt support. Table 3.4a gives an example of how the IRQ selection is determined. Setting the IGATE9 bit to 0 disables Interrupts support for Opto-isolator 9.

Reading this bit determines the status of the IGATE9 bit.

Bit10: IGATE10 – This bit is used to enable/disable Interrupt support for Opto-isolator input 10 (PA10). Setting this bit to 1 enables one to select any one of 8 IRQs on the ISA Bus. The actual IRQ selection are determined by the IMUXP1 and the IMUXP2 Registers (offset 12 and 14). For example, bit 14 (A0) in the IMUXP1 Register is the low bit in the decoder and Bit0 in the IMUXP2 Register is the high bit in the decoder. These bits set the IRQ selection for Opto-Isolator 10, with IGATE10 enabling/disabling interrupt support. Table 3.4b gives an example of how the IRQ selection is determined. Setting the IGATE10 bit to 0 disables Interrupts support for Opto-isolator 10.

Reading this bit determines the status of the IGATE10 bit.

Bit11: IGATE11 – This bit is used to enable/disable Interrupt support for Opto-isolator input 11 (PA11). Setting this bit to 1 enables one to select any one of 8 IRQs on the ISA Bus. The actual IRQ selection is determined by the IMUXP2 Register (offset 14). For example, bits 1 (low) to 3 (high) set the IRQ selection for Opto-Isolator 11, with IGATE11 enabling/disabling interrupt support. Table 3.4a gives an example of how the IRQ selection is determined. Setting the IGATE11 bit to 0 disables Interrupts support for Opto-isolator 11.

Reading this bit determines the status of the IGATE11 bit.

Bit12: IGATE12 – This bit is used to enable/disable Interrupt support for Opto-isolator input 12 (PA12). Setting this bit to 1 enables one to select any one of 8 IRQs on the ISA Bus. The actual IRQ selection is determined by the IMUXP2 Register (offset 14). For example, bits 4 (low) to 6 (high) set the IRQ selection for Opto-Isolator 12, with IGATE12 enabling/disabling interrupt support. Table 3.4a gives an example of how the IRQ selection is determined. Setting the IGATE12 bit to 0 disables Interrupts support for Opto-isolator 12.

Reading this bit determines the status of the IGATE12 bit.

Bit13: IGATE13 – This bit is used to enable/disable Interrupt support for Opto-isolator input 13 (PA13). Setting this bit to 1 enables one to select any one of 8 IRQs on the ISA Bus. The actual IRQ selection is determined by the IMUXP2 Register (offset 14). For example, bits 7 (low) to 9 (high) set the IRQ selection for Opto-Isolator 13, with IGATE13 enabling/disabling interrupt support. Table 3.4a gives an example of how the IRQ selection is determined. Setting the IGATE13 bit to 0 disables Interrupts support for Opto-isolator 13.

Reading this bit determines the status of the IGATE13 bit.

Bit14: IGATE14 – This bit is used to enable/disable Interrupt support for Opto-isolator input 14 (PA14). Setting this bit to 1 enables one to select any one of 8 IRQs on the ISA Bus. The actual IRQ selection is determined by the IMUXP2 Register (offset 14). For example, bits 10 (low) to 12 (high) set the IRQ selection for Opto-Isolator 14, with IGATE14 enabling/disabling interrupt support. Table 3.4a gives an example of how the IRQ selection is determined. Setting the IGATE14 bit to 0 disables Interrupts support for Opto-isolator 14.

Reading this bit determines the status of the IGATE14 bit.

Bit15: IGATE15 – This bit is used to enable/disable Interrupt support for Opto-isolator input 15 (PA15). Setting this bit to 1 enables one to select any one of 8 IRQs on the ISA Bus. The actual IRQ selection is determined by the IMUXP2 Register (offset 14). For example, bits 13 (low) to 15 (high) set the IRQ selection for Opto-Isolator 15, with IGATE15 enabling/disabling interrupt support. Table 3.4a

gives an example of how the IRQ selection is determined. Setting the IGATE15 bit to 0 disables Interrupts support for Opto-isolator 15.

Reading this bit determines the status of the IGATE15 bit.

3.5) GBUF – Global Buffer Status Register (offset 8, read only)

This register is used to determine whether a positive level shift did occur in any one of the Opto-Isolators when using Global Interrupt share mode. 16 bit read to these registers are recommended.

GBUF Register (read only)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PBX7	PBX6	PBX5	PBX4	PBX3	PBX2	PBX1	PBX0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAX7	PAX6	PAX5	PAX4	PAX3	PAX2	PAX1	PAX0

Bits 0-7: PAX0 to PAX7 - These bits determine whether a positive edge has occurred in any of the low order (D0 to D7) Opto-isolators Inputs. If a high is detected on any of the bits then a positive transition has occurred on that opto-isolator. If one of the bits is set, it can result in an interrupt occuring if the IGATEG0 Bit (Bit 6) in the GLCNTRL Register (offset 4) is enabled and the IRQ set accordingly. You can clear the PAX0 to PAX7 registers by writing a 0 and then a 1 to the GRES0 bit (bit 0) in the Global Status Register (offset 2).

Bits 8-15: PBX0 to PBX7 - These bits determine whether a positive edge has occurred in any of the high order (D8 to D15) Opto-isolators Inputs. If a high is detected on any of the bits then a positive transition has occurred on that opto-isolator. If one of the bits is set, it can result in an interrupt occuring if the IGATEG1 Bit (Bit 7) in the GLCNTRL Register (offset 4) is enabled and the IRQ set accordingly. You can clear the PBX0 to PBX7 registers by writing a 0 and then a 1 to the GRES1 bit (bit 1) in the Global Status Register (offset 2).

3.6) IMUXP0 – Local Mux Interrupt Control Register (offset 10, read/write)

This register is used to set individual interrupts for each optically isolated input. Effectively MUXP0 is used as address lines to map each optically isolated inputs to a specific IRQ. If any one of the Opto-isolators was enabled, the pulse is set up and vectored to the Decoder to a specific IRQ. This register configures this line to any of 8 IRQs lines.

IMUXP0 Register (write mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
MUXP5A0	MUXP4A2	MUXP4A1	MUXP4A0	MUXP3A2	MUXP3A1	MUXP3A0	MUXP2A2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MUXP2A1	MUXP2A0	MUXP1A2	MUXP1A1	MUXP1A0	MUXP0A2	MUXP0A1	MUXP0A0

IMUXP0 Register (read mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
MUXP5A0	MUXP4A2	MUXP4A1	MUXP4A0	MUXP3A2	MUXP3A1	MUXP3A0	MUXP2A2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MUXP2A1	MUXP2A0	MUXP1A2	MUXP1A1	MUXP1A0	MUXP0A2	MUXP0A1	MUXP0A0

Bits 0-2: MUXP0A0 to MUXP0A2 - These bits are used to set up an IRQ line for the Opto-isolator 0 (PA0). Bits 0 to 2 sets the IRQ selection for Opto-Isolator 0, with IGATE0 enabling/disable interrupt support. IGATE0 must be enabled in order to select an interrupt. Table 3.6a determines the appropriate writes to Bits 0 to 2 to select 1 of 8 IRQs.

Reading these bits determines the status of MUXP0A0 to MUXP0A2.

MUXP0A2	MUXP0A1	MUXP0A0	IGATE0	IRQ
Bit 2	Bit 1	Bit 0		
A2	A1	A0	Gx	
0	0	0	1	10
0	0	1	1	11
0	1	0	1	12
0	1	1	1	15
1	0	0	1	2
1	0	1	1	7
1	1	0	1	5
1	1	1	1	3

Table 3.6a: Mux Table for setting IRQs for Opto-Isolator 0

Bits 3-5: MUXP1A0 to MUXP1A2 - These bits are used to set up an IRQ line for the Opto-isolator 1 (PA1). Bits 3 to 5 sets the IRQ selection for Opto-Isolator 1, with IGATE1 enabling/disable interrupt support. IGATE1 must be enabled in order to select an interrupt. Table 3.6a gives an example of the appropriate writes from Bits 3 to 5 to select 1 of 8 IRQs. Bit 3 is Address Decode A0, Bit 4 is Address Decode A1, Bit 5 is Address Decode A2 and Gx is IGATE1.

Reading these bits determines the status of MUXP1A0 to MUXP1A2 bits.

Bits 6-8: MUXP2A0 to MUXP2A2 - These bits are used to set up an IRQ line for the Opto-isolator 2 (PA2). Bits 6 to 8 sets the IRQ selection for Opto-Isolator 2, with IGATE2 enabling/disable interrupt support. IGATE2 must be enabled in order to select an interrupt. Table 3.6a gives an example of the appropriate writes from Bits 6 to 8 to select 1 of 8 IRQs. Bit 6 is Address Decode A0, Bit 7 is Address Decode A1, Bit 8 is Address Decode A2 and Gx is IGATE2.

Reading these bits determines the status of MUXP2A0 to MUXP2A2.

Bits 9-11: MUXP3A0 to MUXP3A2 - These bits are used to set up an IRQ line for the Opto-isolator 3 (PA3). Bits 9 to 11 sets the IRQ selection for Opto-Isolator 3, with IGATE3 enabling/disable interrupt support. IGATE3 must be enabled in order to select an interrupt. Table 3.6a gives an example of the appropriate writes from Bits 9 to 11 to select 1 of 8 IRQs. Bit 9 is Address Decode A0, Bit 10 is Address Decode A1, Bit 11 is Address Decode A2 and Gx is IGATE3.

Reading these bits determines the status of MUXP3A0 to MUXP3A2.

Bits 12-14: MUXP4A0 to MUXP4A2 - These bits are used to set up an IRQ line for the Opto-isolator 4 (PA4). Bits 12 to 14 sets the IRQ selection for Opto-Isolator 4, with IGATE4 enabling/disable interrupt support. IGATE4 must be enabled in order to select an interrupt. Table 3.6a gives an example of the appropriate writes from Bits 12 to 14 to select 1 of 8 IRQs. Bit 12 is Address Decode A0, Bit 13 is Address Decode A1, Bit 14 is Address Decode A2 and Gx is IGATE4.

Reading these bits determines the status of MUXP4A0 to MUXP4A2.

Bits 15: MUXP5A0 - This bit in conjunction with bits 0 and 1 in the IMUXP1 Register are used to set up an IRQ line for the Opto-isolator 5 (PA5). MUXP5A0, MUXP5A1 and MUXP5A2 sets the IRQ selection for Opto-Isolator 5, with IGATE5 enabling/disable interrupt support. IGATE5 must be enabled in order to select an interrupt. Table 3.6a gives an example of the appropriate writes from Bits 15, Bit 0 and 1 in IMUXP1 in order to select 1 of 8 IRQs. Bit 15 is Address Decode A0, Bit 0 (IMUXP1 Register) is Address Decode A1, Bit 2 (IMUXP1 Register) is Address Decode A2 and Gx is IGATE5.

Reading this bit determines the status of MUXP5A0.

3.7) IMUXP1 – Local Mux Interrupt Control Register 2 (offset 12, read/write)

This register is used to set individual interrupts for each optically isolated input. Effectively MUXP1 is used as address lines to map each optically isolated inputs to a specific IRQ. If any one of the Opto-isolators was enabled, the pulse is set up and vectored to the Decoder to a specific IRQ. This register configures this line to any of 8 IRQs lines.

IMUXP1 Register (write mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
MUXP10A1	MUXP10A0	MUXP9A2	MUXP9A1	MUXP9A0	MUXP8A2	MUXP8A1	MUXP8A0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MUXP7A2	MUXP7A1	MUXP7A0	MUXP6A2	MUXP6A1	MUXP6A0	MUXP5A2	MUXP5A1

IMUXP1 Register (read mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
MUXP10A1	MUXP10A0	MUXP9A2	MUXP9A1	MUXP9A0	MUXP8A2	MUXP8A1	MUXP8A0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MUXP7A2	MUXP7A1	MUXP7A0	MUXP6A2	MUXP6A1	MUXP6A0	MUXP5A2	MUXP5A1

Bits 0-1: MUXP5A1 to MUXP5A2 - This bit in conjunction with MUXP5A0 (bit 15) in the IMUXP0 Register are used to set up an IRQ line for the Opto-isolator 5 (PA5). MUXP5A0, MUXP5A1 and MUXP5A2 sets the IRQ selection for Opto-Isolator 5, with IGATE5 enabling/disable interrupt support. IGATE5 must be

enabled in order to select an interrupt. Table 3.6a gives an example of the appropriate writes from Bits 15, Bit 0 and 1 in IMUXP1 in order to select 1 of 8 IRQs. Bit 15 is Address Decode A0 (IMUXP0 Register), Bit 0 (IMUXP1 Register) is Address Decode A1, Bit 2 (IMUXP1 Register) is Address Decode A2 and Gx is IGATE5.

Reading this bit determines the status of MUXP5A1 and MUXP5A2.

Address A2	Address A1	Address A0	Gate Cntrl	IRQ
MUXP0A2 (Bit2)	MUXP0A1 (Bit1)	MUXP0A0 (Bit0)	IGATE0 (Bit0)	
MUXP1A2 (Bit5)	MUXP1A1 (Bit4)	MUXP1A0 (Bit3)	IGATE1 (Bit1)	
MUXP2A2 (Bit8)	MUXP2A1 (Bit7)	MUXP2A0 (Bit6)	IGATE2 (Bit2)	
MUXP3A2 (Bit11)	MUXP3A1 (Bit10)	MUXP3A0 (Bit9)	IGATE3 (Bit3)	
MUXP4A2 (Bit14)	MUXP4A1 (Bit13)	MUXP4A0 (Bit12)	IGATE4 (Bit4)	
MUXP5A2 (Bit1)	MUXP5A1 (Bit0)	MUXP5A0 (Bit15)	IGATE5 (Bit5)	
MUXP6A2 (Bit4)	MUXP6A1 (Bit3)	MUXP6A0 (Bit2)	IGATE6 (Bit6)	
MUXP7A2 (Bit7)	MUXP7A1 (Bit6)	MUXP7A0 (Bit5)	IGATE7 (Bit7)	
MUXP8A2 (Bit10)	MUXP8A1 (Bit9)	MUXP8A0 (Bit8)	IGATE8 (Bit8)	
MUXP9A2 (Bit13)	MUXP9A1 (Bit12)	MUXP9A0 (Bit11)	IGATE9 (Bit9)	
MUXP10A2 (Bit0)	MUXP10A1 (Bit15)	MUXP10A0 (Bit14)	IGATE10 (Bit10)	
MUXP11A2 (Bit3)	MUXP11A1 (Bit2)	MUXP11A0 (Bit1)	IGATE11 (Bit11)	
MUXP12A2 (Bit6)	MUXP12A1 (Bit5)	MUXP12A0 (Bit4)	IGATE12 (Bit12)	
MUXP13A2 (Bit9)	MUXP13A1 (Bit8)	MUXP13A0 (Bit7)	IGATE13 (Bit13)	
MUXP14A2 (Bit12)	MUXP14A1 (Bit11)	MUXP14A0 (Bit10)	IGATE14 (Bit14)	
MUXP15A2 (Bit15)	MUXP15A1 (Bit14)	MUXP15A0 (Bit13)	IGATE15 (Bit15)	

A2	A1	A0	IGATE	IRQ
0	0	0	1	10
0	0	1	1	11
0	1	0	1	12
0	1	1	1	15
1	0	0	1	2
1	0	1	1	7
1	1	0	1	5
1	1	1	1	3

Table 3.7a: Mux Table for setting IRQs for Opto-Isolators

Bits 2-4: MUXP6A0 to MUXP6A2 - These bits are used to set up an IRQ line for the Opto-isolator 6 (PA6). Bits 2 to 4 sets the IRQ selection for Opto-Isolator 6, with IGATE6 enabling/disable interrupt support. IGATE6 must be enabled in order to select an interrupt. Table 3.6a gives an example of the appropriate writes from

Bits 2 to 4 to select 1 of 8 IRQs. Bit 2 is Address Decode A0, Bit 3 is Address Decode A1, Bit 4 is Address Decode A2 and Gx is IGATE6.

Reading these bits determines the status of MUXP1A0 to MUXP1A2 bits.

Bits 5-7: MUXP7A0 to MUXP7A2 - These bits are used to set up an IRQ line for the Opto-isolator 7 (PA7). Bits 5 to 7 set the IRQ selection for Opto-Isolator 7, with IGATE7 enabling/disable interrupt support. IGATE7 must be enabled in order to select an interrupt. Table 3.6a gives an example of the appropriate writes from Bits 5 to 7 to select 1 of 8 IRQs. Bit 5 is Address Decode A0, Bit 6 is Address Decode A1, Bit 7 is Address Decode A2 and Gx is IGATE7.

Reading these bits determines the status of MUXP7A0 to MUXP7A2.

Bits 8-10: MUXP8A0 to MUXP8A2 - These bits are used to set up an IRQ line for the Opto-isolator 8 (PA8). Bits 8 to 10 sets the IRQ selection for Opto-Isolator 8, with IGATE8 enabling/disable interrupt support. IGATE8 must be enabled in order to select an interrupt. Table 3.6a gives an example of the appropriate writes from Bits 8 to 10 to select 1 of 8 IRQs. Bit 8 is Address Decode A0, Bit 9 is Address Decode A1, Bit 10 is Address Decode A2 and Gx is IGATE8.

Reading these bits determines the status of MUXP8A0 to MUXP8A2.

Bits 11-13: MUXP9A0 to MUXP9A2 - These bits are used to set up an IRQ line for the Opto-isolator 9 (PA9). Bits 11 to 13 sets the IRQ selection for Opto-Isolator 9, with IGATE9 enabling/disable interrupt support. IGATE9 must be enabled in order to select an interrupt. Table 3.6a gives an example of the appropriate writes from Bits 11 to 13 to select 1 of 8 IRQs. Bit 11 is Address Decode A0, Bit 12 is Address Decode A1, Bit 13 is Address Decode A2 and Gx is IGATE9.

Reading these bits determines the status of MUXP4A0 to MUXP4A2.

Bits 14-15: MUXP10A0 to MUXP10A1- These bits in conjunction with bits 0 in the IMUXP2 Register are used to set up an IRQ line for the Opto-isolator 10 (PA10). MUXP10A0 (in the IMUXP1 Register), MUXP10A1 (in the IMUXP1 Register) and MUXP10A2 (in the IMUXP2 Register) sets the IRQ selection for Opto-Isolator 10, with IGATE10 enabling/disable interrupt support. IGATE10 must be enabled in order to select an interrupt. Table 3.7a gives an example of the appropriate writes from Bits 14 in the IMUXP1 Register, Bit 15 in the IMUXP1 Register and Bit 0 in the IMUXP2 Register in order to select 1 of 8 IRQs. Bit 14 is Address Decode A0 (in the IMUXP1 Register), Bit 15 (in the IMUXP1 Register) is Address Decode A1, Bit 0 (IMUXP2 Register) is Address Decode A2 and Gx is IGATE10.

Reading these bits determines the status of MUXP10A0 and MUXP10A1.

3.8) IMUXP2 – Local Mux Interrupt Control Register 3 (offset 14, read/write)

This register is used to set individual interrupts for each optically isolated input. Effectively MUXP2 is used as address lines to map each optically isolated inputs to a specific IRQ. If any one of the Opto-isolators was enabled, the pulse is set up and vectored to the Decoder to a specific IRQ. This register configures this line to any of 8 IRQs lines.

IMUXP2 Register (write mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
MUXP15A2	MUXP15A1	MUXP15A0	MUXP14A2	MUXP14A1	MUXP14A0	MUXP13A2	MUXP13A1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MUXP13A0	MUXP12A2	MUXP12A1	MUXP12A0	MUXP11A2	MUXP11A1	MUXP11A0	MUXP10A2

IMUXP2 Register (read mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
MUXP15A2	MUXP15A1	MUXP15A0	MUXP14A2	MUXP14A1	MUXP14A0	MUXP13A2	MUXP13A1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MUXP13A0	MUXP12A2	MUXP12A1	MUXP12A0	MUXP11A2	MUXP11A1	MUXP11A0	MUXP10A2

Bits 0: MUXP10A2 – This bit in conjunction with bits 14 and 15 in the IMUXP1 Register are used to set up an IRQ line for the Opto-isolator 10 (PA10). MUXP10A0 (in the IMUXP1 Register), MUXP10A1 (in the IMUXP1 Register) and MUXP10A2 (in the IMUXP2 Register) sets the IRQ selection for Opto-Isolator 10, with IGATE10 enabling/disable interrupt support. IGATE10 must be enabled in order to select an interrupt. Table 3.7a gives an example of the appropriate writes from Bits 14 in the IMUXP1 Register, Bit 15 in the IMUXP1 Register and Bit 0 in the IMUXP2 Register in order to select 1 of 8 IRQs. Bit 14 is Address Decode A0 (in the IMUXP1 Register), Bit 15 (in the IMUXP1 Register) is Address Decode A1, Bit 0 (IMUXP2 Register) is Address Decode A2 and Gx is IGATE10.

Reading this bit determines the status of the MUXP10A2 bit.

Bits 1-3: MUXP11A0 to MUXP11A2 - These bits are used to set up an IRQ line for the Opto-isolator 11 (PA11). Bits 1 to 3 sets the IRQ selection for Opto-Isolator 11, with IGATE11 enabling/disable interrupt support. IGATE11 must be enabled in order to select an interrupt. Table 3.7a gives an example of the appropriate writes from Bits 1 to 3 to select 1 of 8 IRQs. Bit 1 is Address Decode A0, Bit 2 is Address Decode A1, Bit 3 is Address Decode A2 and Gx is IGATE11.

Reading these bits determines the status of MUXP11A0 to MUXP11A2 bits.

Bits 4-6: MUXP12A0 to MUXP12A2 - These bits are used to set up an IRQ line for the Opto-isolator 12 (PA12). Bits 4 to 6 set the IRQ selection for Opto-Isolator 12, with IGATE12 enabling/disable interrupt support. IGATE12 must be enabled in order to select an interrupt. Table 3.7a gives an example of the appropriate writes from Bits 4 to 6 to select 1 of 8 IRQs. Bit 4 is Address Decode A0, Bit 5 is Address Decode A1, Bit 6 is Address Decode A2 and Gx is IGATE12.

Reading these bits determines the status of MUXP12A0 to MUXP12A2.

Bits 7-9: MUXP13A0 to MUXP13A2 - These bits are used to set up an IRQ line for the Opto-isolator 13 (PA13). Bits 7 to 9 sets the IRQ selection for Opto-Isolator 13, with IGATE13 enabling/disable interrupt support. IGATE13 must be enabled in order to select an interrupt. Table 3.7a gives an example of the appropriate writes from Bits 7 to 9 to select 1 of 8 IRQs. Bit 7 is Address Decode A0, Bit 8 is Address Decode A1, Bit 9 is Address Decode A2 and Gx is IGATE13.

Reading these bits determines the status of MUXP13A0 to MUXP13A2.

Bits 10-12: MUXP14A0 to MUXP14A2 - These bits are used to set up an IRQ line for the Opto-isolator 14 (PA14). Bits 10 to 12 sets the IRQ selection for Opto-Isolator 14, with IGATE14 enabling/disable interrupt support. IGATE14 must be enabled in order to select an interrupt. Table 3.7a gives an example of the appropriate writes from Bits 10 to 12 to select 1 of 8 IRQs. Bit 10 is Address Decode A0, Bit 11 is Address Decode A1, Bit 12 is Address Decode A2 and Gx is IGATE14.

Reading these bits determines the status of MUXP14A0 to MUXP14A2.

Bits 13-15: MUXP15A0 to MUXP15A2- These bits are used to set up an IRQ line for the Opto-isolator 15 (PA15). Bits 13 to 15 set the IRQ selection for Opto-Isolator 15, with IGATE15 enabling/disable interrupt support. IGATE15 must be enabled in order to select an interrupt. Table 3.7a gives an example of the appropriate writes from Bits 13 to 15 to select 1 of 8 IRQs. Bit 13 is Address Decode A0, Bit 14 is Address Decode A1, Bit 15 is Address Decode A2 and Gx is IGATE15.

Reading these bits determines the status of MUXP15A0 to MUXP15A2.

3.9) ISETX – Interrupt Set/Reset Register (offset 18, read / write)

This register is used to determine whether a positive level shift did occur in any one of the Opto-Isolators when using Normal Interrupt share mode. The register is also used to reset any of the flip-flops that was set by Opto-Isolator 0 to 16. 16 bit read to these registers are recommended.

ISETX Register (read mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PBY7	PBY6	PBY5	PBY4	PBY3	PBY2	PBY1	PBY0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAY7	PAY6	PAY5	PAY4	PAY3	PAY2	PAY1	PAY0

ISETX Register (write mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
RESP15	RESP14	RESP13	RESP12	RESP11	RESP10	RESP9	RESP8

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESP7	RESP6	RESP5	RESP4	RESP3	RESP2	RESP1	RESP0

Bits 0-7: PAY0 to PAY7 - These bits determine whether a positive edge has occurred in any of the low order (D0 to D7) Opto-isolators Inputs. If a high is detected on any of the bits then a positive transition has occurred on that opto-isolator. If one of the bits is set, it can result in an interrupt occuring if the IGATE0 to IGATE7 Bits (ie: Bits 0 to 7 for Opto-isolator 0 to 7) in the IGATE Register (offset 6) are enabled. You can clear the PAX0 to PAX7 registers by writing a 0 and then a 1 to the RESP0 to RESP7 bit respectively.

Bits 8-15: PBX0 to PBX7 - These bits determine whether a positive edge has occurred in any of the high order (D8 to D15) Opto-isolators Inputs. If a high is detected on any of the bits then a positive transition has occurred on that opto-isolator. If one of the bits is set, it can result in an interrupt occuring if the IGATE8 to IGATE15 Bits (ie: Bits 8 to 15 for Opto-isolator 8 to 15) in the IGATE Register (offset 6) are enabled. You can clear the PBX0 to PBX7 registers by writing a 0 and then a 1 to the RESP8 to RESP15 bit respectively.

3.10) DIO – Digital I/O Register (offset 20, read / write)

This register is used to read and write to the digital I/O lines available on the External Digital I/O Connector. Any compatible TTL Voltage can be fed into the digital input lines (DI0-DI15) and read back using this register. When this register is written to, the voltages on the Digital Output line will reflect the bit settings. The digital outputs are open collector and can source 20mA.

DIO Register (read mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

Bits 0-7: DI0 to DI7 - These bits are available on the digital I/O connector on the PC62C Board. Any TTL compatible voltage can be fed into these lines and read back to determine it status. If the voltage on the digital I/O connector is less than 0.6V then a logical 0 will be read back. If the voltage is > 2V but less than 5.1V then a logical 1 will be read back.

Bits 8-15: DI8 to DI15 - These bits are available on the digital I/O connector on the PC62C Board. Any TTL compatible voltage can be fed into these lines and read back to determine it status. If the voltage on the digital I/O connector is less than 0.6V then a logical 0 will be read back. If the voltage is > 2V but less than 5.1V then a logical 1 will be read back.

DIO Register (write mode)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

Bits 0-7: DO0 to DO7 – These 8 bits are available on the digital I/O connector on the PC62C Board. When this register is written to, the voltages on the low order Digital Output lines (D0 – D7) will reflect the appropriate bit settings. The digital outputs are TTL Compatible with open collector outputs and can source 20mA.

Bits 8-15: DO8 to DO15 - These 8 bits are available on the digital I/O connector on the PC62C Board. When this register is written to, the voltages on the high byte Digital Output lines (D8 – D15) will reflect the appropriate bit settings. The digital outputs are TTL Compatible with open collector outputs and can source 20mA.

Warning

Do not exceed the min/max voltage specification fed into the digital input lines. The absolute minimum voltage is –0.1V and the absolute maximum voltage is 5.2V. Exceeding the above specifications will damage the PC62C.

3.11) OPTORD1 - Optically Isolated Input Port Register 1 (offset 22, read only)

The register allows one to read the status of Opto Isolator 16 to 31. It is only valid when the expansion board (PC62C-EXP16) is connected to the PC62C. The Register structure is described below.

OPTORD1 Register (read only)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Bit 0 to 7: The bits PC0 to PC7 reflect the status of optically isolated input lines 15 to 23. This register is only valid if the expansion board is connected to the PC62C

Bit 8 to 15: The bits PC8 to PC15 reflect the status of optically isolated input lines 24 to 31. This register is only valid if the expansion board is connected to the PC62C.

It is recommended that a 16 bit read is initiated when reading the status of the Port. Note, however, that two 8 bit reads can also be performed. This feature was included in order to maintain compatibility with the PC62B.

3.12) OPTORD2 - Optically Isolated Input Port Register 2 (offset 24, read only)

The register allows one to read the status of Opto Isolator 31 to 47. It is only valid when the expansion board (PC62C-EXP32) is connected to the PC62C. The Register structure is described below.

OPTORD2 Register (read only)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Bit 0 to 7: The bits PD0 to PD7 reflect the status of optically isolated input lines 32 to 39. This register is only valid if the expansion board is connected to the PC62C

Bit 8 to 15: The bits PD8 to PD15 reflect the status of optically isolated input lines 40 to 47. This register is only valid if the expansion board is connected to the PC62C.

It is recommended that a 16 bit read is initiated when reading the status of the Port. Note, however, that two 8 bit reads can also be performed. This feature was included in order to maintain compatibility with the PC62B.

3.13) OPTORD3 - Optically Isolated Input Port Register 3 (offset 26, read only)

The register allows one to read the status of Opto Isolator 48 to 63. It is only valid when the expansion board (PC62C-EXP32) is connected to the PC62C. The Register structure is described below.

OPTORD3 Register (read only)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0

Bit 0 to 7: The bits PE0 to PE7 reflect the status of optically isolated input lines 48 to 55. This register is only valid if the expansion board is connected to the PC62C

Bit 8 to 15: The bits PE8 to PE15 reflect the status of optically isolated input lines 56 to 63. This register is only valid if the expansion board is connected to the PC62C.

It is recommended that a 16 bit read is initiated when reading the status of the Port. Note, however, that two 8 bit reads can also be performed. This feature was included in order to maintain compatibility with the PC62B.

Chapter 4: Programming Guide

4.0) Introduction

This chapter describes programming the PC 62C at its lowest level. In order to accomplish this, detailed knowledge of chapter 4 and the system hardware is required.

As an alternative to low level programming, driver software is provided with the PC 62C. This is described in Chapter 5.

The advantages of using the driver software are:

a) Detailed knowledge of the PC 62C is not required.
b) The Driver Libraries supports multiple boards. In other words, you can cascade boards in the same computer.
c) The Driver Library is callable from most high level languages.

Programmers who need to incorporate special routines into their application will need to read this chapter. Examples are application programs written in Clarion, Clipper, etc.

Once the PC 62C has been installed into the computer and external connections are made, the board is in an operational state. The PC 62C occupies 32 consecutive Word I/O addresses starting from the board's base address. The base address is set by the DIP Switch on the PC 62C. Programming the PC 62C is done by using input/output instructions in assembly or any other programming language. Reading and writing to these addresses allows data to be moved to and from the PC 62C.

Reading and writing to these ports are normally 16 bit wide. 8 bit Wide Read/Write is also supported but not recommended. Reading and Writing typically takes on the form of one of the following instructions:

Language	Port Read	Port Write	
'C'	value = inp(addre);	outp(addre, value);	(8 bit Read/Write)
	value1 = inpw(addre);	outpw(addre, value1);	(16 bit Read/Write)
'Pascal'	value := port[addre];	port[addre] := value;	(8 bit Read/Write)
	Value1 := portw[addre];	portw[addre] := value1;	(16 bit Read/Write)

'**Assembly'**	mov al, value
	mov dx, addre
	in al, dx
		mov al, value
		mov dx, addre
		out dx, al
			(8 bit Read/Write)

	mov ax, value1
	mov dx, addre
	in ax, dx
		mov ax, value1
		mov dx, addre
		out dx, ax
			(16 bit Read/Write)

where: addre is the I/O location of the PC 62C registers
value is the byte read or written to the register
value1 is the word read or written to the register

4.1) Initialising the PC62C

The PC62C board should be initialised before accessing any data from the Board. To maintain compatibility with the PC62B, the following initialization routine should be done.

a) Write a zero to the IGATE Register (offset 6)
b) Write a zero to the GLMUX Register (offset 4)
c) Write a zero to the GLOBAL Register (offset 2)

Note that the above registers default to zero upon powerup. However, it is important that the above should be initiated to ensure proper operation.

4.2) Reading the Opto-Isolators using Polled I/O

If standard polling on the opto-isolators is required, it can be done as follows:

a) Disable Normal Interrupt Mode by writing a zero to the IGATE Register (offset 6).
b) Disable Global Interrupt Mode by write a zero to the GLMUX Register (offset 4).
c) Disable the MUX control lines by write a zero to the GLOBAL Register (offset 2).
d) Initiate a read on the OPTORD Register.
e) Repeat cycle from d).

4.3) Configuring the Opto-Isolators using Shared Interrupt Mode

Each Opto-isolator can be configured to used an Interrupt Line. However, since only 8 IRQ Lines are available, interrupt sharing should be used. The Global Status Register should be initialised in order to map a positive level shift to an IRQ Line. The 16 Opto-Isolators are divided into the low order 8 and a high order 8. The first 8 lines will then be mapped to a single shared IRQ line while the last eight lines mapped to another single shared IRQ Line. The reason for the division is to prioritise the first 8 lines and the last 8 lines. The Procedure is as follows:

a) Write C0h to the GLCNTRL Register.
b) Write F4h to the GLCNTRL Register (Set sets up IRQ2 for the first 8 Opto-Isolators and IRQ5 for the high order (D8 to D15) Opto Isolators.
c) Setup an ISR for IRQx and IRQy (in this example it is 2 and 5)
d) When a positive edge is seen on one of the Opto-isolators, an interrupt will be generated (either in the first eight or the last 8).
e) An ISR should check which opto-isolator has changed state by reading the GBUF Register (using one single 16 bit read).
f) After determining which opto-isolator has changed state, proceed with the necessary action.
g) If any other opto-isolator has changed state (after reading the GBUF register) proceed with the necessary action.
h) Clear the Interrupt Enable flip-flops after all the necessary action is taken. You can clear either each individual flip-flips by writing to the ISETX Register (Offset or reset the first eight or last 8 flip-flops by writing a 0 and then a 1 to the GRES0 (bit 0) or GRES1 (bit1) in the GLOBAL Register (Offset 2).
i) Issue an End of Interrupt (EOI) command to the Interrupt controller. Note that an EOI command must be issued to both Interrupt Controllers.
j) Repeat the above cycle from e) to i).

Warning

Do not configure both IRQ MUXes in the GLCNTRL Register to the same Interrupt. This will lead to two open collector lines driving each other and can yield inexplicable results.

4.4) Configuring the Opto-Isolators using Normal Interrupt Mode

Each Opto-isolator can be configured to an Interrupt Line. However, since only 8 IRQ Lines are available, only eight can be vectored to an individual IRQ. The rest can be vectored to one common IRQ line using Shared IRQ Mode (see section 4.2). To configure the IRQ lines proceed as follows:

a) Set the appropriate bit for each opto-isolator (max 8 at any one time) in the IGATE Register.
b) Select the appropriate IRQ by writing to IMUXP0, IMUXP1 and IMUXP2.
c) Setup an ISR for each IRQ
d) When a positive edge is seen on one of the Opto-isolators, an interrupt will be generated.
e) An ISR should take the necessary action.
f) Clear the Interrupt Enable flip-flops after all the necessary action is taken. You can clear either each individual flip-flips by writing to the ISETX Register (Offset or reset the first eight or last 8 flip-flops by writing a 0 and then a 1 to the GRES0 (bit 0) or GRES1 (bit1) in the GLOBAL Register (Offset 2).
g) Issue an End of Interrupt (EOI) command to the Interrupt controller. Note that an EOI command must be issued to both Interrupt controllers.
h) Repeat the above cycle from d) to g).

Warning

Do not configure both IRQ MUXes in the GLCNTRL Register and the IMUXP0, IMUXP1, IMUXP2 to the same Interrupt. This will lead to two open collector lines driving each other and can yield inexplicable results.

4.5) Reading the Digital I/O Lines

There are 16 TTL compatible Digital Inputs and 16 TTL compatible Digital Outputs on the PC62C. These can be read and written too using the DIO Register (offset 20).

A Pascal example of how to read and write to the digital ports is given below:

```
Program Digitaltest(Input, Output);

{ This program test the digital input and output lines. On the PC62C
connector, connect the digital input lines [DIN0 to DIN15] to the
Digital Output Lines [DOUT0 to DOUT15] respectively. The aim is to
write a value from 1 to 65535 and read it back using the Digital
Input Lines. If an error occur during the read or write, a 'failure'
message will be displayed else a 'pass' message will be displayed. }

VAR   I, j, k        : longint;
      Count, dummy   : longint;

Begin

Count := 10;         { Repeat test 10 times }

for i := 1 to count do              { external digital I/O test }
  begin
k := 0;
   error := 0;    { initialise error count to 0 }

   for k := 1 to 65535 do
     begin
       portw[ba+20] := k;      { write to the digital output lines
       dummy := portw[ba+20];  { read these lines back }
       if dummy <> k then      { verify if they correspond }
         begin           { If not then increment the error count }
           error := error + 1;
         end;   { Digital I/O compare }
     end;
   if error <> 0 then     {If error detected then display failure}
      begin
       gotoxy(10,10)
       write('Digital I/O Test Fail: ', error);
      end
      else begin     {If no error was detected the display pass }
            gotoxy(10,10)
            write('Digital I/O Test Pass: ', error);
           end;
  end;     { test count to 10 }
end.       { End Program }
```

Chapter 5: Driver Software

Full driver software is supplied with the PC 62C package. Full details are explained in the EDR Software developers kit User Manual. A summary of the drivers is explained below.

For the latest update Driver software and technical information, see our WebSite: http://www.eagle.co.za

Both DOS and Windows Languages are supported: They are:

DOS Languages:

Borland C/C++ Version 3.1 or 4.0
Microsoft C/C++ Version 6.0 or 7.0
Borland Pascal / Turbo Pascal Version 6.0 or 7.0
Microsoft QuickBasic Version 4.5

Windows Languages:

Delphi V1.00 / V2.00 / V3.00
Borland C/C++ 3.1 or 4.0
Microsoft C/C++ 6.0 or 7.0
Borland Pascal / Turbo Pascal Version 6.0 or 7.0
Visual Basic V1.00 thru V5.00

5.1) Board Handles

All EDR functions used above require a board handle as the first parameter. The board handle defines which board is affected by the function call. Using this method has several advantages, For example, there is no need for a 'select board' function; working with parallel boards is much easier; different applications using the EDR at the same time will not conflict with each other.

Board handles are integers obtained by calling EDR_AllocBoardHandle (see 7.2 of EDR Developers Toolkit). Once allocated a board handle must be initialised to the PC 62C before it can be accessed. This is achieved by calling EDR_InitBoard or EDR_InitBoardType (see 7.5 of EDR manual) with the base address or EDR_loadConfiguration (see section 7.8 of EDR manual).

EDR_InitBoard will attempt to detect the PC 62C at the base address specified.

5.2) Interrupt functions

The Opto-Isolator lines are connected to a latch and fed into the IRQ line if normal or Shared Interrupt Mode (or both) is used. An ISR can be installed using the EDR driver functions to service these lines when pulses toggles the Opto Isolator line + Opto-Isolator Line Return. Note that all the lines are latched. If any of the opto-isolator lines are vectored to the PC's Interrupt System, the latches should be cleared in the ISR.

These functions are callable from virtually any programming language. See the EDR Software Developers Kit User Manual.

5.3) Quick Function Reference

The PC 62C Enhanced Interrupt Driven Optically Isolated Input Board which utilises the following functions calls contained in the EDR driver developers toolkit. They are:

Function Name	Description
EDR_DIOConfigurePort	Configures a digital port for a particular mode and direction. EDR only directly supports mode 0 (EDR_DIO_SIMPLE) with the driver functions. Other modes can be be used but you will need to write your own support code.
EDR_DIOLineInput	Gets the status of a single line (bit) in a digital input port. If the port is an output port then the last value written to the line (bit) is returned.
EDR_DIOLineOutput	Changes a single line (bit) in a digital output port.
EDR_DIOPortOutput	Writes a byte of data to the PC 62C I/O port
EDR_DIOPortInput	Reads a byte of data from the PC 62C I/O Port. If the port is an output port then the last value written to the port is returned.
EDR_HasDOReadback	Indicates if a particular board type's digital output ports can be read back or not. If the board supports readback from DO ports then doing EDR_DIOPortInput or EDR_DIOLineInput on an output port will read the last value written to the port from a board register. If the readback is not supported the EDR returns its software copy of the last value written using EDR_DIOPortOutput or EDR_DIOLineOutput.
EDR_EnableInterrupt	Enables or disables the specified interrupt on the PC 62C. Note that this just programs the board registers (ie: writing to IEN0 and IEN1 Registers) so that it will/will not generate the interrupt. If the interrupt is masked then interrupts from the board will be blocked. Disabling interrupts or enabling interrupts when they are already enabled may generate extra interrupts. Make sure that your ISR are prepared to handle these rogue interrupts.
EDR_InstallISR	Installs an ISR for the specified hardware interrupt request

Function Name	Description
EDR_UninstallISR	Removes an interrupt service routine that was installed with EDR_InstallISR
EDR_InstallBoardISR	Installs an ISR for a particular type of interrupt installed on the PC 62C.
EDR_UninstallBoardISR	Removes an interrupt service routine that was installed with EDR_InstallBoardISR
EDR_MaskIRQ	Masks or unmasks a particular IRQ level
EDR_MaskBoardIRQ	Masks or unmasks a particular board interrupt
EDR_ResetInterrupt	Resets an interrupt latch on the PC 62C and sends an EOI command to one of the PCs interrupt controllers on completion of the interrupt
EDR_AllocBoardHandle	Allocates a new board handle to the PC 62C. If no board handles are available then a 0 is returned. This is particularly useful is multiple PC 62C are present in the same.computer.
EDR_FreeBoardHandle	Releases a board handle allocated to the PC 62C making it available to any other PC card
EDR_InitBoardType	Initialises a board and allocates a board handle to it
EDR_ConfigDialog	Diplays a dialog box that allows the user to manually configure the driver for the Board in the computer
EDR_SaveConfiguration	Function writes configuration information to a file for later loading with EDR_LoadConfiguration
EDR_LoadConfiguration	Loads details of the Cards configuration from the file created by EDR_SaveConfiguration
EDR_RestoreDefaults	Restores factory default configuration for a baord attached to a handle
EDR_IsBaseAddressInUse	Checks if any board initialised with EDR is using the specified I/O address
EDR_DetectBoard	Tries to determine the type of board present at a specified I/O address.
EDR_SetBoardType	Changes the board type attached to a board handle
EDR_SetIRQLevel	Set the IRQ level EDR will use for the interrupt ID specified.
EDR_NumDIOPorts	Gets the number of DIO ports a board has.
EDR_ValidDIOPortConfig	Checks the configuration of a digital port.
EDR_ValidInterruptID	Checks to see if the board supports the ID specified
EDR_ValidIRQLevel	Checks an IRQ level

Chapter 6: Testing the PC 62C

Before attempting to interface the PC 62C with your application, it is essential that you test the board first. This is done using the following procedure:

6.1) Testing the PC 62C Board

Install the PC 62C using the procedure described in the Chapter 2: Installation. Proceed as follows:

a) Make a test loom by connecting the digital outputs [DO0-DO15] to the Digital Inputs [DI0-DI15]. Also connect the Digital Outputs [DO0-D15] to the optically isolated inputs [PA0-7] to [DO0-DO7] and [PB0-7] to [DO8-DO15] respectively. All the return lines should be connected to GND on the digital I/O connector. COMA and COMB should be connected to GND on the DB37 Connector.

b) Switch the Computer on

c) On the DOS prompt, go to the C:\EDR\TPAS\DEMOS\ sub-directory

d) Run the 62CTEST.EXE Test program.

If an error message 'Board not found' appear on your screen then the PC 62C was not installed at that address. Try a different base address as specified in Apendix A (eg: 700h) and re-run the test S/W. If the problem persists then try increasing the wait states on the PC 62C Board and re-run test software. The board should work.

If the PC 62C is found, a message will appear on the screen: 'PC 62C Board found'. The program comprehensively tests the register structure and each optically isolated input line. You may feed any voltage on the optically isolated input lines up to a maximum of 24V. Any TTL signals can be fed into the digital I/O lines.

6.2) Connecting Normally Open devices to the Digital Input Lines

When connecting switches, etc, to the Digital Inputs of the PC62C, it is important to ensure that the inputs are set to a defined state at all times. Figure 6.2 gives an example.

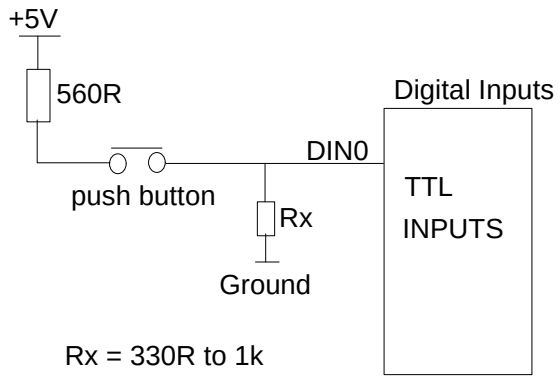


Figure 6.2: Connecting Normally Open devices to the Digital Inputs

Figure 6.2 gives an example of how to connect a push button to one of the Digital Input lines on Connector J6. We assume that when the Push button is closed, the Port line will go high (logic 1 = +5V). When the push button is not closed, the port line should be low. However, many Users do not connect the 'pull-down' resistor to the port line. If this is not done, the port line will be in a floating state and can hence yield either a high or a low.

Thus you must ensure that the port line is always connected which is done via a resistor network.

Chapter 7: Troubleshooting

Problem: 'Board not found' message appears on the screen when running test software.

Solution: Another I/O card might be using the same base address location as the PC 62C. Try a different base address other than the manufacturer's default base address (eg: 700h) and re-run test software 62CTEST.EXE found in sub directory C:\EDR\TPAS\DEMOS\. If the problem persists then try increasing the wait states on the PC 62C. If the PC 62C still does not work even after the maximum number of wait states was chosen then try a different computer with a different motherboard. If the test still fails then the PC 62C is faulty. Return the board to your distributor for repairs.

Problem: Data written to the digital Output Register does not set the output ports correctly.

Solution: Check the ports using the walkbit test program called WALKBIT.EXE found in EDR\TPAS\DEMOS subdirectory. Monitor the digital lines of on connector J6 and check if the problem persists. If so, then the Digital Output Latches might be faulty. Please send the PC 62C back to your distributor for repairs.

Problem: I connected a push button to one of the input port lines. When it is closed it is set to +5V (yield a logical 1) and the program reads a logical 1. However, when it is open, random numbers are read by the program on the digital input lines.

Solution: When the push button is not connected, the port line is in a floating (not connected). You must connect a 'pulldown' resistor (experiment from 330R to 1k) to the port line in order to ensure that it is in a defined state. Also note that if a port is configured as an input then all unused lines MUST be grounded. See Section 6.2 for more details.

Problem: Interrupts does not occur when any of Opto-Isolators receives a pulse from 0V to above the threshold of 3.1V. In other words, a square pulse Posituve edged 0 to 24V does not yield an interrupt.

Solution: It is possible that the Opto-isolator was not configured in Interrupt Mode. First read back the IGATE Register [Base + 6] and check if the appropriate Interrupt Enable Bit was set. For example, if an IRQ does not occur on Opto isolator 0, check if bit 0 was enabled. If not, set it to 1. Next, configure the IRQ to any of 8 using the IMUXP0 Register (Bits 0 to 2). Re-trigger the Opto-isolator. An IRQ should occur.

Don’t forget to reset the Interrupt Flip Flops after an IRQ has occurred on a particular Opto-isolator. A Reset should be done by writing a 0 and then a 1 to the ISETX Register (Offset 18) to the appropriate Opto-Isolators Interrupt Enable flip-flop.

Warning

Any parts replaced on the PC 62C must be done by a qualified or trained technician. If you (the user) is not a trained technician then rather return the board to your distributor for repairs explaining in detail what the problem is.

If you cannot solve the problem then simply call your distributor for immediate help.

Chapter 8: Repair Service

The PC 62C is guaranteed for a period of 1 year. If the board is faulty within this period, we will gladly repair it free of charge provided that the maximum specification was not exceeded. If any burn't tracks are seen on the PC 62C Board, warranty will be void. A repair charge will be levied in the user requires the board to be repaired.

Before sending the board to your distributor for repairs, ensure that you go through Chapter 7: TroubleShooting Hints thoroughly. If, after you have gone through this Chapter, the board still does not work, return it for repairs stating in detail what the problem is.

Our repair service centre will be available to repair our products even after the 1 year warranty. A small service fee will be levied which usually covers the cost of the components that are faulty.

Specifications

Computer Host Interface

Base Address:	Switchable from 0 to 17FFh on 32 Word boundaries
Bus Type:	AT, ISA or EISA
I/O Wait States:	0, 2, 4, or 8 Jumper selectable.
Number of Registers:	Thirty Two 16-bit Registers
Word size:	16 bits
Word transfer Rate:	10Mhz max (depends on computer and program)
Interrupts:	Software selectable from IRQ2, 3, 7, 10, 11, 12, 15

Optically Isolated Inputs

Input voltage:	0 to 3V	logical low
	3.1V to 24V	logical high
Max reverse voltage:	400V peak	
Max input current:	1A peak 30mA continuous	

LED:

Forward Voltage:	1.15V (typ), 1.5V (max) [I_f =10mA]
Reverse Current:	100µA (max) [V_r = 3V]
Capacitance:	30pF (typ) [V=0, f=1MHz]

Photo Transistor:

DC Forward Current Gain:	200 (typ) [V_{ce}=5V, I_c=500µA]
C-E Breakdown Voltage:	30V (min) [I_c=1mA, I_f = 0]
E-B Breakdown Voltage:	70V (min) [I_c=500µA]
E-C Breakdown Voltage:	7V (min) [I_e=100µA]
Collector Dark Current:	1nA (typ), 50nA (max) [V_{ce}=10V]

Coupled:

Current Transfer Ratio:	20% (min), 100% (typ) [I_f =10mA, V_{ce}=10V]
C-E Saturation Voltage:	0.1V (typ), 0.5V (max) [I_f =50mA, I_c=2mA]
Capacitance Input to Output:	0.8pF [V_s=0V, f=1MHz]
Isolation Resistance:	$10^{11}\Omega$ [V_s=500V]
Isolation Voltage:	2500Vrms [VAC, 1 minute] (Toshiba)
Rise/Fall time:	2µs [V_{ce}=10V, I_{cb}=50µA, R_l=100Ω]

Signal frequency response:	10kHz
Interrupt link:	Sofware selectable from IRQ2, 3, 7, 10, 11, 12, 15

Digital Inputs/Outputs

Number of lines:	16 Input and 16 Output Lines	
Compatibilty:	TTL	
Input Voltage:	Logical Low:	0.1V to 0.8V
	Logical High:	2V to 5V
Output Voltage:	Logic 0:	0.45V max
	Logic 1:	2.4V min
Output Current:	Low State (V_{OH}):	24mA max
	High State (V_{OL}):	-2.6mA max
Max Darlington drive current:	24mA on each Output line	

Absolute Maximum TTL Inputs

Absolute Max Input voltage:	5.4V*
Absolute Min Input voltage:	-0.2V*

Warning

Stresses greater than listed above may cause permanent damage to the PC 62C. This stress rating only applies to the PC 62C at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. We do not recommend exposure to absolute maximum ratings.

I/O Connector

Opto-Isolator Input Connector:	37 D-type Male
Digital I/O Connector:	40 way IDC header
Max User +5V current:	250mA (at I/O connector)
Max User +12V current:	250mA (at I/O connector)

Enviromental

Operating temperature:	0°C to 55°C
Storage temperature:	-55°C to 150°C
Relative humidity:	5% to 90% non-condensing
PC Board size:	181mm x 115mm (including edge connector)

Power Supply Requirements

+5V Supply:	*:*	150mA typ (excludes +5V power for User Interfacing)

Appendix A (Base Address Settings)

Base Address Switch Settings

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
00	ON	ON	ON	ON	ON	ON	ON	ON	00
20	ON	ON	ON	ON	ON	ON	ON	OFF	20
40	ON	ON	ON	ON	ON	ON	OFF	ON	40
60	ON	ON	ON	ON	ON	ON	OFF	OFF	60
80	ON	ON	ON	ON	ON	OFF	ON	ON	80
A0	ON	ON	ON	ON	ON	OFF	ON	OFF	A0
C0	ON	ON	ON	ON	ON	OFF	OFF	ON	C0
E0	ON	ON	ON	ON	ON	OFF	OFF	OFF	E0
100	ON	ON	ON	ON	OFF	ON	ON	ON	100
120	ON	ON	ON	ON	OFF	ON	ON	OFF	120
140	ON	ON	ON	ON	OFF	ON	OFF	ON	140
160	ON	ON	ON	ON	OFF	ON	OFF	OFF	160
180	ON	ON	ON	ON	OFF	OFF	ON	ON	180
1A0	ON	ON	ON	ON	OFF	OFF	ON	OFF	1A0
1C0	ON	ON	ON	ON	OFF	OFF	OFF	ON	1C0
1E0	ON	ON	ON	ON	OFF	OFF	OFF	OFF	1E0
200	ON	ON	ON	OFF	ON	ON	ON	ON	200
220	ON	ON	ON	OFF	ON	ON	ON	OFF	220
240	ON	ON	ON	OFF	ON	ON	OFF	ON	240
260	ON	ON	ON	OFF	ON	ON	OFF	OFF	260
280	ON	ON	ON	OFF	ON	OFF	ON	ON	280
2A0	ON	ON	ON	OFF	ON	OFF	ON	OFF	2A0
2C0	ON	ON	ON	OFF	ON	OFF	OFF	ON	2C0
2E0	ON	ON	ON	OFF	ON	OFF	OFF	OFF	2E0
300	ON	ON	ON	OFF	OFF	ON	ON	ON	300
320	ON	ON	ON	OFF	OFF	ON	ON	OFF	320
340	ON	ON	ON	OFF	OFF	ON	OFF	ON	340
360	ON	ON	ON	OFF	OFF	ON	OFF	OFF	360
380	ON	ON	ON	OFF	OFF	OFF	ON	ON	380
3A0	ON	ON	ON	OFF	OFF	OFF	ON	OFF	3A0
3C0	ON	ON	ON	OFF	OFF	OFF	OFF	ON	3C0
3E0	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	3E0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
400	ON	ON	OFF	ON	ON	ON	ON	ON	400
420	ON	ON	OFF	ON	ON	ON	ON	OFF	420
440	ON	ON	OFF	ON	ON	ON	OFF	ON	440
460	ON	ON	OFF	ON	ON	ON	OFF	OFF	460
480	ON	ON	OFF	ON	ON	OFF	ON	ON	480
4A0	ON	ON	OFF	ON	ON	OFF	ON	OFF	4A0
4C0	ON	ON	OFF	ON	ON	OFF	OFF	ON	4C0
4E0	ON	ON	OFF	ON	ON	OFF	OFF	OFF	4E0
500	ON	ON	OFF	ON	OFF	ON	ON	ON	500
520	ON	ON	OFF	ON	OFF	ON	ON	OFF	520
540	ON	ON	OFF	ON	OFF	ON	OFF	ON	540
560	ON	ON	OFF	ON	OFF	ON	OFF	OFF	560
580	ON	ON	OFF	ON	OFF	OFF	ON	ON	580
5A0	ON	ON	OFF	ON	OFF	OFF	ON	OFF	5A0
5C0	ON	ON	OFF	ON	OFF	OFF	OFF	ON	5C0
5E0	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	5E0
600	ON	ON	OFF	OFF	ON	ON	ON	ON	600
620	ON	ON	OFF	OFF	ON	ON	ON	OFF	620
640	ON	ON	OFF	OFF	ON	ON	OFF	ON	640
660	ON	ON	OFF	OFF	ON	ON	OFF	OFF	660
680	ON	ON	OFF	OFF	ON	OFF	ON	ON	680
6A0	ON	ON	OFF	OFF	ON	OFF	ON	OFF	6A0
6C0	ON	ON	OFF	OFF	ON	OFF	OFF	ON	6C0
6E0	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	6E0
700	ON	ON	OFF	OFF	OFF	ON	ON	ON	700
720	ON	ON	OFF	OFF	OFF	ON	ON	OFF	720
740	ON	ON	OFF	OFF	OFF	ON	OFF	ON	740
760	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	760
780	ON	ON	OFF	OFF	OFF	OFF	ON	ON	780
7A0	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	7A0
7C0	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	7C0
7E0	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	7E0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
800	ON	OFF	ON	ON	ON	ON	ON	ON	800
820	ON	OFF	ON	ON	ON	ON	ON	OFF	820
840	ON	OFF	ON	ON	ON	ON	OFF	ON	840
860	ON	OFF	ON	ON	ON	ON	OFF	OFF	860
880	ON	OFF	ON	ON	ON	OFF	ON	ON	880
8A0	ON	OFF	ON	ON	ON	OFF	ON	OFF	8A0
8C0	ON	OFF	ON	ON	ON	OFF	OFF	ON	8C0
8E0	ON	OFF	ON	ON	ON	OFF	OFF	OFF	8E0
900	ON	OFF	ON	ON	OFF	ON	ON	ON	900
920	ON	OFF	ON	ON	OFF	ON	ON	OFF	920
940	ON	OFF	ON	ON	OFF	ON	OFF	ON	940
960	ON	OFF	ON	ON	OFF	ON	OFF	OFF	960
980	ON	OFF	ON	ON	OFF	OFF	ON	ON	980
9A0	ON	OFF	ON	ON	OFF	OFF	ON	OFF	9A0
9C0	ON	OFF	ON	ON	OFF	OFF	OFF	ON	9C0
9E0	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	9E0
A00	ON	OFF	ON	OFF	ON	ON	ON	ON	A00
A20	ON	OFF	ON	OFF	ON	ON	ON	OFF	A20
A40	ON	OFF	ON	OFF	ON	ON	OFF	ON	A40
A60	ON	OFF	ON	OFF	ON	ON	OFF	OFF	A60
A80	ON	OFF	ON	OFF	ON	OFF	ON	ON	A80
AA0	ON	OFF	ON	OFF	ON	OFF	ON	OFF	AA0
AC0	ON	OFF	ON	OFF	ON	OFF	OFF	ON	AC0
AE0	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	AE0
B00	ON	OFF	ON	OFF	OFF	ON	ON	ON	B00
B20	ON	OFF	ON	OFF	OFF	ON	ON	OFF	B20
B40	ON	OFF	ON	OFF	OFF	ON	OFF	ON	B40
B60	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	B60
B80	ON	OFF	ON	OFF	OFF	OFF	ON	ON	B80
BA0	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	BA0
BC0	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	BC0
BE0	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	BE0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
C00	ON	OFF	OFF	ON	ON	ON	ON	ON	C00
C20	ON	OFF	OFF	ON	ON	ON	ON	OFF	C20
C40	ON	OFF	OFF	ON	ON	ON	OFF	ON	C40
C60	ON	OFF	OFF	ON	ON	ON	OFF	OFF	C60
C80	ON	OFF	OFF	ON	ON	OFF	ON	ON	C80
CA0	ON	OFF	OFF	ON	ON	OFF	ON	OFF	CA0
CC0	ON	OFF	OFF	ON	ON	OFF	OFF	ON	CC0
CE0	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	CE0
D00	ON	OFF	OFF	ON	OFF	ON	ON	ON	D00
D20	ON	OFF	OFF	ON	OFF	ON	ON	OFF	D20
D40	ON	OFF	OFF	ON	OFF	ON	OFF	ON	D40
D60	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	D60
D80	ON	OFF	OFF	ON	OFF	OFF	ON	ON	D80
DA0	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	DA0
DC0	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	DC0
DE0	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	DE0
E00	ON	OFF	OFF	OFF	ON	ON	ON	ON	E00
E20	ON	OFF	OFF	OFF	ON	ON	ON	OFF	E20
E40	ON	OFF	OFF	OFF	ON	ON	OFF	ON	E40
E60	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	E60
E80	ON	OFF	OFF	OFF	ON	OFF	ON	ON	E80
EA0	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	EA0
EC0	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	EC0
EE0	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	EE0
F00	ON	OFF	OFF	OFF	OFF	ON	ON	ON	F00
F20	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	F20
F40	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	F40
F60	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	F60
F80	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	F80
FA0	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	FA0
FC0	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	FC0
FE0	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	FE0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
1000	OFF	ON	ON	ON	ON	ON	ON	ON	1000
1020	OFF	ON	ON	ON	ON	ON	ON	OFF	1020
1040	OFF	ON	ON	ON	ON	ON	OFF	ON	1040
1060	OFF	ON	ON	ON	ON	ON	OFF	OFF	1060
1080	OFF	ON	ON	ON	ON	OFF	ON	ON	1080
10A0	OFF	ON	ON	ON	ON	OFF	ON	OFF	10A0
10C0	OFF	ON	ON	ON	ON	OFF	OFF	ON	10C0
10E0	OFF	ON	ON	ON	ON	OFF	OFF	OFF	10E0
1100	OFF	ON	ON	ON	OFF	ON	ON	ON	1100
1120	OFF	ON	ON	ON	OFF	ON	ON	OFF	1120
1140	OFF	ON	ON	ON	OFF	ON	OFF	ON	1140
1160	OFF	ON	ON	ON	OFF	ON	OFF	OFF	1160
1180	OFF	ON	ON	ON	OFF	OFF	ON	ON	1180
11A0	OFF	ON	ON	ON	OFF	OFF	ON	OFF	11A0
11C0	OFF	ON	ON	ON	OFF	OFF	OFF	ON	11C0
11E0	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	11E0
1200	OFF	ON	ON	OFF	ON	ON	ON	ON	1200
1220	OFF	ON	ON	OFF	ON	ON	ON	OFF	1220
1240	OFF	ON	ON	OFF	ON	ON	OFF	ON	1240
1260	OFF	ON	ON	OFF	ON	ON	OFF	OFF	1260
1280	OFF	ON	ON	OFF	ON	OFF	ON	ON	1280
12A0	OFF	ON	ON	OFF	ON	OFF	ON	OFF	12A0
12C0	OFF	ON	ON	OFF	ON	OFF	OFF	ON	12C0
12E0	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	12E0
1200	OFF	ON	ON	OFF	OFF	ON	ON	ON	1200
1320	OFF	ON	ON	OFF	OFF	ON	ON	OFF	1320
1340	OFF	ON	ON	OFF	OFF	ON	OFF	ON	1340
1360	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	1360
1380	OFF	ON	ON	OFF	OFF	OFF	ON	ON	1380
13A0	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	13A0
13C0	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	13C0
13E0	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	13E0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
1400	OFF	ON	OFF	ON	ON	ON	ON	ON	1400
1420	OFF	ON	OFF	ON	ON	ON	ON	OFF	1420
1440	OFF	ON	OFF	ON	ON	ON	OFF	ON	1440
1460	OFF	ON	OFF	ON	ON	ON	OFF	OFF	1460
1480	OFF	ON	OFF	ON	ON	OFF	ON	ON	1480
14A0	OFF	ON	OFF	ON	ON	OFF	ON	OFF	14A0
14C0	OFF	ON	OFF	ON	ON	OFF	OFF	ON	14C0
14E0	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	14E0
1500	OFF	ON	OFF	ON	OFF	ON	ON	ON	1500
1520	OFF	ON	OFF	ON	OFF	ON	ON	OFF	1520
1540	OFF	ON	OFF	ON	OFF	ON	OFF	ON	1540
1560	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	1560
1580	OFF	ON	OFF	ON	OFF	OFF	ON	ON	1580
15A0	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	15A0
15C0	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	15C0
15E0	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	15E0
1600	OFF	ON	OFF	OFF	ON	ON	ON	ON	1600
1620	OFF	ON	OFF	OFF	ON	ON	ON	OFF	1620
1640	OFF	ON	OFF	OFF	ON	ON	OFF	ON	1640
1660	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	1660
1680	OFF	ON	OFF	OFF	ON	OFF	ON	ON	1680
16A0	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	16A0
16C0	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	16C0
16E0	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	16E0
1700	OFF	ON	OFF	OFF	OFF	ON	ON	ON	1700
1720	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	1720
1740	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	1740
1760	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	1760
1780	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	1780
17A0	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	17A0
17C0	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	17C0
17E0	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	17E0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
1800	OFF	OFF	ON	ON	ON	ON	ON	ON	1800
1820	OFF	OFF	ON	ON	ON	ON	ON	OFF	1820
1840	OFF	OFF	ON	ON	ON	ON	OFF	ON	1840
1860	OFF	OFF	ON	ON	ON	ON	OFF	OFF	1860
1880	OFF	OFF	ON	ON	ON	OFF	ON	ON	1880
18A0	OFF	OFF	ON	ON	ON	OFF	ON	OFF	18A0
18C0	OFF	OFF	ON	ON	ON	OFF	OFF	ON	18C0
18E0	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	18E0
1900	OFF	OFF	ON	ON	OFF	ON	ON	ON	1900
1920	OFF	OFF	ON	ON	OFF	ON	ON	OFF	1920
1940	OFF	OFF	ON	ON	OFF	ON	OFF	ON	1940
1960	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	1960
1980	OFF	OFF	ON	ON	OFF	OFF	ON	ON	1980
19A0	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	19A0
19C0	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	19C0
19E0	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	19E0
1A00	OFF	OFF	ON	OFF	ON	ON	ON	ON	1A00
1A20	OFF	OFF	ON	OFF	ON	ON	ON	OFF	1A20
1A40	OFF	OFF	ON	OFF	ON	ON	OFF	ON	1A40
1A60	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	1A60
1A80	OFF	OFF	ON	OFF	ON	OFF	ON	ON	1A80
1AA0	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	1AA0
1AC0	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	1AC0
1AE0	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	1AE0
1B00	OFF	OFF	ON	OFF	OFF	ON	ON	ON	1B00
1B20	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	1B20
1B40	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	1B40
1B60	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	1B60
1B80	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	1B80
1BA0	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	1BA0
1BC0	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	1BC0
1BE0	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	1BE0

Base Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Base Address
1C00	OFF	OFF	OFF	ON	ON	ON	ON	ON	1C00
1C20	OFF	OFF	OFF	ON	ON	ON	ON	OFF	1C20
1C40	OFF	OFF	OFF	ON	ON	ON	OFF	ON	1C40
1C60	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	1C60
1C80	OFF	OFF	OFF	ON	ON	OFF	ON	ON	1C80
1CA0	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	1CA0
1CC0	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	1CC0
1CE0	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	1CE0
1D00	OFF	OFF	OFF	ON	OFF	ON	ON	ON	1D00
1D20	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	1D20
1D40	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	1D40
1D60	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	1D60
1D80	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	1D80
1DA0	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	1DA0
1DC0	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	1DC0
1DE0	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	1DE0
1E00	OFF	OFF	OFF	OFF	ON	ON	ON	ON	1E00
1E20	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	1E20
1E40	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	1E40
1E60	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	1E60
1E80	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	1E80
1EA0	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	1EA0
1EC0	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	1EC0
1EE0	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	1EE0
1F00	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	1F00
1F20	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	1F20
1F40	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	1F40
1F60	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	1F60
1F80	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	1F80
1FA0	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	1FA0
1FC0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	1FC0
1FE0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	1FE0

Appendix B (PC62C Template)

Appendix B