Eagle Technologies

PCI-730 DAQ Module

Technical Manual

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1. Module Features

1.1 PCI Interface

- The PCI-730 DAQ module is PCI 2.2 compliant at 32 bits and 33 Mhz.
- The modules are 5V and 3.3V PCI slot compatible.
- The module implements a target only interface.

1.2 Analogue Input Interface

- Sixteen single ended or 8 differential inputs are supported. These can be mixed on a channel per channel basis.
- Programmable full scale input ranges of +/- 2.5V, +/- 5V or +/- 10V are available on a channel per channel basis.
- Input Coupling DC
- Maximum working voltage ± 11 V relative to module ground.
- FIFO Buffer Size Maximum 2048 with programmable word count interrupt.
- Channel List Buffer Size Maximum sixteen entries
- Data Transfers PCI target, 32 bit DWORD, Memory mapped.
- Maximum Sampling Rate 200 KS/s. Programmable 32 bit timer, 20 MHz base clock
- Resolution Fourteen bits
- Relative Accuracy ± 1 LSB maximum
- Absolute Maximum Error ± 2 LSB max.
- External trigger From TTL input source

1.3 Analogue Output

- Number of channels 4
- Output Range +/- 10V @ 5 mA.
- Maximum update rate 840 ns per transfer to a DAC channel.
- Settling time 1 us to 0.1% of full scale, 2us to .015% of full scale..
- Data Transfer: PCI target, 32 bit DWORD, Memory mapped
- Resolution 14 Bits

- Absolute Maximum Error +/- 2 mV

1.4 Digital I/O

- Number of channels 24
- Compatibility 82C55
- I/O Characteristics 82C55

1.5 82C54 Counter Timers

- Number of 82C54 devices 1
- Gate Control Jumper selectable from either External IO or Internal FPGA.
- Clock Control Jumper selectable from either External IO or Internal FPGA.

2. Hardware Overview

2.1 Analogue Input Channel

This chapter provides a hardware overview of the PCI-730 DAQ module. A block diagram of the analogue input channel is shown in Figure 1.

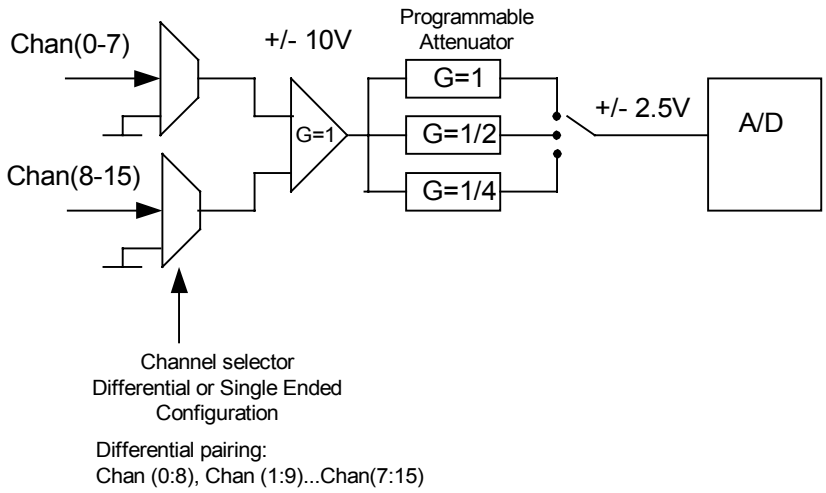

Figure 1 PCI-730 Analogue Input Channel Functional Diagram

Sixteen single ended or eight differential inputs are provided. The configuration of each channel (or pair) is programmable on a channel per channel basis and is programmed as a function of the data configured in the Channel List.

The maximum input voltage on any channel is +/-10V which is scaled down to the +/- 2.5V required by the A/D. To cater for +/5V and +/-2.5V full scale input signals the attenuator is programmable on a channel per channel basis and is also defined in the channel list.

The sixteen deep (maximum) channel list is provided . This list contains the channel's configuration information and also defines the sequence of channels to be converted and stored in the result FIFO. On each tick of the A/D timer clock (maximum 200 kHz) the next channel in the list is converted. The channel list will wrap to the first entry whenever the end of list is detected hence the list need not always contain a full 16 channel configuration.

The A/D timer tick can also be generated under software control. This allows the user to setup the channel list and sequence through the conversions using programmed I/O commands.

2.2 Analogue Output Channel

Four +/-10V analogue outputs are provided by the Analog Devices AD5554 QUAD DAC chip.

These DAC's can only be accessed using programmed I/O commands as no buffer list is provided. The DAC's are serial devices that are timed and controlled by the FPGA. To programme a DAC channel the host need merely write to the common DAC Control Register. The FPGA will monitor the updates to this register and sequence the data to the correct DAC channel (this takes 840 ns.) On each host write to this DAC control register a BUSY flag is set which is only cleared when the DAC channel in the AD5554 is updated. New DAC data should only be written when the DAC Control Register is ready to accept a new command.

2.3 Module Address Map & BIT Definitions

The module uses PCI 2.1 compatible target only interface. The module is mapped to a 64Kbyte memory space and only supports 32 bit, DWORD aligned, Memory WRITE/READ commands.

NOTE: Not all registers are fully decoded.

The PCI-730 module's control registers and FIFO' s are mapped as per Table 1.

Configuration register BAR0 used as the base.		
Offset Address(Hex)	**Register Name**	**Description**
XX00 – XX3C	A/D_CHANNEL_LIST	A 16 x 8 Buffer used to hold Channel Configuration data. When first enabled, the A/D initialises it's buffer pointer to 0 and each A/D clock tick , will execute the current buffer command. The number of entries in the buffer is define in the AD_SETUP register. After N clock ticks the cycle will re-start at index 0 Configures the conversion list & configuration. Usually WRITE only but it can be read by the host when in TEST mode. **Bits <4:0>** : CHANNEL SELECTION (READ/WRITE) Select the input channel as follows: "00000": Channel 0. "00001": Channel 1. "00010": Channel 2. : : "01111": Channel 15. "1------": Input is 0 V. **Bits <5>:** INPUT MODE (READ/WRITE) Select SE or DE for the channel defined in <4:0> "0" Channel "N" is single ended "1" Channel "N" is paired with Channel "N+8". **Bits <7:6>** : ATTENUATION (READ/WRITE) Selects the input attenuator as follows "00": Attenuator = ¼. Input is +/- 2.5V "01": Attenuator = ½ . Input is +/- 5V "10": Attenuator = 1. Input is +/- 10V. "11": Attenuator = 0. Input is AGND

Configuration register BAR0 used as the base.		
Offset Address(Hex)	**Register Name**	**Description**
XX40	A/D_SETUP	Used to configure the A/D mode of operation. **Bit<0>**: A/D ENABLE (READ/WRITE) '0': A/D is disabled. (default) '1': A/D is enabled. **Bit<1>**: A/D CLOCK MODE (READ/WRITE) '0': A/D is configured to operate from the A/D Timer clock '1': A/D is configured to operate under programmed I/O under control of bit(11). **Bit<2>**: AD RESULT FIFO RESET CONTROL (READ/WRITE) '0': A/D Result FIFO is are in operational mode '1': A/D Result FIFO is RESET. NOTE: This will also reset the A/D's Channel List pointer to 0. **Bit<3>**: AD RESULT FIFO TEST MODE (READ/WRITE) '0': A/D Result FIFO is in operational mode. '1': A/D Result FIFO is in TEST mode and can be written and read by the host. **Bit<7:4>**: ENTRIES IN CHANNEL LIST (READ/WRITE) Defines the (number +1) of entries in the channel list. A value of "0000" defines 1 entry, 15 = 16 entries i.e. the channel list is full. **Bit<8>**: A/D TRIGGER MODE (READ/WRITE) '0': EXT_TRIGGER is ignored. '1': EXT_TRIGGER must be asserted. **Bit<9>**: RESULT FIFO STATUS (READONLY) '0': A/D result FIFO has less entries than the water mark value. '1': A/D result FIFO has more entries than the water mark value **Bit<10>**: INTERRUPT ENABLE (READ/WRITE) '0': A/D FIFO Interrupts are disabled '1': A/D FIFO Interrupts are enabled This interrupt can be generated whenever the number of words in the A/D result FIFO exceed that programmed in the A/D_WATERMARK register. **Bit<11>**: PROGRAMMED I/O A/D CONVERT(READ/WRITE) Writing a '1' to this bit will trigger a A/D conversion cycle if Bit<1> is set. This bit will toggle back to a '0' whenever the current conversion is completed and the result available in the FIFO. **Bit<12>**: A/D FIFO RESULT IS 32 BIT (READ/WRITE) '0': AD Result FIFO is read as 16 bits only. (Default) '1': AD Result FIFO is read as 32 bits. Note that in this 32 bit mode the word count, watermark and FIFO pointers still operate as though the interface and RAM is 16 bits wide.- which it is. However, doing a thirty two bit read will double read the sixteen bit RAM and pack the results as follows: Bits(15:0): First sixteen bits in the FIFO (at Pointer x) Bits(31:0): Second sixteen bits in the FIFO (at Pointer x+1).

Configuration register BAR0 used as the base.		
Offset Address(Hex)	**Register Name**	**Description**
XX44	A/D_FIFO_DATA	Contains the A/D conversion results. Usually READ only but it can be written by the host when in TEST mode. The FIFO is 2048 x 16 deep. **Bits <15:14>** : are always track bit<13> . **Bits <13:0> :** Contain A/D result or host test data. All conversions are BI-POLAR the ideal A/D results are coded as follows: **CODE A/D Input Voltage** 0001111111111111 = 2.5V – 1 LSB 0000000000000000 = 0 1110000000000000 = - (2.5V – 1 LSB).
XX48	A/D_TIMER_CONTROL	READ/WRITE **Bits <31:0>:** Sets up the A/D Timer Clock Period Sets the initial count for a programmable down counter operating from a 20 MHz clock source. The timer will down count whenever the A/D is enabled. On reaching a terminal count of 0, the A/D sample will be taken, the result stored in the A/D FIFO and the channel list pointer incremented. The timer will then re-load. If the A/D is not enabled this register can be WRITE/READ for test purposes.
XX4C	A/D_WATERMARK	READ/WRITE **Bits <10:0>:** Defines the A/D FIFO watermark level. Whenever the number of entries in the A/D result FIFO exceeds this programmed value an A/D interrupt is generated if enabled.

Configuration register BAR0 used as the base.		
Offset Address(Hex)	**Register Name**	**Description**
XX5X	DAC_CONTROL REGISTER	**Bits <15:0>:** DAC DATA (READ/WRITE) Defines the 14 (or 16) bits of data to written to the DAC. Bit <15> is always MSB. **Bits <17:16>:** DAC CHANNEL NUMBER (READ/WRITE) Defines the DAC channel to which the data is to be written. **Bits <18>:** DAC_RESOLUTION(READ/WRITE) '0': DAC is 14 bits : Default '1': DAC is 16 bits **Bit <19>:** DAC_DONE_FLAG (READ ONLY) This bit is cleared whenever this register is written and the FPGA is busy formatting the data to the DAC channel. This bit will transition to a '1' when a new DAC command can be issued. On RESET this bit is set to '1'.

Configuration register BAR0 used as the base.		
Offset Address(Hex)	**Register Name**	**Description**
XX6X	82C54_CONFIG	Defines some external configuration controls for the external 82C54 counter timer. **GATE CONTROL** **Bits <0>:** READ/WRITE FPGA GATE control for Counter 0. Maps to F_GATE0. **Bits <1>:** READ/WRITE FPGA GATE control for Counter 1. Maps to F_GATE1. **Bits <2>:** READ/WRITE FPGA GATE control for Counter 1. Maps to F_GATE2. **TIMER STATUS FLAGS** **Bits <3>:** A status flag that is set whenever a rising edge is detected on Counter 0's COUT terminal count condition. Can be un-masked to generate an interrupt. This flag can only be set by the timer's TC signal and can only be cleared by the software writing '**1**' to this bit. **Bits <4>:** A status flag that is set whenever a rising edge is detected on Counter 1's COUT terminal count condition. Can be un-masked to generate an interrupt. This flag can only be set by the timer's TC signal and can only be cleared by the software writing '**1**' to this bit. **Bits <5>:** A status flag that is set whenever a rising edge is detected on Counter 2's COUT terminal count condition. Can be un-masked to generate an interrupt. This flag can only be set by the timer's TC signal and can only be cleared by the software writing '**1**' to this bit. **TIMER STATUS FLAGS INTERUPT MASK BITS** **Bits <8:6>:** READ/WRITE Interrupt un-mask for Status Flags <5:3>. An interrupt is generated whenever any of the status bits <5:3> are asserted and the interrupt is un-masked. "0": Interrupt is masked. "1": Interrupt is enabled. **Bits <15:9>:** READ/WRITE Reserved **FPGA EXTERNAL CLOCK FREQUENCY FOR 82C54.** **Bits <31:16>:** READ/WRITE Defines the initial count for a down counter that is used as an optional FPGA generated clock for the 82C54. (Signal 82C54_CLK). Frequency = 20Mhz/(2(N+1))This counter is always enabled and operates from the 20 MHz base clock. This output toggles whenever the counter reaches a terminal count of 0 and re-loads i.e. it is always a 50% duty cycle.

Configuration register BAR0 used as the base.		
Offset Address(Hex)	**Register Name**	**Description**
XX7X	82C54_INTERFACE	These addresses provide a direct READ/WRITE access to the 8 bit ports supported by the external 82C54 counter timer. PCI Address(2) Maps to the 82C54 A(0) line. PCI Address(3) Maps to the 82C54 A(1) line.
XX8X	82C55_INTERFACE	These addresses provide a direct READ/WRITE access to the 8 bit ports supported by the external 82C55 PIO Device PCI Address(2) Maps to the 82C55 A(0) line. PCI Address(3) Maps to the 82C55 A(1) line.
XX9X	EEPROM INTERFACE	Used to access the serial EEPROM. **Bits <0>:** (READ/WRITE) Maps directly to the EEPROM CS signal. **Bits <1>:** (READ/WRITE) Maps directly to the EEPROM DI signal. Data to the EEPROM **Bits <2>:** (READ/WRITE) Maps directly to the EEPROM CLK signal. Clock to the EEPROM **Bits <3>:** (READ) Maps directly to the EEPROM DO signal. Data from the EEPROM

Table 1 PCI-730 Register Address Map

3. NOTES

(a) When operating the AD result FIFO in 32 bit mode, the only difference between this and normal sixteen bit mode is that the FPGA internally reads the FIFO twice and packs the two sixteen bit words into a 32 bit result. This only adds 2 x PCI clock cycles to a normal sixteen bit read cycle. The word counter, watermark register etc. will still reflect the FIFO status in terms of 16 bit A/D results.

BEWARE not to try and read the FIFO in 32 bit mode when there are only an ODD number of 16 words in the result as the FIFO read pointer will be incremented regardless. Beware of the following scenario:

- FIFO is initialised (reset) and the A/D enabled.
- A/D writes one 16 bit result and increments it's write pointer to 1.
- Host reads ONE 32 bit word. Data(15:0) contains the A/D word and Data(31:16) contains garbage. The FIFO read pointer is incremented to 2.
- The A/D now writes a new conversion to index 1.
- The Host cannot access this as it's read pointer has incremented past this result.