How the heck do I measure a gate drive slewing at 70kV/us?

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The Power Point Presentation will be available after the conference.

Abstract

Power Electronic converter efficiency and reliability is determined by a complex tradeoff between gate drive design, switch losses, EMI generation, switch Safe Operating Area and managing parasitic effects. But gate drives can slew common mode at up to 70KV/us, and tools to measure voltage waveforms, power loss, impedance, and stability while exposed to this common mode slew are thin on the ground.

We present a new channel isolated oscilloscope which can measure voltage waveforms, the power loss in a switch device, the wideband impedance of a gate drive power supply, and the charge delivered to a gate all while the gate drive is slewing 700V in 10ns. Using phase coherent channels, and an isolated tracking signal generator for stimulus, the oscilloscope can generate a Bode plot of the closed loop gate drive response, and determine stability.

The oscilloscope can be applied to measure gate driver performance, switch losses, EMI generation and Safe Operating Area during switch operation in a manner not previously possible, and use the results to formalize the system tradeoffs to achieve highest efficiency and reliability.

Some say that without measurement there is no hope. All we know is that this oscilloscope was born for power electronics measurement.

1 Synopsis

1.1 The measurement need

At the heart of all modern power converters is the half bridge with two power switch transistors that switch the output between three states - switch to VBUS- and VBUS+, or floating (both transistors off).

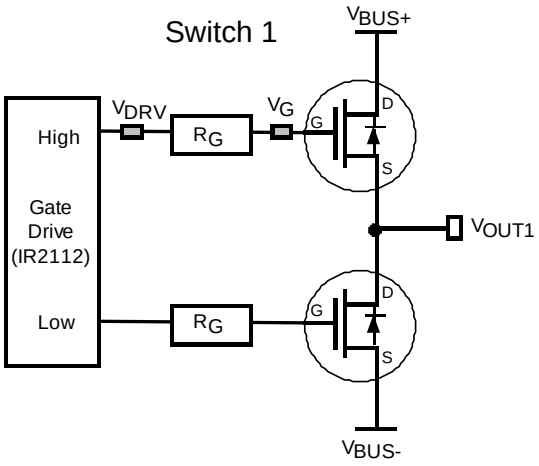


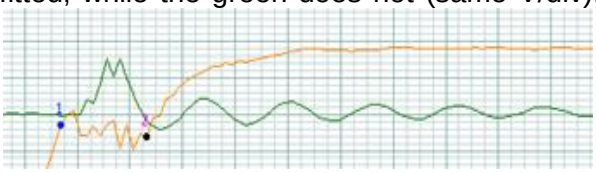
Fig 1. The Half-bridge.

For a three phase inverter, three such half bridges are used. Reliable operation requires each half bridge to set its output while under load. The switching frequency may be as high as several MHz. Modern power converter switch turn on/off times are reducing to nano second periods to increase efficiency, allow higher frequency operation and hence reduced converter volume, reduced cost, and increase control bandwidth. Reducing the turn on and turn off times increases EMI generation, increases the effects of parasitic inductance and capacitance, increases voltage overshoot stress and increases the effect of common mode slew on the gate drive system. Numerous papers have been published concerning the gate drive and increased switch performance [eg 1, 2]. Trading off the positives and negatives requires simulation and measurement. Without measurement the designer must make assumptions, and works in the dark. Reliability is not assured.

The gate drive is getting more complex - some use closed loop control [2] and most constrain the gate drive time/voltage driven from an isolated power supply. To validate the converter design and operation we need to measure such parameters as switch losses (V_{DS} x I_{DS} integrated over the switch time), Voltage Overshoot, Gate drive charge (V_G-V_{DRV}/R_G integrated over time), gate drive delay and switching time. We need to measure between half bridges to ensure switch devices have adequate dead times. We need to verify the closed loop stability, and the power supply impedance, to ensure it can deliver charge at the required frequency. The tool of choice for this is the oscilloscope, but the requirements on the oscilloscope are tough.

Just to put some numbers to some of these requirements:

1. Most mains powered inverters operated off 3 phase 208 - 480VAC power, where the bus voltage is $\sqrt{2}$ times this: 295 - 680VDC. So measurements need to be isolated, and the isolation should meet the IEC61010-2-30 300Vrms Category II standard at a minimum, allowing use on equipment operating at >800 V_{DC}.
2. To measure V_{DRV} and VG while the upper 'high-side' transistor is switching, the oscilloscope must have a high Common Mode Rejection Ratio (CMRR). For a reasonable estimate of gate drive charge, we want less than 1% voltage waveform distortion. Assuming a 10x probe (which makes the CMRR 10x worse), we want less that 0.1% voltage waveform distortion at the oscilloscope input. Assuming a gate drive voltage of the order of 10V, this is <10mV. With a 650V slew, we need a CMRR of 650/10mV >96 dB. Typical IGBT inductive rise/fall times range from 30ns to 1us, corresponding to bandwidths of about 10MHz to 350kHz ($BW = {}^{1}/_{\pi\Delta t}$). SiC MOSFET switches have rise/fall times of 40 - 70ns [3] , corresponding to bandwidths of 8 - 5MHz, while GAN high voltage transistors switch in as little as 7ns [4], a bandwidth of 45MHz Thus a requirement of >96dB CMRR at 50MHz is a good spec.
3. The coaxial cable shield inductance and the capacitance to ground (or the free space capacitance) of the measurement system form an LC tank which is excited by the high slew rate switch edges. For example the measured inductance of a typical 1.2m 10x probe common to common is about 900nH. With an isolated capacitance of coax to ground of about 10pF, $f = {}^{1}/_{2\pi\sqrt{LC}}$ or about 53 MHz. Decreasing the inductance or capacitance increase the ring frequency. The ring is impressed longitudinally along the length of the coax, generating a signal between the probe tip, and the coax outer which adds to the signal being measured. This ring can be seen in the captured signals. It is quite troublesome and can be much larger than the common mode induced errors. The principal solution is to increase the coaxial shield impedance by fitting common mode lossy ferrites around the coaxial cable. As an example the yellow signal has a ferrite fitted, while the green does not (same V/div):



1.2 The Solution

The Cleverscope CS448 [5] has been designed from the ground up to measure these kinds of signals. It has >100 dB CMRR at 50 MHz with 1kV working voltage between channels and ground. All 4 channels are phase aligned with better than +140 ps skew so it can be used for impedance and gain/phase measurement. The signal generator also has >110 dB CMRR at 50 MHz, with a working voltage between the output and ground of 800V. The CS448 provides coherent measurement of the channel inputs and tracking generator. In addition the CS448 has 110 dB frequency domain dynamic range using its 14 bit ADC's for EMI, and frequency response analysis.

2 The Measurements

2.1 The Measurement Setup

Tests were made using a Cleverscope CS1090 bridge driver with 10ns rise and fall times, and a SEW Movitrac variable speed drive to illustrate differences in timing and voltage.

2.2 SEW Movitrac Gate Drive Measurements

The SEW Movitrac is a small variable speed drive using IR2112 gate drivers with 220 ohm series resistors driving the switching FETs (R_G). R_{IL} is 0.1 ohms. There is no R_{IU}. The high side gate is measured:

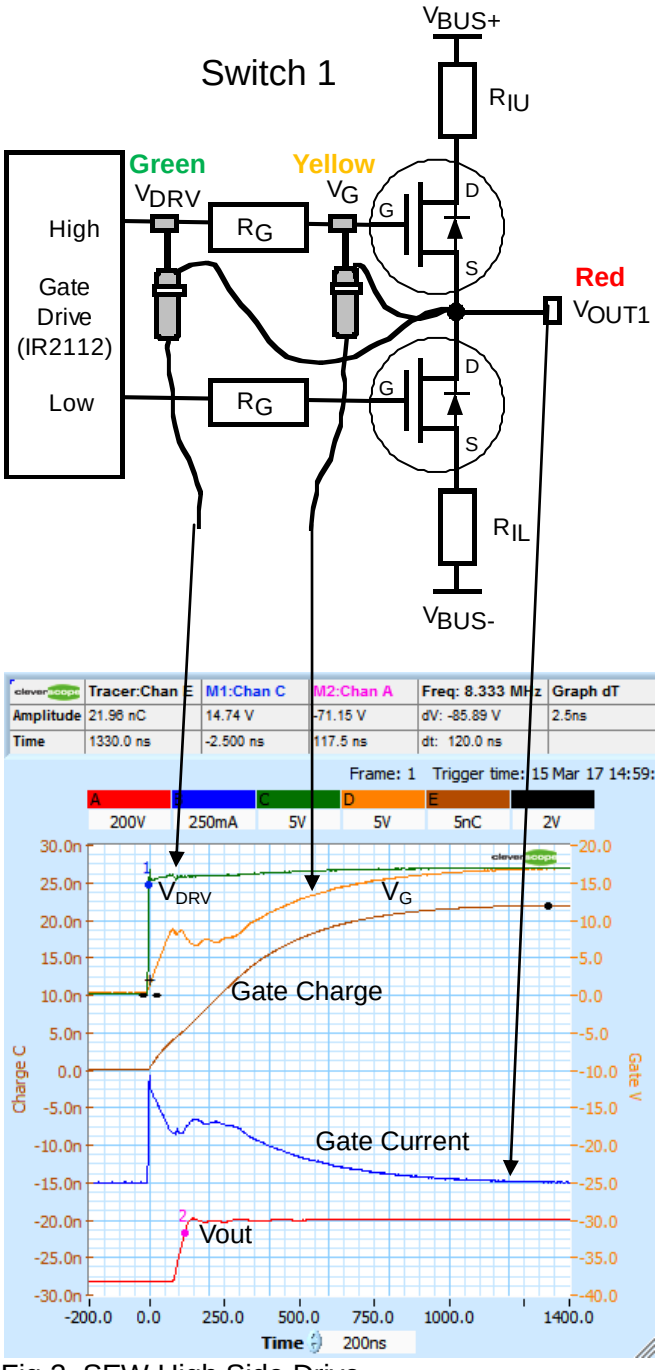


Fig 2. SEW High Side Drive

Measurements:

- The Gate voltage is 17.0V maximum.
- The Gate Current (derived from V_{DRV}-V_G/R_G, where R_G = 220 ohms) is 714mA maximum.
- The total gate charge is 21.96 nC (Tracer), derived by integrating the gate current over time.
- The gate plateau lasts 190 ns.
- The total gate rise time is about 1us.
- The gate plateau voltage is 8.1V
- The Vout turn on delay is 120ns (M2-M1).
- The Vout rise is 37ns, from -321V to 0V.

These values set the limits on switch frequency.

2.3 CS1090 Gate Drive Measurements

The CS1090 is a Cleverscope tool to verify performance under high slew rates. It uses fast FETs to achieve rise and fall times of about 10ns. The higher slew rates exhibit test cases for greater parasitic generation.

The CS1090 uses a IRS2453D Bridge driver with a 180 mA constant current source with a 10 ohm drive resistor. We measure across the high side drive resistor:

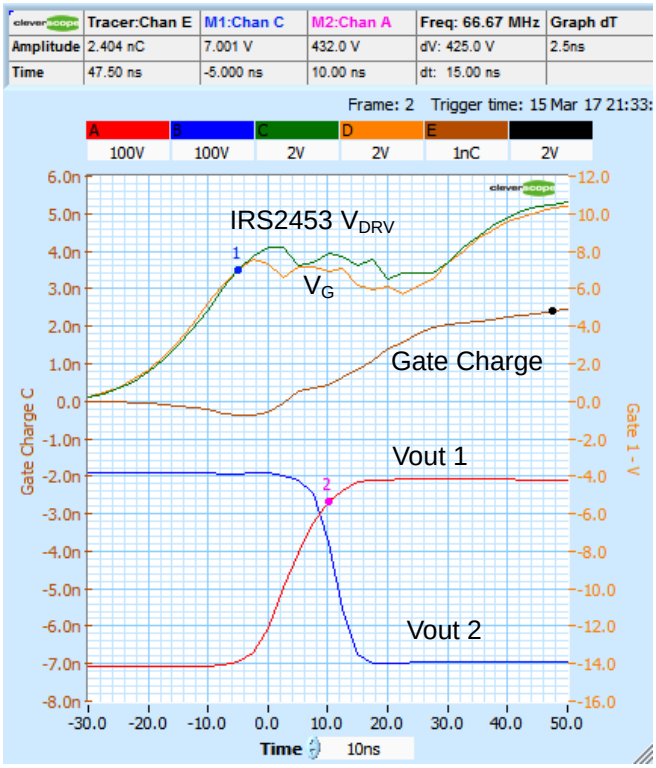


Fig 3 Cleverscope CS1090 High Side Gate Drive

Measurements:

- The Gate voltage is 12.5V maximum.
- The Gate Current (derived from V_{DRV}-V_G/R_G, where R_G = 10 ohms) is 180mA.
- The total gate charge is 2.5 nC, derived by integrating the gate current over time.
- The gate plateau lasts 30 ns.
- The total gate rise time is about 80ns.
- The gate plateau voltage is about 6V
- The V_G to V_{OUT} turn on delay is 8ns.
- Vout rises from 0V to 500V in 13ns

The ripple in the plateau voltage is slew rate induced (the gate is transitioning 500V in 13ns during this period).

2.3.1 Dead Time Measurements and shoot through

Dead time is the time during which both gates in opposing half bridges are turned off. If the dead time period is too small, turn off delays may cause opposing switches to be on at the same time, increasing loss, and perhaps causing damage.

Shoot through is another variation of both transistors being on, this time being caused by the high side FET turn on dV/dt coupling through C_{GD} of the low side FET, which drives the gate positive (when it should be low).

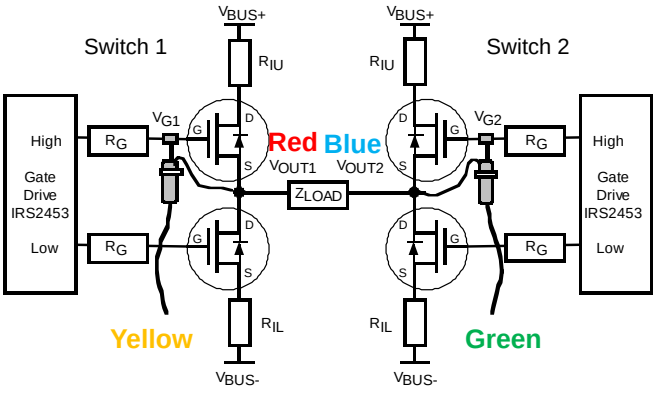


Fig 4. Bridge connected pair of half bridges.

By probing both high side gates, we can measure dead time and shoot through, as shown in Fig 5.

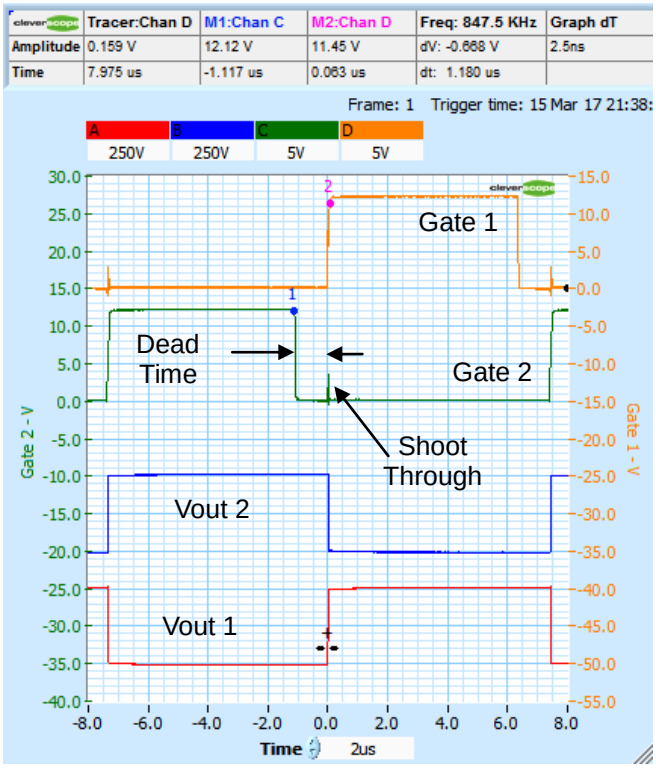


Fig 5 CS1090 Dead Time and Shoot through step

Measurements:

- The dead time between Gate 2 turning off and Gate 1 turning on is 1.180us.
- The dead time between Gate 1 turning off and Gate 2 turning on is 1.20 us.
- The gate voltage is 12.5V, and they are attached to Vout 1 and Vout 2, which swing from 0V to 500V.
- Rise time is 10.1 ns and fall time is 9.3ns (because we do not have a probe on the IRS2453 output the transition is slightly faster).
- The switching period is 14.8us (67 kHz).

We can see evidence of the Off gate voltage pulsing as the opposing switch turns on. It is important to determine if this is of sufficient level to turn on the FET.

The voltage reached is a function of C_{GD}, C_{GS}, the drive resistor, and the Vout rise time.

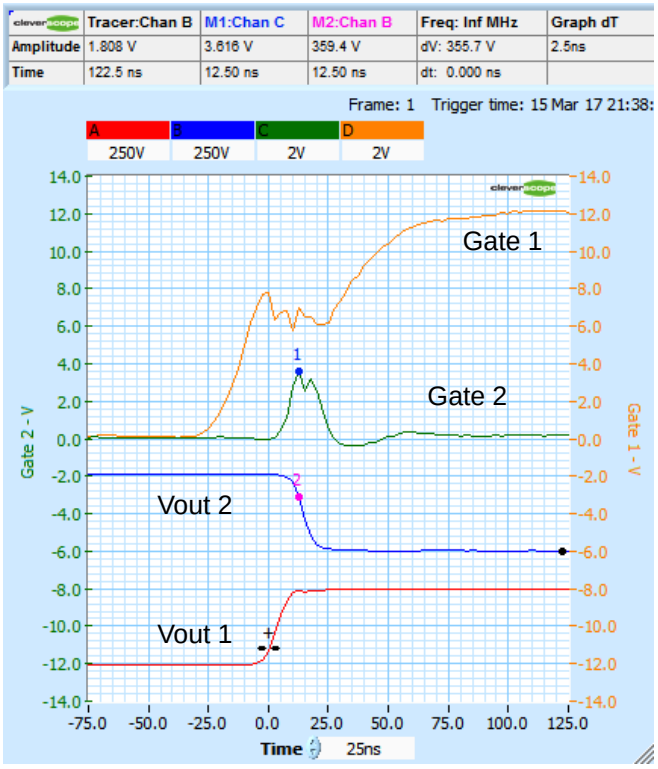


Fig 6. CS1090 gate 2 shoot through step

Measurements:

- The Gate 2 capacitive step height is 3.6V.
- The gate threshold voltage is 3-3.5V.

Insufficient charge is transferred to turn on the device (compare it with the other gate). This is a marginal situation, and either the slew rate or the gate drive resistor should be adjusted.

2.4 V_{DS} Power Loss

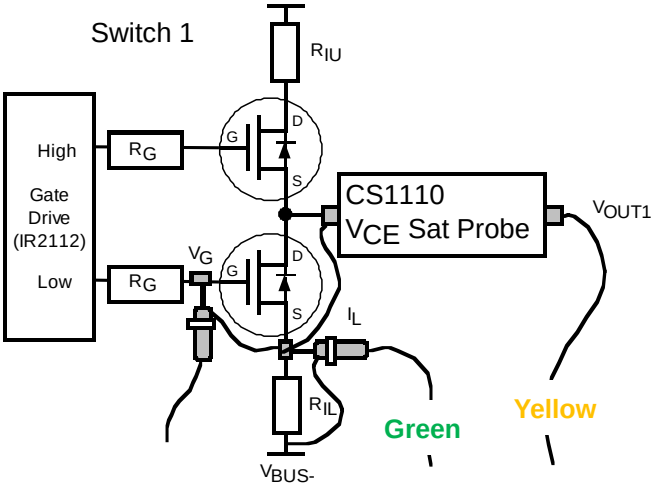


Fig 7. Power Loss measurements

The Power Loss can be carried out on either the high or low transistor. In this case, the SEW drive had a low side 0.1 ohm sense resistor. The CS1110 VCE Sat probe is used to measure the low saturation voltage in the presence of switching voltages of up to 1kV.

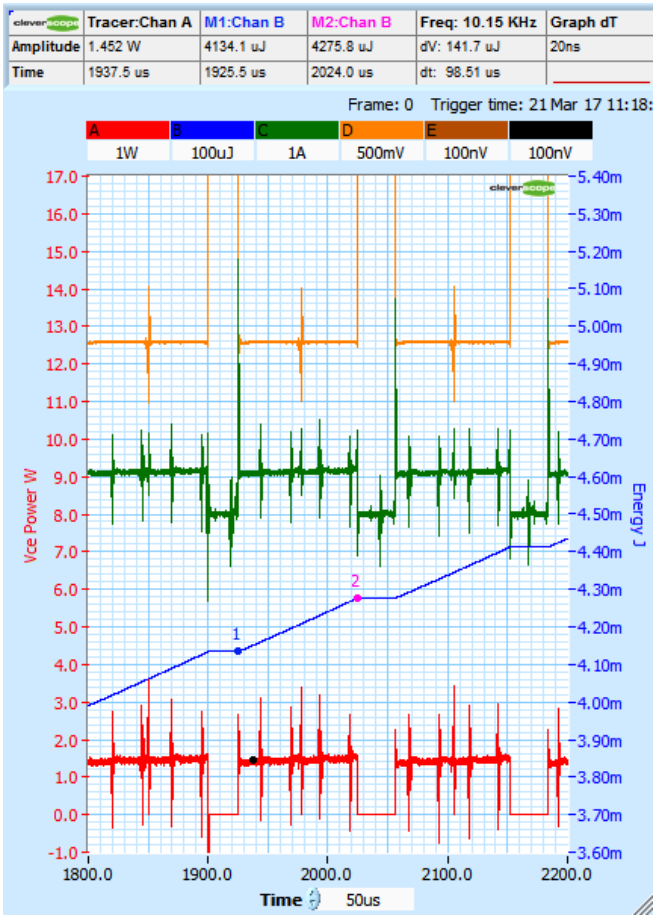


Fig 8. Power loss in the SEW switching transistor

Measurements:

- The saturation voltage V_{DS} (Chan D) is 1.298V
- The I_L current (Chan C) is 1.1A
- The switch power I_L x V_{DS} is 1.4W
- The integrated energy loss is (M2-M1) = 141uJ.

By measuring power loss over a longer period we can gain an accurate measure of the load power dissipated in the switch transistor.

In Fig 9. We have integrated the load power over one output cycle, using the full time resolution of the oscilloscope (2ns). This approach yields a more precise power loss estimate than average power, and displays peak power in the cycle.

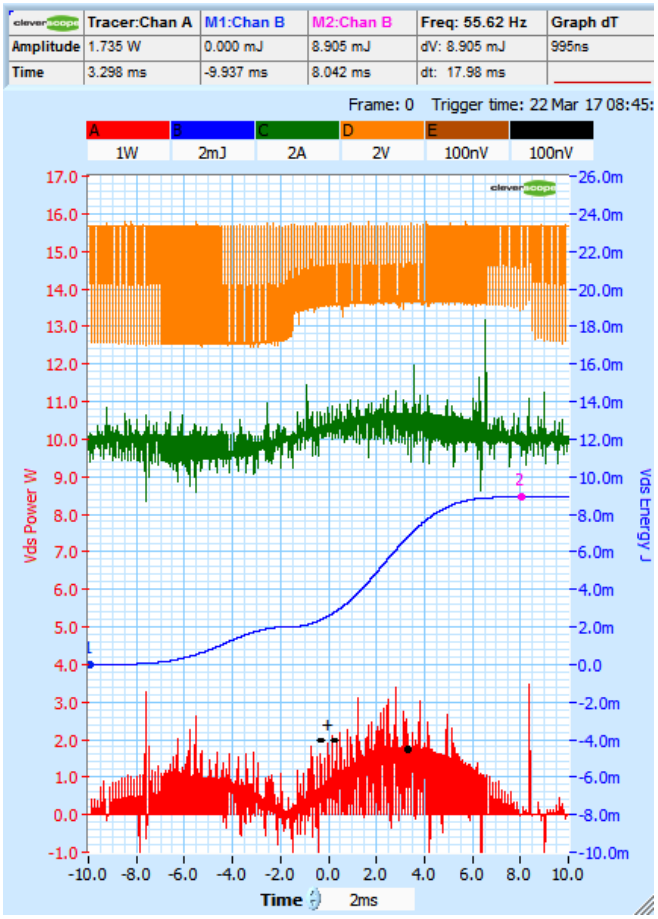


Fig 9. Power loss over a cycle (18ms)

Measurements:

- Maximum power loss is 1.7W (excluding short transients)
- Total energy over one cycle is 8.9mJ. Thus the total energy per second is 494.4mJ, or 0.49W dissipation. It's a small lightly loaded drive!

Although the graph time resolution is 995ns, Maths was done over the full data set, and so takes into account a portion of the switch loss and all the load loss. This example shows the use of understandable names and units in graph labeling.

2.5 EMC Performance

The delay time, rise time and fall time are all determined by the gate drive. These values in turn determine switch loss (pv), device stress (Irrm) and LsdIcoff/dt voltage overshoot, and EMI generation.

EMI generation is initially proportional to the switch frequency, and has amplitude falling at 20 dB/decade. A corner frequency is developed at a frequency corresponding to the switch rise time, tr, as f = $1/\pi tr$. The EMI amplitude falls at 40 dB/decade from this point. The lower the rise time, the lower the corner frequency, and hence the lower total EMI products.

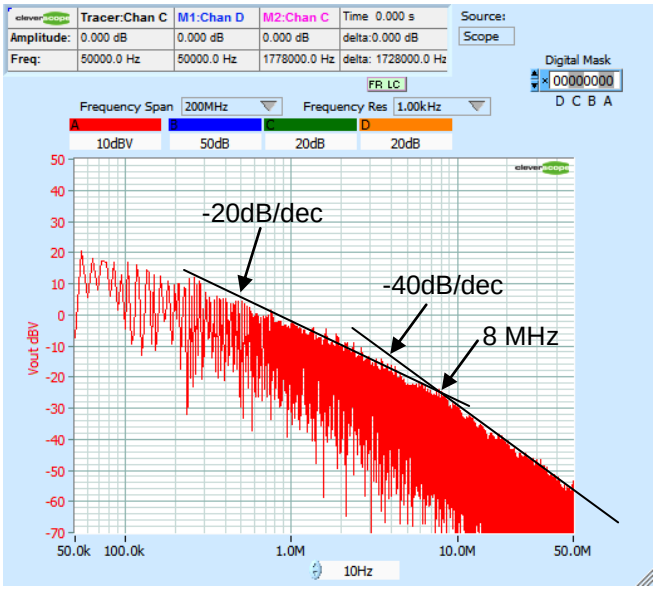


Fig 10. SEW drive harmonic production.

Measurements:

- The Vout risetime of 37ns corresponds to 8.6 Mhz, and we see a 40 dB corner at about 8 Mhz (a rise time of about 40ns).

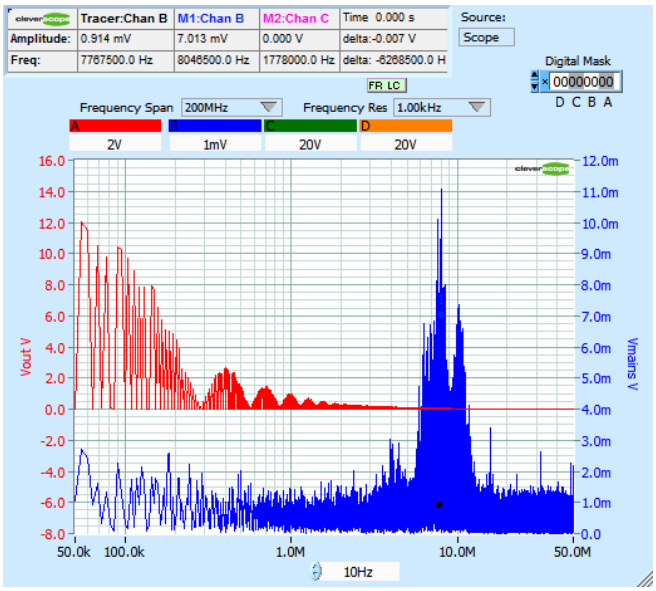


Fig 11. SEW drive mains voltage noise.

The SEW drive input mains voltage shows a peak

of about 11mV at around 8MHz (corresponding to the switch rise time) and 10 MHz (the switch fall time).

The FCC specifies an EMI maximum line voltage of 1000uV (0.45 - 1.6MHz) and 3000uV (1.6 - 30MHz) by direct measurement.

Measurements:

- The maximum mains voltage in the 1.6 - 30 MHz range is 11 mV at 8.0 MHz (which corresponds to the rise time we measured). This is in excess of the standard.
- Voltages in the 0.45- 1.6 MHz range are well in excess of the standard.

The SEW drive does not meet the FCC standard, and line filters will be required.

3 Probing tips for minimum parasitic noise

During the course of our measurements we determined some good rules of thumb to minimize parasitic voltages that are not part of the signal.

These are:

1. Ensure oscilloscope probes use ferrite suppression devices fitted close to the probe end. Materials with >300 Ohm impedance from 2 - 300 MHz are suitable.
2. The gate drive should be designed to be amenable to measurement. This means locating the pads for small coaxial connectors such as U.FL or MMCX connectors on the PCB with a ground plane and minimum connection track inductance (minimizing loop area) and capacitance (minimizing length). Maximum CMRR is maintained by keeping any exposed sense tracks as short as possible, and protected by a common plane. These attributes are all important for optimum gate drive performance as well. For high voltage switching nodes (eg V_{DS}) the connectors must be appropriately rated.
3. For loss measurements of the switching device either include intrinsic current measurement (eg SenseFETs) or include RF coaxial current sense resistors in series with the high and low side of the switch. Coaxial shunt switch energy and impedance value should match the inverter power handling capacity (for sense elements see http://www.tandmresearch.com/). For lower frequency measurements a Rogowski coil current sensor can be used (eg from http://www.pemuk.com/). Provision for looping around the current path should be made.

4 Conclusion

An optically isolated channel high dynamic range oscilloscope and signal generator is useful in measuring the values outlined, carrying out the tradeoff analysis, and verifying the design and operation of the converter. We know of no other tool with sufficient CMRR and dynamic range to do this job as simply.

5 References

[1] Y. Lobsiger and J. W. Kolar, —Stability and robustness analysis of d/dt-closed-loop IGBT gate drive,‖ in Proc. of the 28th Annual IEEE Applied Power Electronics Conf. and Exposition (APEC), Long Beach, CA, USA, Mar. 2013, pp. 2682-2689.

[2] L. Chen and F. Z. Peng, —Switching loss analysis of closed-loop gate drive,‖ in Proc. of the 25th Annual IEEE Applied Power Electronics Conf. and Exposition (APEC), Palm Springs, CA, USA, Feb. 2010, pp. 1119–1123.

[3] CREE CAS300M12BM2 Data Sheet

[4] Transphorm TPH3208LDG Data Sheet

[5] https://cleverscope.com/news/cs448/