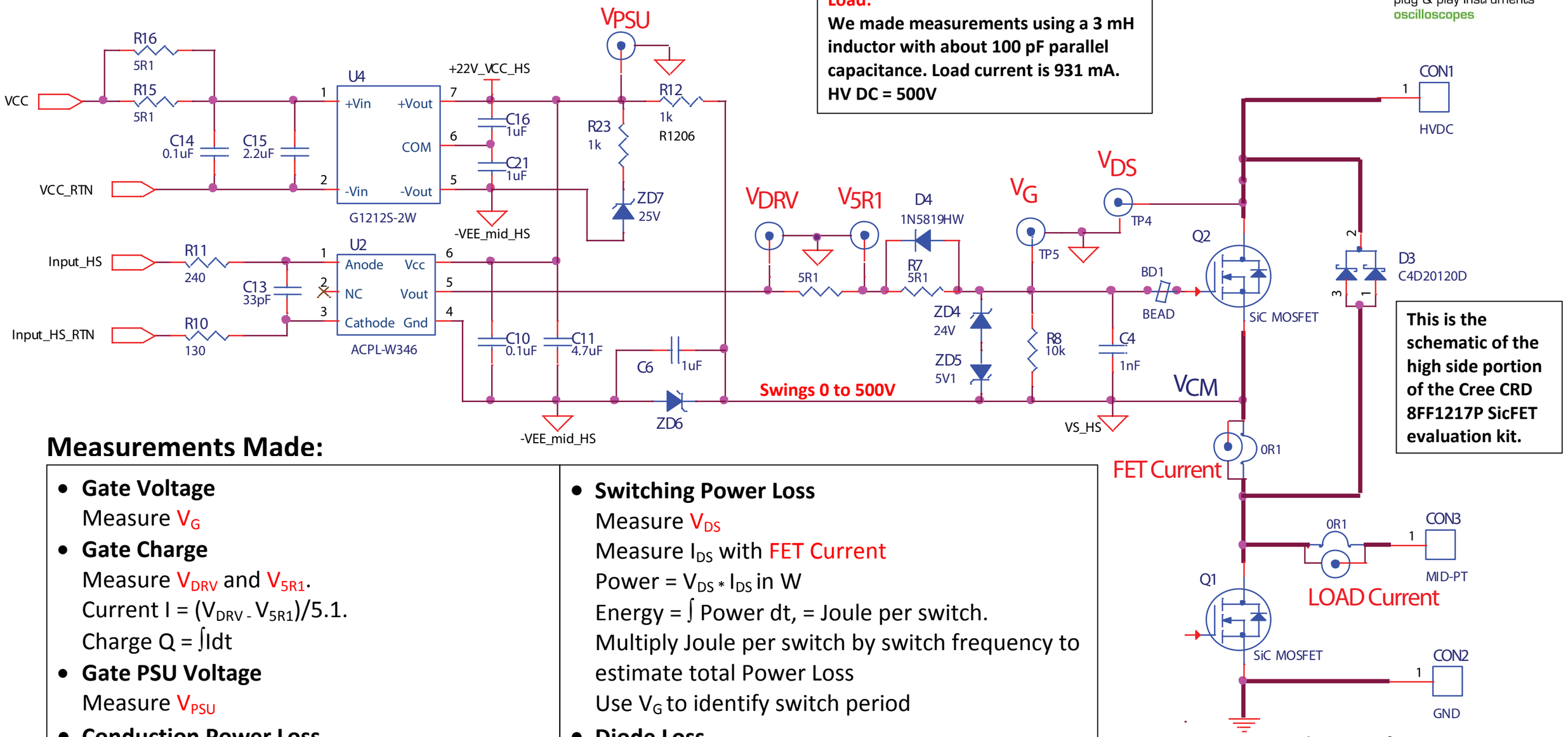
Cree SicFET High Side Measurements using the CS448

Load:
We made measurements using a 3 mH inductor with about 100 pF parallel capacitance. Load current is 931 mA. HV DC = 500V



Schematic of CRD 8FF1217P

This is the schematic of the high side portion of the Cree CRD 8FF1217P SicFET evaluation kit.

Measurements Made:

- **Gate Voltage**
  Measure V_G
- **Gate Charge**
  Measure V_{DRV} and V_{5R1}.
  Current I = $(V_{DRV} - V_{5R1})/5.1$.
  Charge Q = $\int Idt$
- **Gate PSU Voltage**
  Measure V_{PSU}
- **Conduction Power Loss**
  Measure V_{DS} with $V_{CE\text{-}SAT}$ Probe,
  Measure I_{DS} with FET Current
  Power = $V_{DS} * I_{DS}$ in W
  Energy = $\int$ Power dt, = J per switch cycle.
  Use V_G to identify ON period

⊙ = BNC measurement relative shield

- **Switching Power Loss**
  Measure V_{DS}
  Measure I_{DS} with FET Current
  Power = $V_{DS} * I_{DS}$ in W
  Energy = $\int$ Power dt, = Joule per switch.
  Multiply Joule per switch by switch frequency to estimate total Power Loss
  Use V_G to identify switch period
- **Diode Loss**
  Measure V_{DS}
  Measure I_{Diode} with Load Current
  Power = $V_{DS} * I_{Diode}$ in W
  Energy = $\int$ Power dt, = Joule per switch.
  Multiply Joule per switch by switch frequency to estimate total Diode Loss
  Use V_G and V_{DS} to identify Diode ON period

⊙ = **BNC connection**

The Measurement Challenge

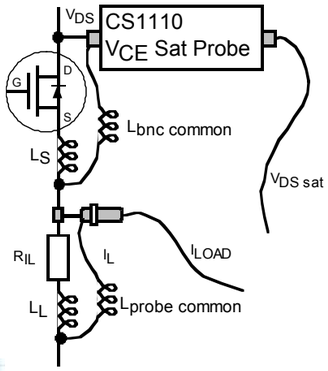
Slew Rate Rejection

The reference common mode voltage (VCM) is attached to and swinging with VOUT. The effective bandwidth of the edge is set by the edge rise or fall time: $BW = \frac{1}{\pi t_r}$

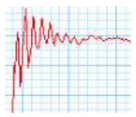
So a SicFet transition of 10ns has an effective bandwidth of BW = 1/(π 10n) = 32 MHz.

High Inductance connections

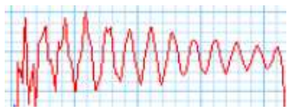
The inductance of a piece of wire is about 1nh/mm, so the common connection will have inductance if it is not coaxial (eg $L_{probe\ common\ or}\ L_{PC}$). If there is series inductance (eg L_S) in a current path this will add a voltage error to measurements of V_{DS}. A standard ground clip is 140mm long (140nH) while a sprung ground clip is 10mm long (10nH). Probe input capacitance, C_{probe} is 12 pF, and CS448 ground capacitance, C_{ground} is 14pF. L_S might vary 3 - 10nH. Based on these values these bad things happen:



1. **The measured signal (eg 15V gate drive) initiates ringing between Lprobe common and C_{probe}.**



2. **The common signal VCM (eg 650V) initiates ringing between between L_{PC} and C_{ground}. This combines with (1). L_{PC} has an impedance of about X = 2 π F L = 2 π 32M 140n = 28 Ohm. C_{ground} has an impedance of X = 1/2 π F C = 1/(2 π 32 MHz 14p) = 355 ohm, so the voltage generated across L_{PC} is about 650 x 28/355 = 51V, 3x bigger than the 15V being measured! Even with a spring ground clip of 10nH (X = 2 ohm), you will see 650 x 2/355 = 3.6V added signal.**

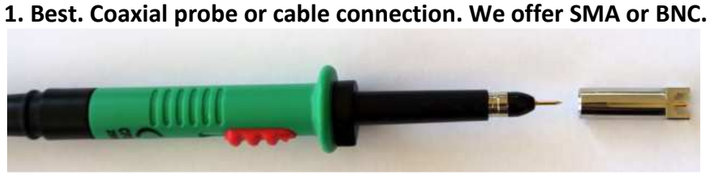


3. **If measuring V_{DS} saturated (say 0.4V) with 10A, L_S = 10nH, V = Ldi/dt = 10n 10/10n = 10V. The inductive voltage totally dominates the V_{DS}.**

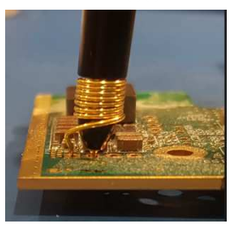
Low inductance four wire connections

This connection method uses four wire connections to avoid measuring L_S, and low inductance connection methods. Coaxial is best. See the next page. Connection methods are:

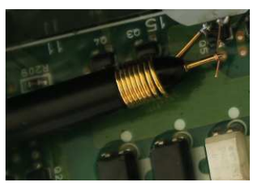
1. Best. Coaxial probe or cable connection. We offer SMA or BNC.

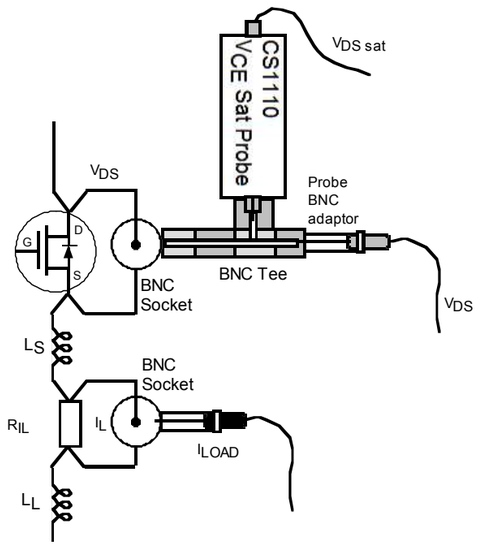


2. OK. Spring ground clip and probe inserted into two vias.



3. Worse. Soldered spring ground clip and soldered wire wrapped around probe tip.





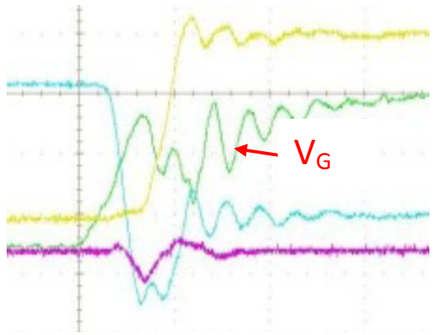
Differential Probe Common Mode Rejection Ratio (CMRR)

You could use a differential probe. The Common Mode Rejection Ratio (CMRR) figure tells you how well the probe rejects common mode slew. Here are CMRR values for PMK Bumble Bee and Tektronix P205A probes, from their data sheets:

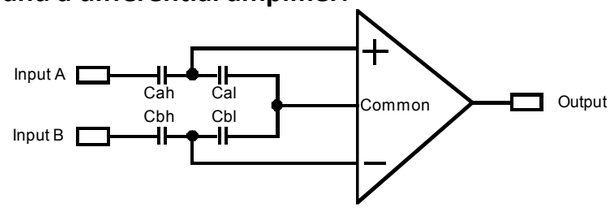
PMK Bumble Bee CMRR		Tektronix P205A CMRR
DC	*> 80 dB*	DC: >80 dB
100 kHz	*> 70 dB*	100 kHz: >60 dB
1 MHz	*> 62 dB*	3.2 MHz: >40 dB
3.2 MHz	*> 50 dB*	50 MHz: >30 dB

Let's say 40 dB for 32 MHz, or 1 part in 100. So with the 650V swing, we will see 6.5V of added spurious signal.

It looks something like this:



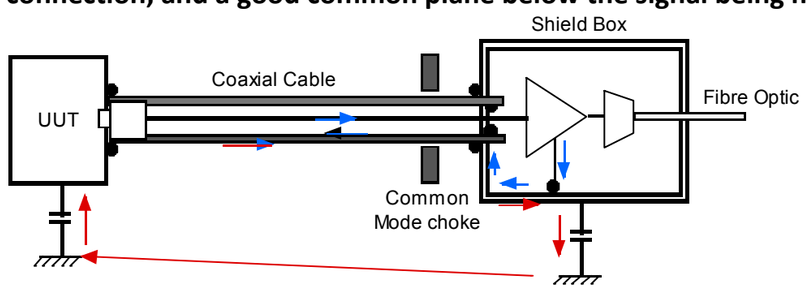
Why so bad? A Diff Probe uses two capacitive dividers and a differential amplifier:



The capacitive divider for each leg is Cah-Cal and Cab - Cbl. The normal input capacitance for each leg is 4 pF. For a 50:1 divider (a common value), Cah will be about 4pF and Cal about 200 pF. The common mode rejection is set by the equality of the two dividers. If the difference between the two dividers is 1 part in 100, then the CMRR will be 40 db, or 20 log (100). For 100dB the match would have to be better than 1 part in 100,000. With Cah = 4pF, a match of better than 4/100,000 pF = 0.04 fF is needed. **This is not possible.**

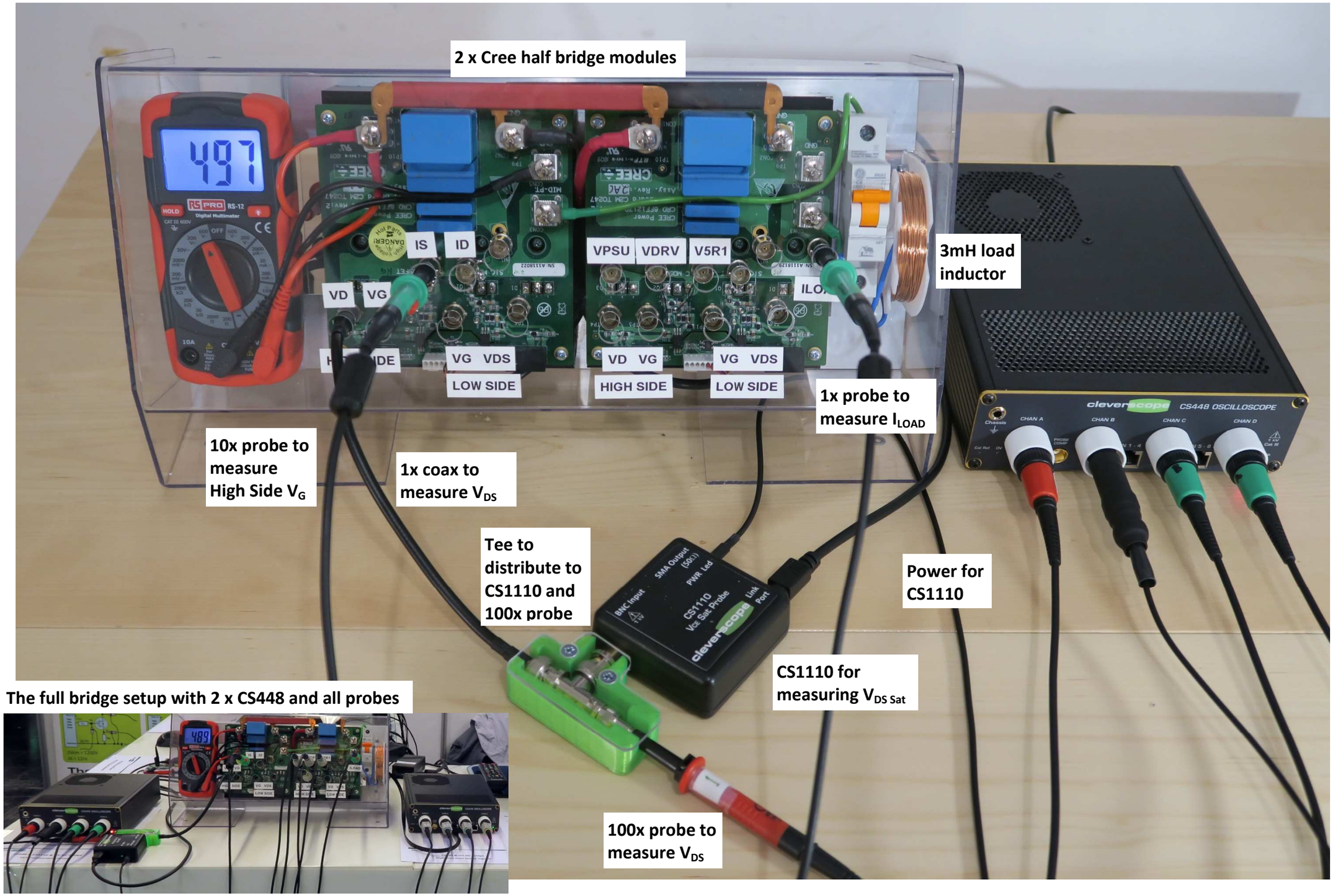
CS448 CMRR

The CS448 has a CMRR of 100 dB at 50 MHz (100,000:1). With the same 650V swing, and a 1x coax connection, you'll see about 7mV of common mode noise. For that, you'll need a coaxial connection, and a good common plane below the signal being measured.



The CS448 is single-ended, and relies on skin effect to separate the signal current (blue) from the common mode current (red). The signal current returns on the inside of the coax shield, while the common mode current flows on the outside of the shield, and returns via capacitive coupling to the UUT. This large loop has high inductance which can ring with the ground capacitance. Reduce the ring by using a common mode choke to increase the impedance to the common mode current, but not the signal current which sums to zero under the choke.

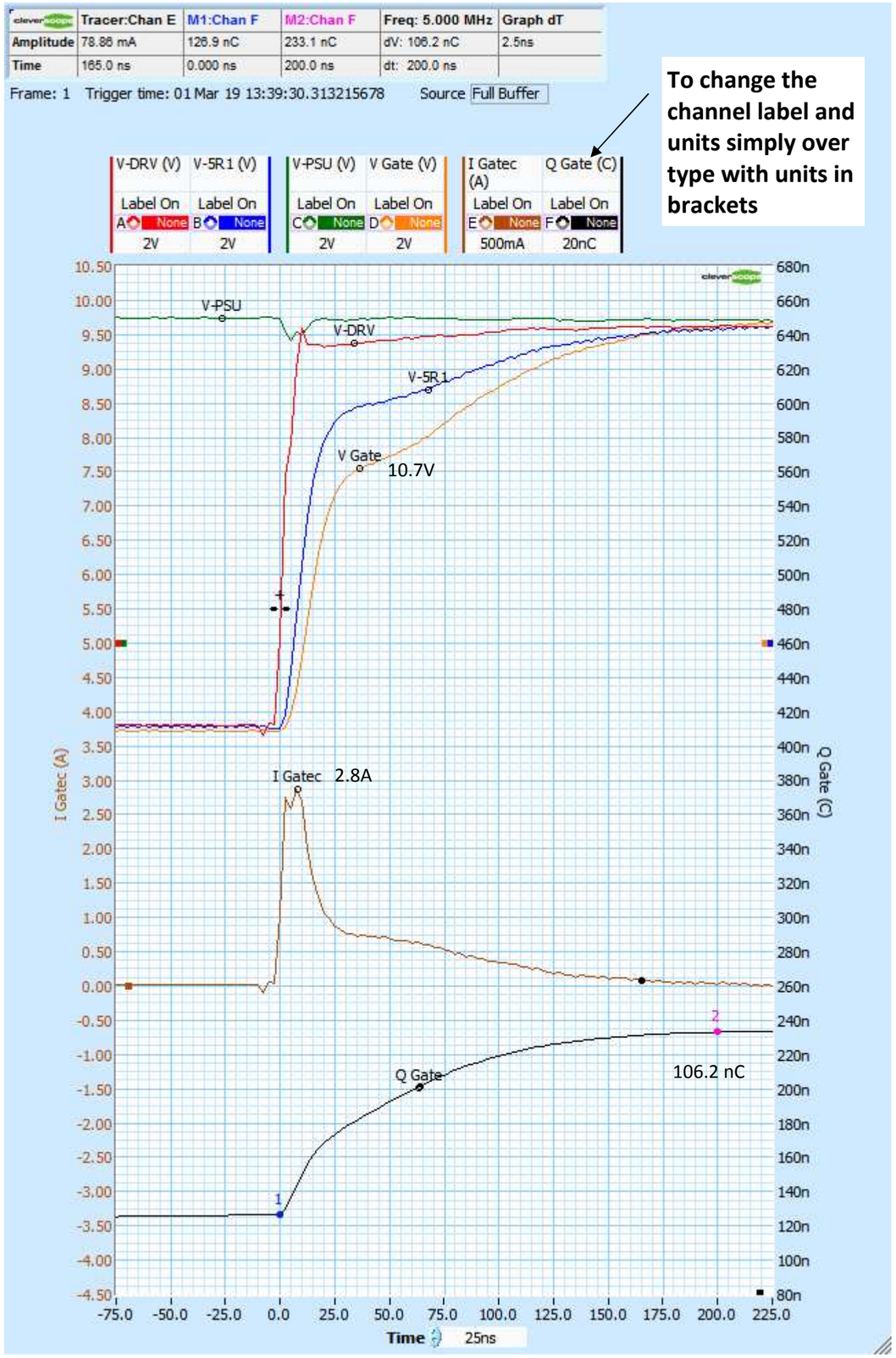
Measurement Setup



All connections are BNC coaxial

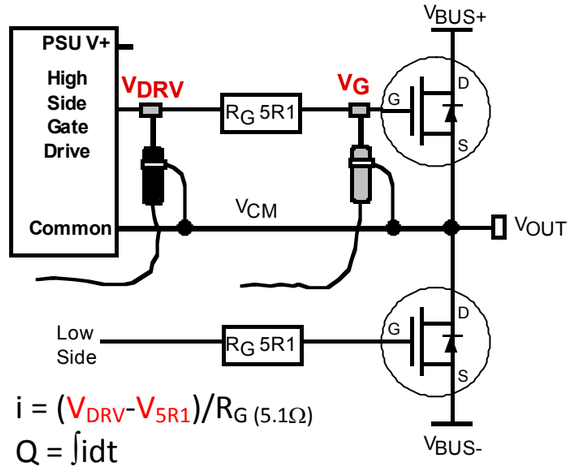
All measurements are on the high side.

The full bridge setup with 2 x CS448 and all probes



To change the channel label and units simply over type with units in brackets

High Side Gate Voltage and Gate Charge



$i = (V_{DRV}-V_{5R1})/R_{G\ (5.1\Omega)}$

$Q = \int i dt$

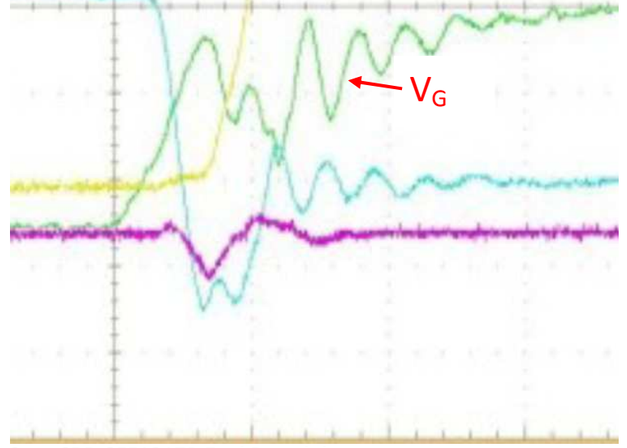
Important Note:
The reference common mode voltage (V_{CM}) is attached to and swinging with V_{OUT}. Very high common mode rejection is needed to make useful measurements of the high side. The CS448 has a CMRR of 100 dB at 50 MHz, meaning it can make clean measurements on a working system.

Measurements

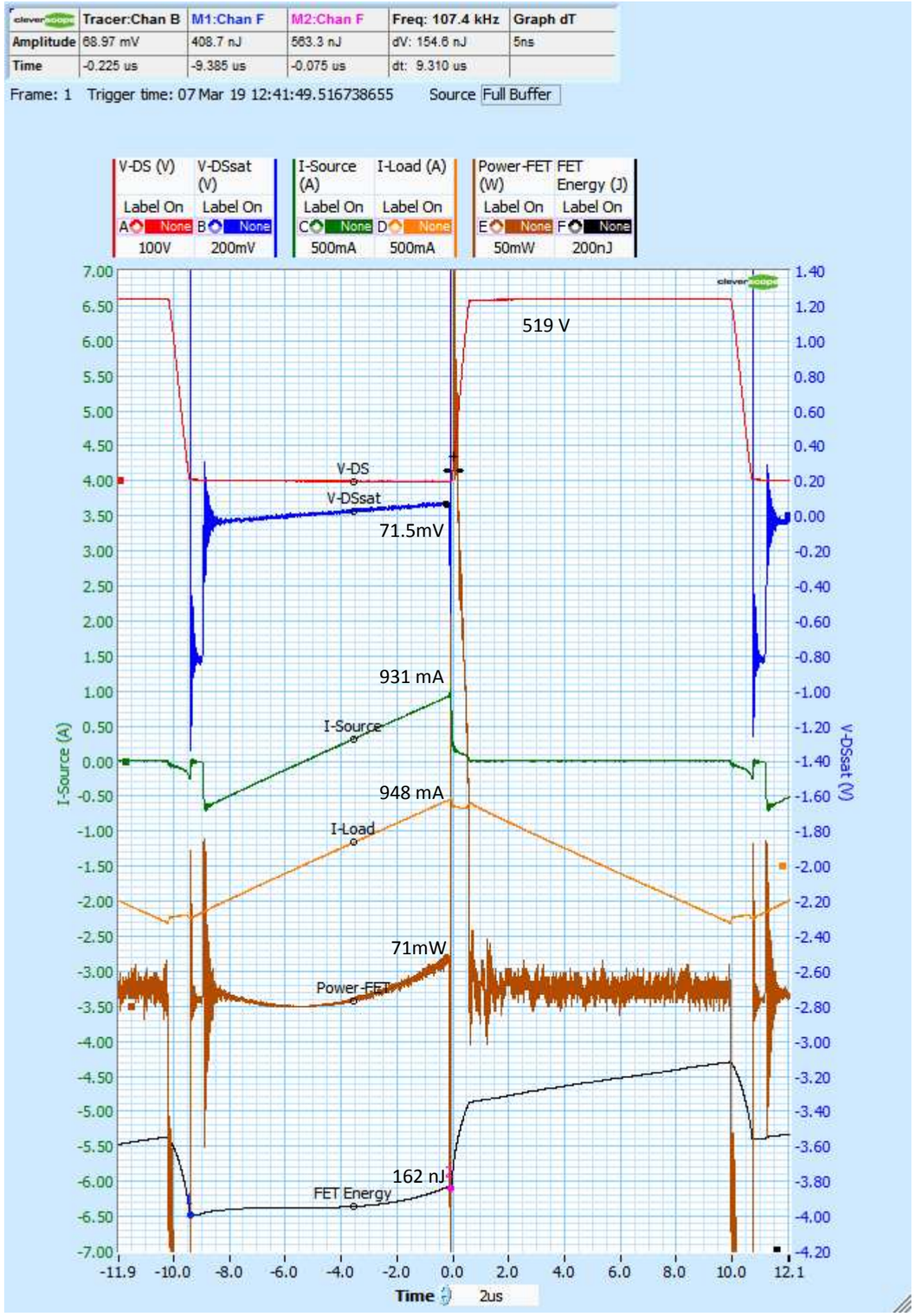
1. V_G has a Miller plateau of about 10.7V The device is fully on at completion of the Miller plateau.
2. Gate current peaks at 2.8A
3. Total Gate charge is 106.2nC
4. Rise time to the Miller plateau is about 45ns, even though the Drive voltage rise time is around 2ns. The gate drive design has significant R and C induced delay.
5. V_{PSU} dips by 1.34V and recovers in 15ns. Current is 2.7A at the dip, so the power supply output impedance is about 0.5 Ohm.

These measurements are used to verify the design.

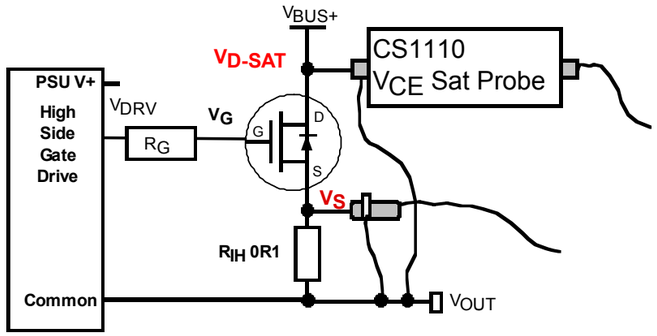
Comparison with the current state of the art from the Cree SicFET EVM Document: Gate Voltage with a Differential probe (green):



Cree CRD 8FF1217P Eval Board document :
T = 100ns/div, Green = High Side Vgs (10V/div), Yellow = Low side Vds (200V/div), Blue = Low side Id (7.6A/div), Pink = Low side Vgs (10V/div)



Conduction Power Loss



$i = V_S/R_{IH\ (0.1\Omega)}$ $V_{DS} = V_{D\text{-}SAT} - V_S$

$P = V_{DS}\ i$

$E = \int Pdt$

Measurements

The Maths display shows the derived values. Values are derived during the high side FET ON period.

1. **$V_{DS\ (saturated)}$ is derived from $V_{D\text{-}SAT} - V_S$ which uses the saturation probe to accurately measure the saturation voltage, which is increasing as the current increases. At the completion of the ON time, V_D is 71.5mV.**
2. **$V_{DS\ (Full)}$ is the voltage the FET is switching. It is 519V. Notice the VCE-SAT Probe is measuring the high side saturation voltage with a common measuring terminal that is swinging between 0 and 519V.**
3. **The FET Current, i, is derived from $V_S/R_{IH\ (0.1\Omega)}$ and peaks at 931mA with the load being used. It starts off negative, and change to positive as the current in the inductive load reverses. The FET series resistance is R = V/I = 0.0715/0.931 = 76.8 mOhm.**
4. **The FET instantaneous power is $P = V_{DS}\ i$. It peaks at 71mW.**
5. **The FET energy per switch cycle $E = \int Pdt$. We measure 162nJ. Assuming 50kHz operation, total energy loss is 50k x 162nJ = 18mJ/s. Average power is therefore 8.1 mW.**

These measurements are used to verify the design.

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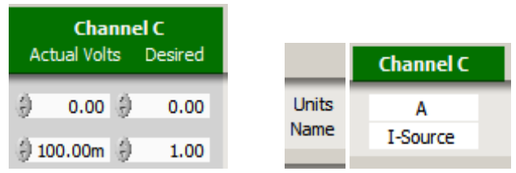
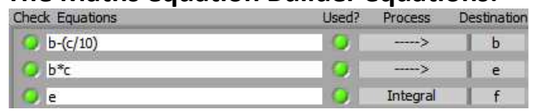
Scaling and Maths

Chan C has been scaled so 0.1V measured equals 1A (using the 0R1 current sense resistor), and named I-Source with units of A.



The Maths equation Builder equations:

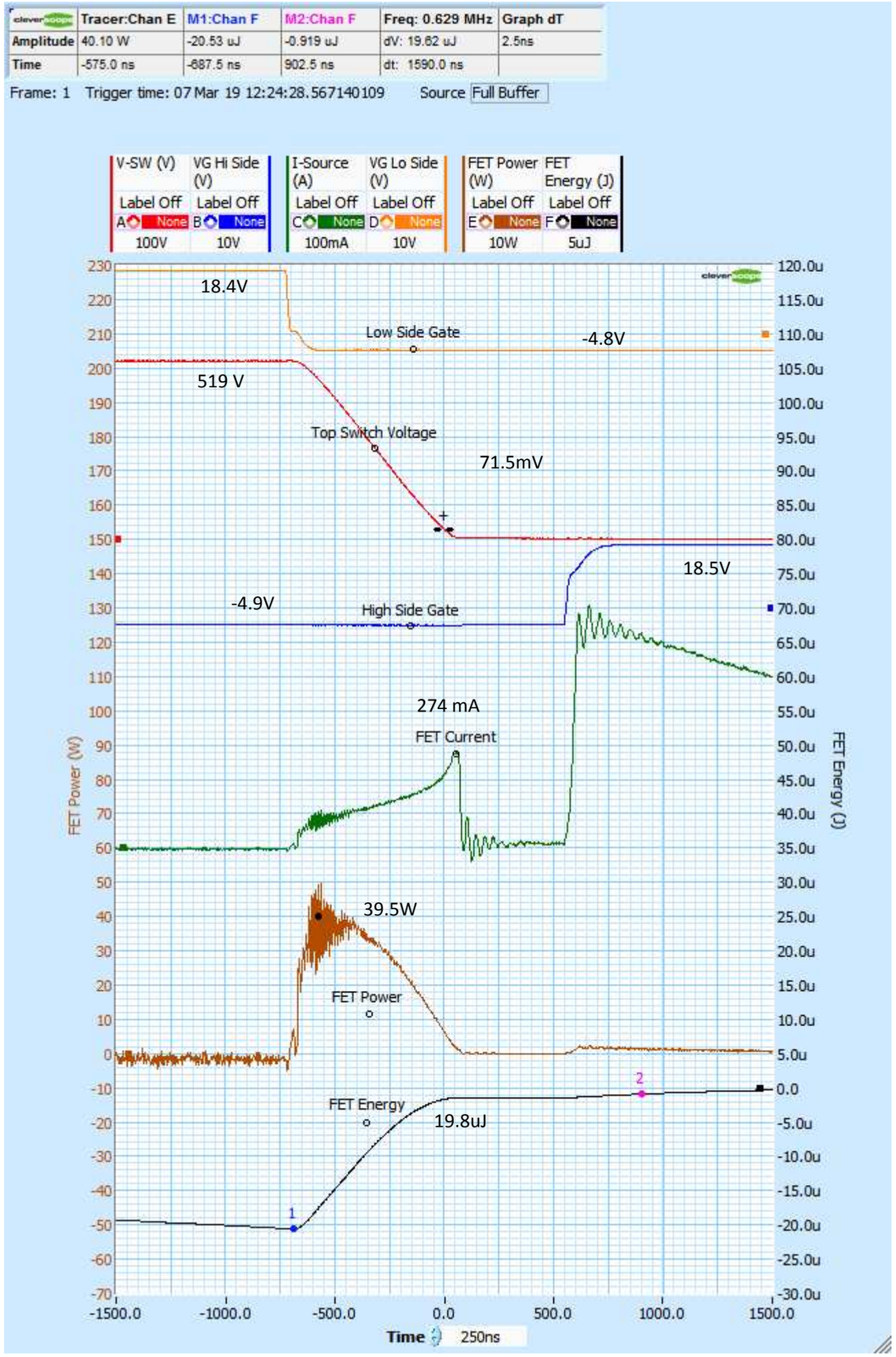


Chan B is $V_{D\text{-}SAT}$. Chan C is I_S and divided by 10 to get it back to volts. The first line calculates V_{DS}. The second line calculates $P = V_{DS}\ i$

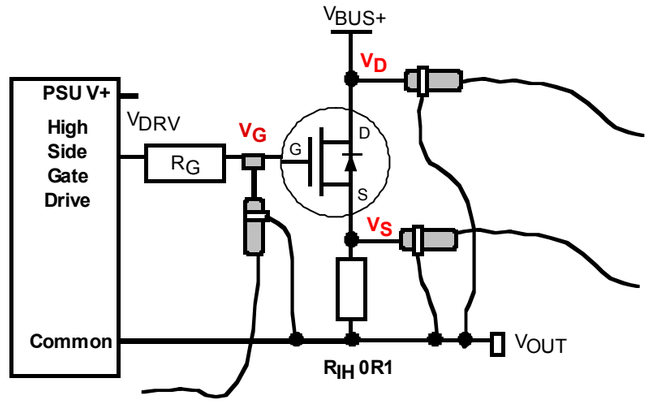
The third line calculates $E = \int Pdt$

$V_{CE\text{-}SAT}$ Probe

The VCE-SAT Probe is used to accurately measure low level voltages (-7 to + 5V) while ignoring input voltages above +5V (1000V maximum). It is isolated from the Link Port (used for power and control), and can be used to measure High Side V_{DS} during saturation.



Switching Power Loss



$i = V_S/R_{IH\ (0.1\Omega)}$ $V_{DS} = V_D - V_S$

$P = V_{DS}\ i$

$E = \int Pdt$

Measurements

The Maths display shows the derived values. Values are derived during the high side FET switch transition.

1. **V_{DS} is derived from V_D - V_S which uses a 100x probe to accurately measure the voltage VDSoss the FET, which is decreasing as the device turns on and the current increases. V_{DS} changes from 519V (FET off) to 71.5mV (FET on).**
2. **The FET/body diode current, i, is derived from $V_S/R_{IH\ (0.1\Omega)}$ and peaks at 274mA with the load being used.**
3. **The FET instantaneous power is $P = V_{DS}\ i$. It peaks at 39.5W.**
4. **The FET energy per switch cycle $E = \int Pdt$. We measure 19.8uJ. Assuming 50kHz operation, total energy loss is 50k x 19.8uJ = 0.99J/s. Average power is therefore 1W. The switch losses are much higher than the conduction losses.**

These measurements are used to verify the design.

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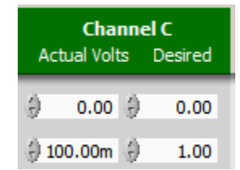
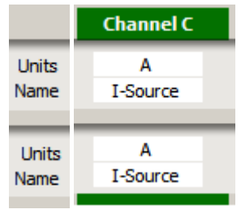
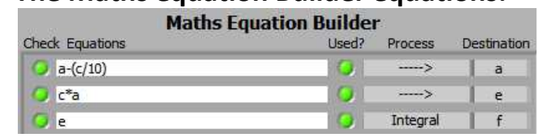
Scaling and Maths

Chan C has been scaled so 0.1V measured equals 1A (using the 0R1 current sense resistor), and named I-Source with units of A.





The Maths equation Builder equations:



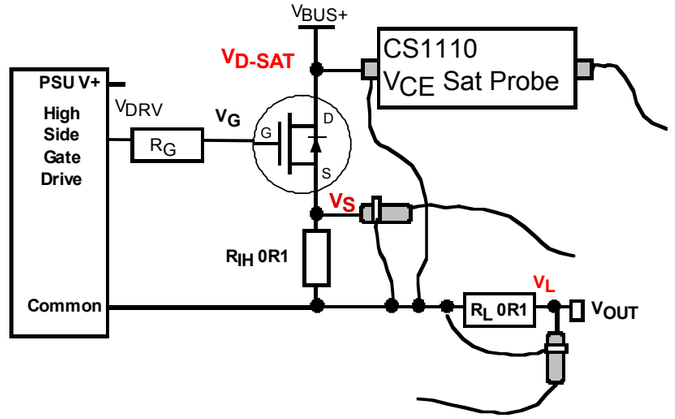
Chan A is V_D. Chan C is I_S and divided by 10 to get it back to volts. The first line calculates V_{DS}.
The second line calculates $P = V_{DS}\ i$
The third line calculates $E = \int Pdt$

Observations

The Switch loss is high because the inductor current flows to charge the parasitic capacitance in the reverse direction until FET V_{DS} reduces to 0. This current is flowing through the body diode (the FET is off), and starts reducing when the low side FET turns off, and during the dead time. We notice these things:

- **The high side FET voltage takes 700 ns to reduce to 0.**
- **The total dead time from low side gate turn off to high side gate turn on is 1277 ns.**
- **There is initial ringing of 24.9MHz. Further investigation could be used to find the circuit parasitics.**

Diode Power Loss



$V_{DS} = V_{D-SAT} - V_S$ $i_{FET} = V_{D-SAT}/R_{IH\ (0.1\Omega)}$

$I_{Diode} = V_L/R_{L\ (0.1\Omega)}$

$P_{Diode} = V_{DS}\ i_{Diode}$

$E = \int Pdt$

Measurements

The Maths display shows the derived values. Values are derived during the Diode forward on-time which occurs after the low side transistor has turned off and we are in the dead time after the Hi Side V_{DS} has fallen to zero.

1. **$V_{DS\ (saturated)}$ is derived from $V_{D-SAT} - V_S$ which uses the saturation probe to accurately measure the diode forward voltage while free-wheeling current flows through it in the dead time. The Diode forward voltage is about 847mV.**
2. **The free-wheeling current, $I_{Diode} = V_L/R_L\ (0.1\Omega)$, is measured by R_L as it goes to the load.**
3. **The Power dissipated in the diode is therefore $P_{Diode} = V_{DS}\ i_{Diode}$ Instantaneous power is about 0.53W.**
4. **The Energy dissipated in the diode per switch cycle is the integral of the instantaneous power, $E = \int Pdt$. We measure 265nJ. With 50k transitions per second, this is 13mJ/s, or 13 mW.**

These measurements are used to verify the design.

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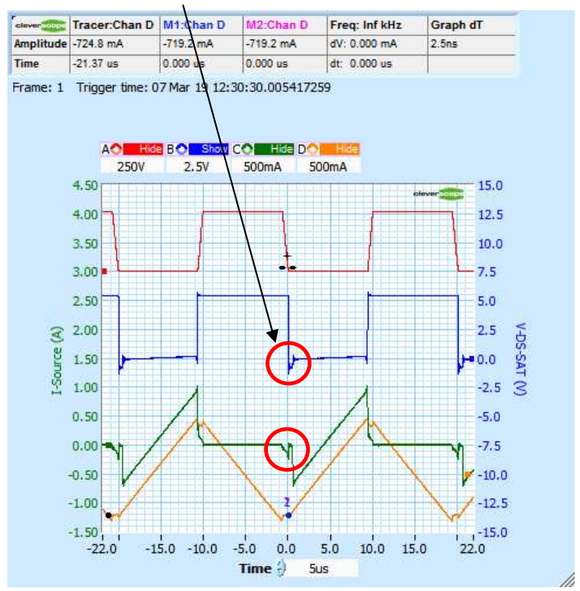
The point at which the Diode is on needs to be identified. This is the point at which the diode is forward biased at the end of the dead time.



Scaling and Maths

The channels measuring V_S and V_L have been scaled so 0.1V measured equals 1A.

The Maths equation Builder equations:

Maths Equation Builder

Check	Equations	Used?	Process	Destination
●	b-(c/10)	●	----->	b
●	b*d	●	----->	e
●	e	●	Integral	f

Chan B is V_{D-SAT}. Chan C is I_S and divided by 10 to get it back to volts. The first line calculates V_{DS}.

Chan D is i_{Diode}, and the second line calculates $P = VDS\ i_{Diode}$.

The third line calculates $E = \int Pdt$

CS448/CS328A Additional Capabilities

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Frequency Response Analysis

Easily analyse powered active or passive networks to meet design intent.

Passive component

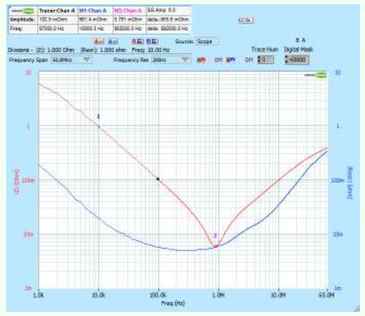
- RMS or Power response
- Gain/Phase
- Impedance / Phase, Q, Resr
- Inductance / Phase, Q, Resr
- Capacitance / Phase, DF, Resr

Powered Op Amp or Power Supply

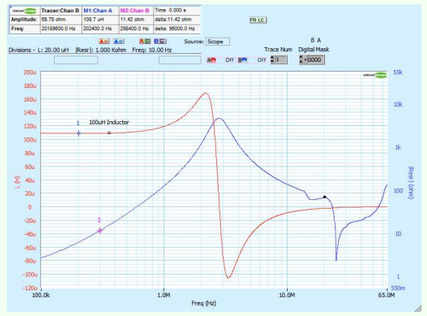
- Gain/Phase
- Input Impedance / Phase
- Output Impedance / Phase
- Power Supply Rejection Ratio

Live power supply Gain/Phase

Ceramic Capacitor Impedance



Power Inductor Inductance

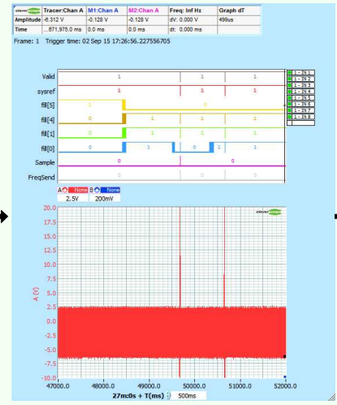


Streaming

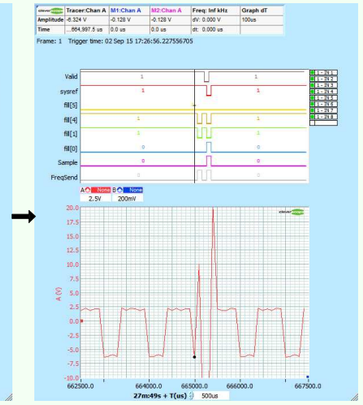
Easily save very long captures (secs to months) to disk with as fine as 200ns resolution, including 2ns peak capture. Find unexpected features, zoom in quickly to investigate.

Unexpected glitch during buffered clock system generation, happened after 1668 seconds.

See there are actually two glitches!



See the glitch happens with an unexpected load sequence.



Standard Capabilities

- Symbolic Maths with live Matlab link (with 10 lines of equations).
- Spectrum Analyser with settable Bandwidth and Resolution
- Protocol Decoding
- Signal Information Display with 47 functions and logging to Excel
- Tracking display for very fast examination of fine detail
- Mixed Signal triggering with dual triggers including counting and period

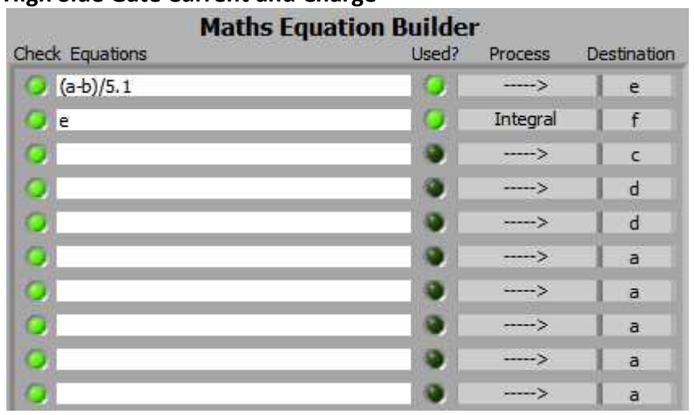
Bart Schroder
Ken Henderson

www.cleverscope.com

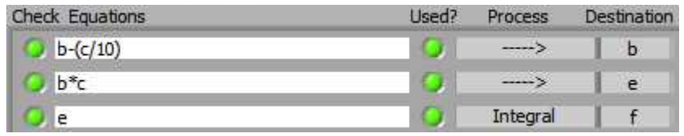
Maths Equation Builder Equations

The CS448 application uses the Maths Equation Builder to derive plots for Power, Energy, Current etc. You can have up to 10 maths equations, including symbolic, conditional and function components.

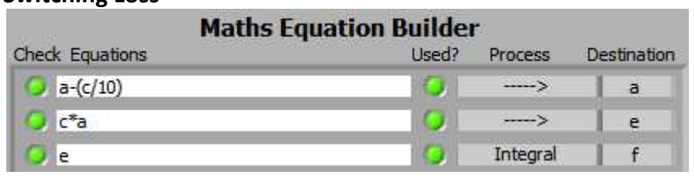
1. **High Side Gate Current and Charge**



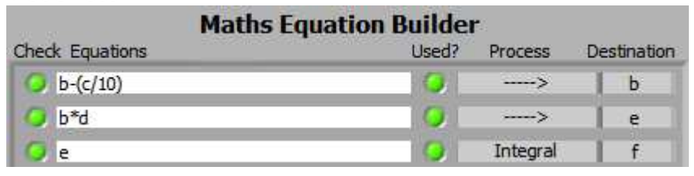
2. **Conduction Power Loss**



3. **Switching Loss**

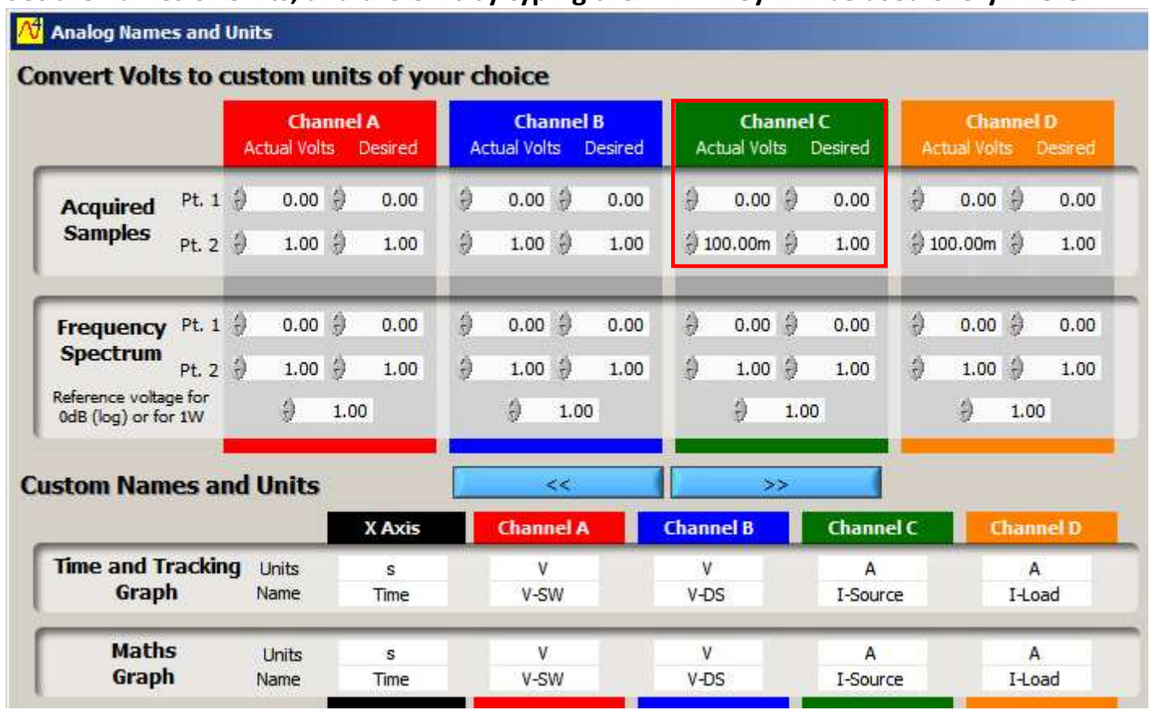


4. **Diode Loss**



Unit names and scaling

Scale input signals simply by specifying the input value, and the desired output value. Set the names of Units, and the Unit by typing them in. They will be used everywhere.



CS448 Application

Notice these features:

1. **Axes are labeled with the signal name, and are in useful units, and include grid lines with numeric values.**
2. **Derived values such as current and charge are easily generated with the maths equation builder.**
3. **The graph can be annotated for ease of understanding.**
4. **Markers are used for measurements.**
5. **Inserting the graph into a document is simply Ctrl C + Ctrl V.**