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# Using the CS1090 500V Bridge

**IMPORTANT**: The CS1090 generates lethal voltages. Do not touch any cables or metal during operation.

## Summary

The CS1090 is used to demonstrate the CS448 in use. The CS1090 includes two half bridges with BNC connections to several interesting circuit nodes including the upper and lower gate drives, the two half bridge switched nodes, and an across-bridge connection.



The Power switch is used to turn on the 19V power source. Up is OFF.

A CS448 black digital RJ45 cable can be plugged into the CS1090 and into the oscilloscope to display the gate drive control signals.

When the internal power supply is greater than 30V the HV Led indicator is on.

The Link port uses a Mini Din 8 plug and USB adaptor to the PC for control. The installation for the USB driver and control program is detailed in a later section.

The two half bridges are labelled 1 and 2 respectively. The SW sockets switch between 0V and 500V with a rise time of about 7ns. SW 1-2 is between the two switching nodes, and switches  $\pm 500V$ .

The G1 and G2 sockets are the Gate Drives, l = low side and h = high side. I1h probes the high transistor switch current, and I1l probes the low side transistor switch current. D1l and D2h probes the Driver chip. A series resistor of 10 Ohm limits current. The Gate current is (D1h-G1h)/10. From this gate charge can be calculated.

### **Connector and Transistor Schematic**

The BNC sockets connect as shown:



The CS1090 uses Diodes Inc DGD2304 half bridge drivers with typical 290mA high current and 600 mA low current capability to drive Infineon IPD60R3K3C6 FET switches (650V, 4A,  $3.3\Omega$  R<sub>DSon max</sub>, 4.6nC gate charge).

## Installation

Important: Install the device drivers before plugging in the USB Serial Link Cable.

Extract the contents of the CS1090.zip to a folder. The result will contains these files:



Open the CS1090 Serial Port Installer folder:



Determine if your operating system is 32 bit or 64 bit. Most modern operating systems are 64 bit. Start CP210xVCPInstaller\_x64.exe if 64 bit, or CP210xVCPInstaller\_x86.exe if 32 bit. Allow the installer to complete.



Plug the USB Serial Link cable into the Link Port. The cable has a Min Din 8 plug at one end, and a blue USB plug at the other. Plug the USB into a PC USB port. You should see a driver being loaded the first time you do this.

Using the Ada Fruit 954 USB-Serial adaptor the Mini-Din 8 connections are:

Wire	Function	Mini Din
Red	+5V , not	
	used	
Black	0V	Pin 2
White	Rx into	Pin 6
	USB	
Green	Tx out of	Pin 7
	USB	

Make sure the CS448 application is installed, as it provides the run time the CS1090 application relies on.





The Serial Error led should not be lit. Only the serial ports available will be displayed, but we have taken a guess as the Serial Port to use. If you find that the CS1090 does not communicate with the application, see the note on changing the serial port, later.

Make sure the power switch on the CS1090 is up (off). Make sure no probes are plugged in. Plug the 19V power into CS1090, and then turn on the Power Switch. This should cause a message to be received in the Message received area:

1	Message received:										
	<b>A</b> 5	02	OF	0A	01	ЗF	D2	2E			
	Fi	cmwa	are:	: 1	10	Ve	csid	on:1		Checksum:3FD2	ok

If this happens all is good. If not, see the section on finding the right serial port.

# Using the CS1090

Turn off the CS1090 power switch and attach the BNC tip adaptors to one green 1x/10x probe and one red 100x probe. You will find the adaptors in the probe accessory bag:



Set the green probe to 10x, as shown. Wrap three turns of the probe cable near the plug end around an LF1290 common mode choke, which should have come with the CS448.

Make sure power switch is OFF (up) and no LEDs lit. Plug in the probes as below:



We will be probing Halfbridge 1 - SW1 (the switch) and G1h (the high side gate drive output). Plug the red probe into Chan A, and the green probe into Chan B in the CS448. Make sure the compensation screws are facing upwards for later adjusting. It's good to have the cables hanging in Air to minimize capacitance.

We will use the CS1090 to compensate the probes for flatness. Start the CS448 application. Load the file *CS1090 SW1 and G1h.apc* using File/Open. This will set up the CS448 correctly, or you can set up manually as for the graph below.



Now switch the power switch down on the CS1090.

**IMPORTANT**: Do not touch any metal or the cables as lethal voltages are present.

You should see the picture above. The Scope Graph shows the 50 kHz switch frequency, while the Tracking graph shows one positive switch transition with the High Side Gate drive turning on. Note that the Gate Drive is transitioning between 0 and 500V, so be careful NOT to touch it.



On the CS1090 application, slide the Frequency slider down to 1 kHz. You should see the graph below. The A channel should be flat and the B channel gently sloping as the High Side power supply decays under load. There should be no change to the Tracking graph.



If the A channel is not flat, use the insulated double ended adjustment tool in the probe accessory bag to adjust it until it is flat. The lower part of each square wave should be 0V. Adjust the B channel for a sloping straight line (the power supply is sagging as the gate drive power supply capacitor decays). The reduction of

Gate Drive voltage seen in Chan B (blue) Gate Drive is due to the Miller (Reverse Transfer) Capacitance pulling charge out of the gate as the voltage rises.

### Experimentation

Vary the Output Voltage and notice that there is very little effect on the Gate drive waveform. Do the same with Frequency.

Turn on Signal Information (View/Signal Information) and select *Pulse* under *Time Info*, and set the Information source to *Tracker*. Note the Chan A (500V) rise time is about 7ns.

Signal Inform	[	Show Logging				
Function	Chan A	Chan B	Chan C	Chan D		
0 -> 1 Time	6.860 ns	50.17 ns	31.59 ns	28.96 ns		
1 -> 0 Time	0.000 s	0.000 s	0.000 s	0.000 s		
V '1'	507.6 V	13.94 V	6.419 mV	37.53 mV		
V '0'	2.810 V	123.0 mV	-2.705 mV	-18.50 mV		
V swing	504.8 V	13.82 V	9.125 mV	56.03 mV		
Overshoot	2.524 V	69.78 mV	1.141 mV	13.83 mV		
Slew rate						
Pulse Period						
Pulse Frequency						
Pulse Length	0.000 s	0.000 s	0.000 s	0.000 s		
Duty Cyde						
Do Average Time Info Information Source						
Send DD	E	Pulse	<b>▽ T</b> r	acker 🗸		

Zoom the tracking graph out so you see both edges. Make the display a bit wider so you maintain the 2.5ns graph dT:

												Show Logging
								Function	Chan A	Chan B	Chan C	Chan D
Amplitude 8.740 V	M1:Chan A 1.119 V	508.2 V	dV: 505.1 V	2 Graph dT 2.5ns				0 -> 1 Time	7.454 ns	18.36 ns	25.69 ns	25.93 ns
Fime -8.245 us Frame: 2 Trigger time: 1	-0.076 us 9 Apr 18 17:3	0.083 us 2:56.62033259	dt: 0.159 us 10					1 -> 0 Time	7.259 ns	52.85 ns	43.97 ns	35.48 ns
			lana					V '1'	2.465 V	75.73 mV	-3.995 mV	-25.67 mV
100V	2V	5V	5V				- 16.0	V '0'	521.5 V	14.19 V	2.802 mV	17.81 mV
1500	1					clever	14.0	V swing	-519.0 V	-14.11 V	-6.797 mV	-43.48 mV
1400							12.0	Overshoot	2.595 V	73.49 mV	4.758 mV	30.44 mV
1300							8.0	Slew rate	-55.71 kV/us	-615.0 V/us		-1.342 V/us
1100							■ 6.0 4.0	Pulse Period	20.06 us	20.06 us		20.06 us
900 § 800 	L			•		L	2.0 ■0.0 Ω -2.0 西	Pulse Frequency	49.84 kHz	49.84 kHz		49.84 kHz
500							-4.0 S	Pulse Length	9.977 us	11.22 us	9.980 us	9.975 us
300							-8.0	Duty Cyde	50.27 %	44.07 %		50.29 %
200							-12.0					
100 0 • -100		•		<u>1</u> -			-14.0 -16.0 -18.0	Do Averag	e 🗌	Time Info	D Infor	mation Source
-200 -14.0 -12.	D -10.0 +	8.0 -6.0	-4.0 -2.0 Time	0.0 2.0 ) 2us	4.0 6.0 8.0	0 10.0 12.0	-20.0 14.0	Send DD	E	Pulse		acker 🗸

We can see the 500V Chan A signal is slewing at about 55 kV/us, with rise and fall times of around 7ns. The small pulses in Gate Drive plot caused by the Miller (Reverse Transfer) Capacitance injecting charge into the gate as Switch voltage falls.

#### Miller (Reverse Transfer) Capacitance discussion

Time 🕘

10ns

Zooming in on the High Side Gate Voltage we see a drop in the voltage as the upper transistor turns on:

verscope	Tracer:Chan A	M1:Chan A	M2:Chan A	Freq: 100.00 MH	Graph dT			
plitude	5.324 V	40.25 V	507.4 V	dV: 467.1 V	2.5ns			
ne	-15.00 ns	0.000 ns	10.00 ns	dt: 10.00 ns				
ame: 2	Trigger time: 2	0 Apr 18 15:2	3:44.21967000	6				
	AO Non			None				
	100V	2V	10V 1	.0V				
	900					14	1.0	
	000							Drain (D)
	800		$\wedge$			14	2.0	·
	700		1 1 1				).0	
	600			$\Gamma$			0	gd T
				7			Ŭ.	Gate (G)
S	500		1 .	*~		6.	0 ഇ	c i
1	400 -					4.	이 문	gs T
itd			1 1 1					
Ś	300		1 11			2.	0 5	6
	200		/ //			• 0.	0	Source (S)
	100		/					
	100		1 <u>1</u>			-2	.0	input capacitance $(C_{iss}) = C_{gd} + C_{gs}$
	0					-4	.0	Output capacitance $(C_{oss}) = C_{ds} + C$
	-100						0	Reverse transfer capacitance (C <sub>rss</sub> ) =
	-100					1	.0	

As the gate common mode voltage is rapidly rising, the Reverse Transfer (Miller) Capacitance transfers charge from the gate to the negative bus via the uncharged output capacitance (Cds+ Cgd in the equivalent FET diagram), reducing the gate drive voltage. For this reason the Gate Driver needs to be low impedance. We see a drop of about 4V. The typical max DGD2304 gate drive high output current is 290mA.

Similarly the Reverse Transfer Capacitance injects charge from thefully charged Output Capacitance into the gate as the lower transistor turns on, which can start to turn on the FET if there is too much charge injected. The CS448 is a good tool to check for this and verify the gate drive design. We see about 1.7V. The DGD2304 is capable of 600 mA low output current, and this is why the low going injected value is about half as big.



#### Using an Inductor to slow the slew rate, and draw some current

We fitted a 9mH inductor (the Self Resonant Frequency needs to be > 150 kHz at 100mA, I used the FRA to prove the inductor value and SRF - see later section) between the SW1 and SW2 nodes. We measured both SW1 and SW2, and the current in the inductor using I1-2 (a 0.1 ohm resistor in the SW1-2 path). Note that the I1-2 common mode voltage will swing between -Vbus to + Vbus. DO NOT TOUCH IT. We also checked out the high side gate drive on SW1, which swings between 0V and Vbus.

Here we used a Vbus of 150V (the voltage is reduced to limit the inductor current to 100mA peak - the maximum the CS1090 power supply can handle):



Observations:

- The SW1-2 current is ramping linearly up and down as the switches change state. The peak current is about ± 100mA. (As a side not, we can use the Markers to measure the current slope, see Markers 1 and 2, from V = Ldi/dt, di = 135.3mA, dt = 7.2us, V = 154V, so L = 154x 7.2u/0.135 = 8.2mH, which is about right as the inductance reduces with frequency).
- The dead time is clearly visible between the Switch operations, and as reducing current in the current plot, caused by Inductor inter winding capacitance (a parasitic).
- The A and B channels are 20V/div, switching 154V, note the 0V markers on the amplitude axis.

Here is a zoom on the o	dead time	period:
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cleveracope	Tracer:Chan C	M1:Chan B	M2:Chan A	Freq: 0.911 MHz	Graph dT
Amplitude	-16.46 mA	153.3 V	152.5 V	dV: -0.833 V	2.5ns
Time	-705.0 ns	-1222.5 ns	-125.0 ns	dt: 1097.5 ns	

Frame: 2 Trigger time: 20 Apr 18 11:00:07.716662768



The dead time is about 1.1us, and during this time the inductor voltage changes linearly as set by the inductor. Current is increasing and then reducing in the inductor.



We see three things: 1. The current in the dead time is reducing. Simulation shows this to be caused by the inductor inter-winding capacitance short circuiting the inductor current.

2. The switch Voltage rise is now set by V=Ldi/dt, and takes the full 1.1us.

3. Because the slew rate is so much slower we do not see Miller capacitance induced reduction in the gate voltage.

#### Measuring Gate Charge

We can measure the gate charge by probing both G1h (Chan D) which probes the high side gate, and D1h (Chan C) which probes the high side driver. A 10 ohm gate drive resistor is used. We can use the Maths equation builder to calculate the gate current, and the gate charge, form  $Q = \int it$ .

Maths equation	ı builder		<u> </u>
	Maths Equation Builder	· Clear C	Cache Help
Check Equations	Used?	Process	Destination
🔾 (c-d)/10		>	а
🥥 a	Q	Integral	b

Which results in this Maths Graph, annotations describe the plots:



The gate charge is 4.8nC (M2-M1). The data sheet for the IPD60R3K3C6 transistor says 4.6nC, which is not far off. The integral applies from the start of the captured signal. So to find the gate charge for a discrete period of time we have used the Markers to find the difference over that period of time.

Notice also that the DGD2304 is operating at maximum current (309 mA), and has a voltage drop of 15-7 = 8V (the green curve), indicating that the DGD2304 high transistor has an effective on resistance of about 8/0.309 = 25.9 ohms. It will be about half that for the low transistor, as it can sink 600mA.

### Verifying the 9mH Inductor

We used the CS448 FRA module to measure the inductor, to ensure the inductance value, and sufficiently high SRF.



The inductor is about 9mH, but falls off with frequency (as we determined earlier), and the SRF is about 150 kHz, which is about the third harmonic. The inductor is capacitive after this, which explains the losses in the dead time.

## Finding the right serial port

If the CS1090 is not responsive to the CS1090 control program, you may have the wrong serial port. Open Device Manager (Start/Control Panel/Device Manager), and expand Port (COM & LPT). Find the one for Silicon Labs CP210x, and change the serial port to that one. After that the CS1090 should communicate.

