exacq® Technologies

TN-006
Technical Note

Phase Locked Sampling with Exacq CM Boards

In many data acquisition applications, particularly those involving rotating machinery, it is desirable to sample signals synchronously to an external event rather than at absolute time intervals. In the case of rotating machinery, for example, a shaft encoder generates pulses at constant angular intervals. Synchronizing with these pulses allows samples to be taken at known shaft positions regardless of the rotational rate of the machine.

While it may be possible to use the shaft encoder output as an external sample clock or external trigger to the data acquisition system, these approaches have drawbacks. As a sample clock, the encoder may not have sufficient resolution to capture the required number of samples per revolution from all the desired sensors. As a trigger, the trigger-to-sample delay and trigger reset time must be considered.

A different approach with performance advantages is to use a phase locked loop (PLL) to synthesize a sample clock which is synchronous with the shaft encoder pulses. The PLL makes it possible to increase the shaft encoder resolution by synthesizing a multiple of the shaft encoder frequency.

By virtue of its unique architecture, the Exacq Technologies CM Series low cost data acquisition boards can implement such a PLL with no additional hardware, making them ideal for applications in motor/generator monitoring or in engine testing. As shown in Figure 1, Exacq's on-board DSP is the enabling technology.

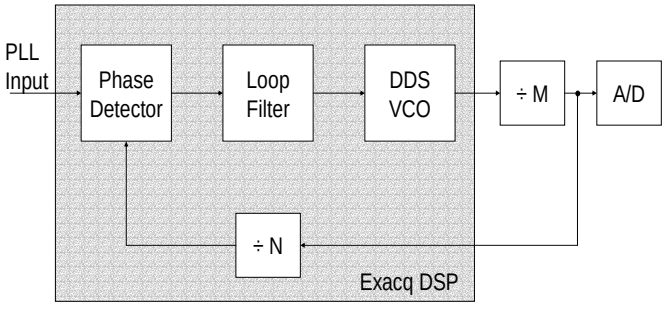

Figure 1 – PLL Architecture

A PLL is comprised of a phase detector, a loop filter, a voltage controlled oscillator (VCO), and an optional loop divider which is used for frequency multiplication. In the CM implementation, the phase detector, loop filter, and loop divider are implemented in DSP software. The phase detector counts the number of VCO clocks between PLL input pulses. The M-divider is automatically programmed, independently from the user programmed N-divider (which sets the number of A/D samples per input pulse), to keep the VCO frequency in the 3-40 MHz range. This high frequency ensures fine error resolution and low jitter. The loop filter is configured such that the PLL has a classic Type II, 2nd order response. This response is characterized in many references on the topic of PLLs, one of which is Motorola (Freescale) Semiconductor Application Note AN-535. Also in the DSP is a direct digital synthesizer (DDS) which is used to generate the A/D converter sampling clock. The nearly infinite frequency resolution of the DDS allows it to be used as the VCO in the PLL implementation.

Use of the PLL is straightforward via the Exacq data acquisition application programming interface (API). First, calling XDA_Ain_SetClock() with the maximum expected sample rate (i.e. maximum expected PLL input frequency times N, the number of samples per input pulse, times the number of channels to sample) sets the M-divider appropriately. Next, calling XDA_Ain_SetPll() programs the loop filter bandwidth and damping parameters, the N-divider, and starts the loop running. This call can be made such that it does not return until the loop is locked; then calling XDA_Ain_Start() begins sampling synchronous with the PLL input pulses. Throughout the capture, PLL error statistics can be read, as well as a flag which indicates whether the loop ever loses lock. As always, the software developers kit (SDK) which includes sample code to use the PLL is available simply by registering on the Exacq web site.

Two relevant applications have been simulated. The first is generator monitoring. The generator rotates at a nearly constant rate of 60 revolutions per second. Observation of voltage or current flow as a function of shaft position can provide information about the health and performance of the generator. In this scenario, the time required for the PLL to synchronize to the generator rotation is less important than achieving very low jitter in the angular position of the sampling instants.

To create the figures below, the Exacq CM board was synchronized to a 60 Hz signal representative of a one pulse per revolution (PPR) shaft encoder on a generator. By setting the PLL N-divider to 360, the one PPR signal was multiplied 360 times to yield a sample clock running at one sample per degree of revolution. To minimize jitter, the loop bandwidth was set fairly low. Figure 2 shows the time required for the PLL to lock, which follows the expected Type II, 2nd order behavior.

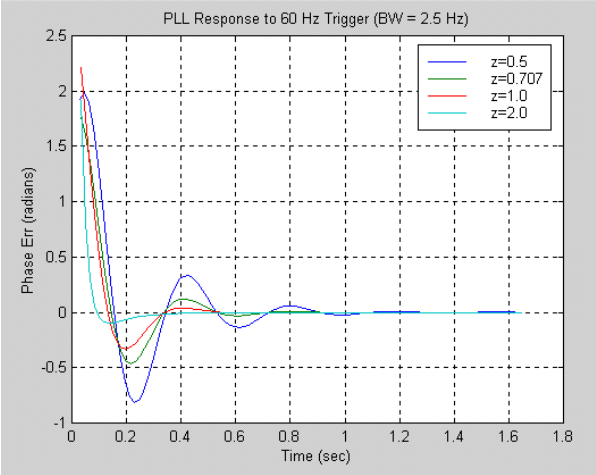

Figure 2 – PLL Locking Transient

Figure 3 shows the steady state error with various tracking bandwidths and two 60 Hz sources, one with negligible jitter and one with 5 us p-p jitter. At 60 Hz, this corresponds to 0.1 degrees p-p jitter, or frequency variation from 59.99 – 60.01 Hz. Clearly, the jitter introduced by the PLL is compared to the source jitter.

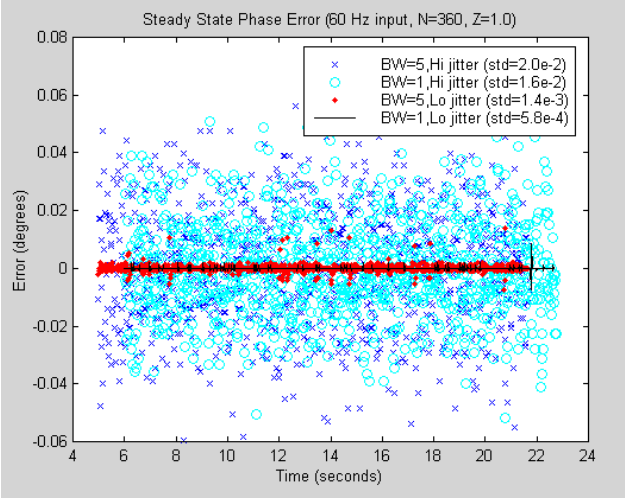

Figure 3 – PLL Narrowband Steady State Jitter

The second case is an engine testing scenario. The engine speed is much more dynamic than that of a generator, with RPMs varying from hundreds to several thousand in the course of a second. The ability of the PLL to track the dynamic signal while minimizing jitter is critical.

The Exacq CM board was synchronized to a signal varying from 6kHz to 48kHz, representing a 720 pulse per revolution shaft encoder with the RPM profile shown in the top of Figure 4. The PLL was set to multiply the input pulse rate by four to yield four measurement channels each with 0.5 degree resolution. With a wide bandwidth setting, the PLL was able to track the encoder output through this profile. The measured error of the sampling clock with respect to shaft angle is shown in the bottom of Figure 4. Note the X-axes are different in the top and bottom plots, as the bottom plot shows error vs. sample number, and the sample rate is not constant with respect to the time axis of the top plot.

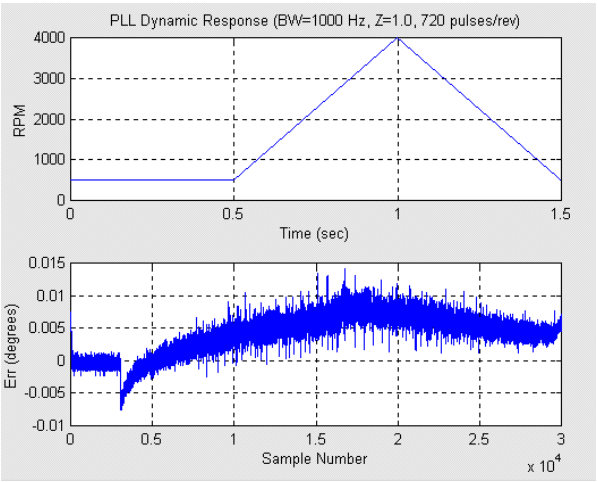

Figure 4 – PLL Dynamic Tracking Response

Figure 5 is similar, except the engine rate variation is smaller. Clearly, the lower rate of RPM change results in smaller tracking errors.

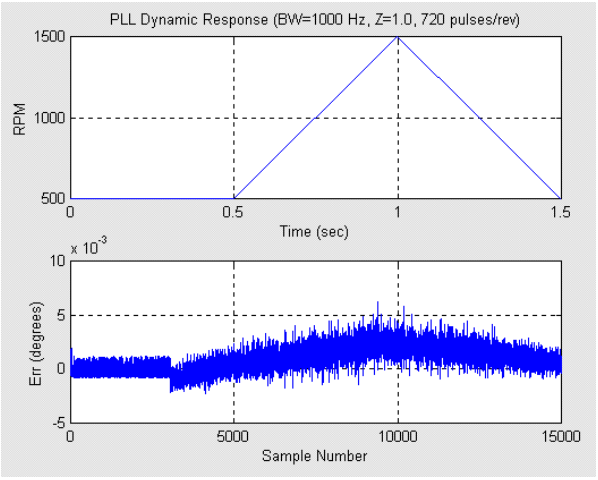

Figure 5 – PLL Dynamic Tracking Response

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