DSP Capabilities of Acquitek Data Acquisition Boards

DSP – A Digital Signal Processor (DSP) is at the heart of Acquitek data acquisition boards, as much for its hardware functionality as for its software utility. As shown in figure 1, the DSP provides simultaneous 80 MB/s input and output ports, 533 MB/s memory throughput via an integrated SDRAM controller, and a 132 MB/s bus mastering PCI interface. Additionally, not shown in the figure, it provides several Direct Digital Synthesizers (DDS) used to derive the input and output sample clocks, and hardware peripherals which control the input and output data flow with no processor intervention.

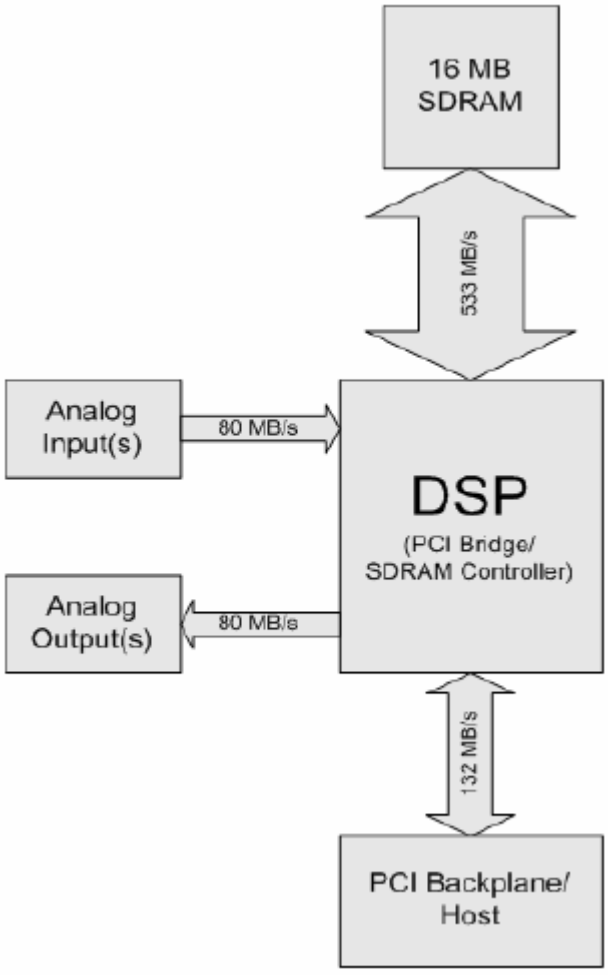

Figure 1 – Acquitek DSP Throughput

Signal Processing Software - The software executing on the DSP is designed to allow the data acquisition and data output functions to proceed smoothly whether the host computer operating system is paying attention or, as is likely the case, it is off monitoring some other task. However, the software required for this purpose utilizes only a fraction of the available DSP horsepower, even at sample rates of 20 MHz or more. As such, Acquitek engineers are adding signal processing features into the data acquisition Application Programming Interface (API). Presently, the available signal processing features are Fast Fourier Transforms (FFT) on the input data. The use of the FFT functions is described in detail starting on page 132 of the *Acquitek Data Acquisition SDK Manual*, but it can be as simple as adding the following lines of code to a data acquisition program:

```
XDA_Ain_SetParm(device, 0 , \
XDA_AIN_PARM_FFT_BLOCK_MODE, 1);

XDA_Ain_SetParm(device, 0 , \
XDA_AIN_PARM_FFT_SIZE, N);

XDA_Ain_SetParm(device, 0 , \
XDA_AIN_PARM_FFT_WINDOW_TYPE, \
FFT_WINDOW_TYPE_HANNING );
```

In an upcoming release of the Acquitek SDK, a similar method for implementing finite impulse response (FIR) and infinite impulse response (IIR) digital filters will be included.

Future – Beginning in spring 2004, development will commence to integrate these (and more) disparate, hard-coded signal processing functions into an integrated framework. A scripting language will enable more complex operations by chaining discrete functions together. An example is shown in figure 2.

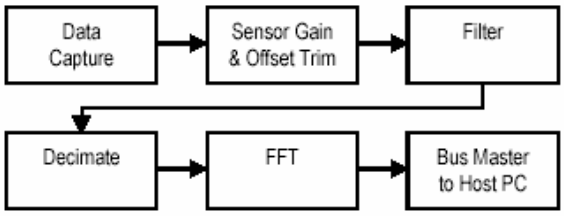

Figure 2 – Example DSP Process Flow

Additionally, next generation DSP hardware will dramatically increase the data throughput, enabling sample rates over 100 MS/s simultaneously for input and output. On-board memory capacity will increase by an order of magnitude, and signal processing horsepower will double with DSP clock rates to 300 MHz.

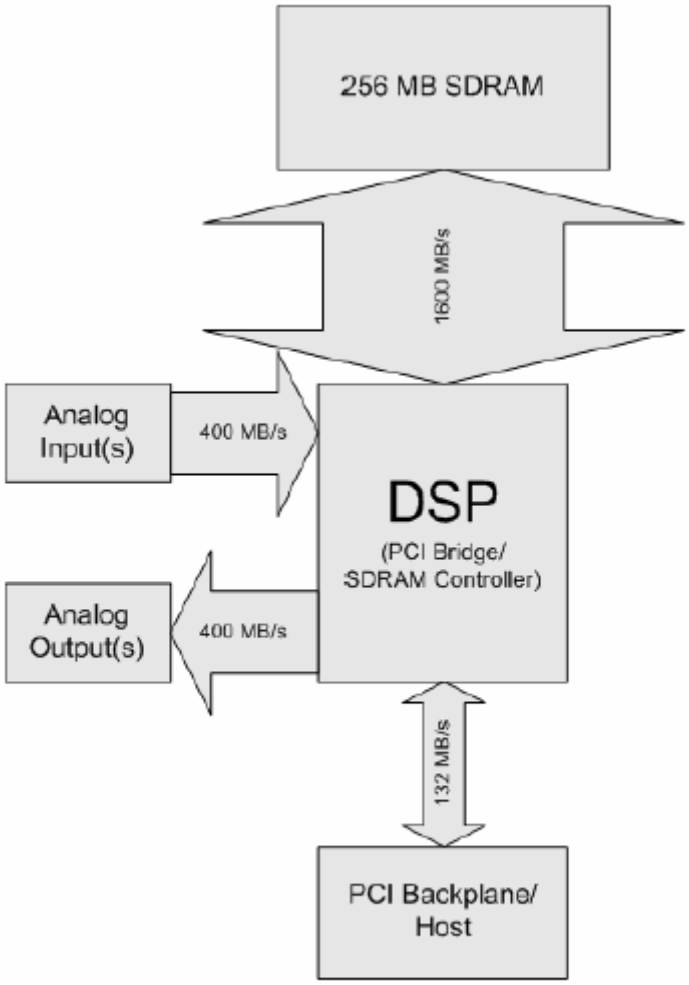

Figure 3 – Next Generation DSP Throughput