TN-002
Technical Note

Vector Network Analysis with an Integrated Analog I/O Board

Background – Despite the digital hype, the world around us still involves analog signals passing through analog circuits. In many applications, engineers must measure the analog effect a circuit has on the magnitude and phase of a signal passing through it. This is done with a vector network analyzer (VNA). For example, in digital communications such DSL, filters are used to suppress interference; but a filter with poor phase response can degrade performance by introducing intersymbol interference. In imaging ultrasound, careful alignment of transducers' phase enables well-focused pictures. In high speed networking, cables must induce little magnitude and phase distortion while carrying the signal.

Implementation - Typically, a VNA injects a sinusoidal signal into the test circuit, and analyzes the circuit's effect on the magnitude and phase of the input signal as the input frequency changes.

Acquitek CH and XH series of boards have several features which make them particularly attractive for VNA applications. Some of these features are highlighted in the system block diagram of Figure 1. What is not easily shown, however, is that all of these features are incorporated onto one single-slot PCI or PXI instrument:

Independent DDS-based input and output sample clocks – Both the output and input sample clocks are generated by direct digital synthesizers capable of 1 Hz resolution. With the large local memory bank, a glitchfree output sine wave can be generated at any desired frequency. On the input, a traditional FFT-based analyzer is constrained by its fixed sample frequency to resolution bandwidth bins that may not be appropriate for narrowband or high resolution analysis. By contrast, the CH/XH sample rate can be adjusted so that the test frequency falls directly in the center of the receive filter, which is a single point of the FFT spectrum computed with the oertzel algorithm. The resolution bandwidth may be varied separately from the number and center requency of the analysis points.

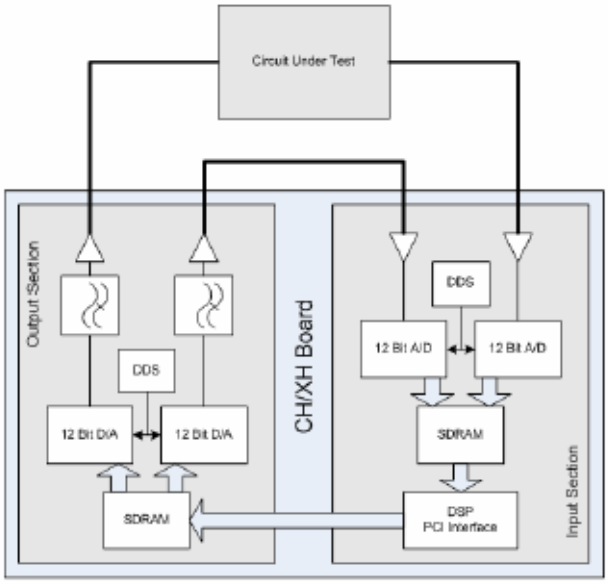

Figure 1 – CH/XH Block Diagram

Dual channel input and output – The second channel is used to loop output directly back to the input. This provides an accurate phase reference without the need for extensive calibration of the on-board analog output filters or synchronization of the independently clocked input and output.

High power driver and sensitive receiver – Dynamic range is maximized with a driver capable of supplying 24dBm into a 50 load and a receiver with -70dBm sensitivity over the Nyquist bandwidth at maximum gain. The resolution bandwith filtering at the test frequency can improve this sensitivity by 30dB or more.

Results – Several cases illustrating the outstanding performance of the CH/XH boards are shown below:

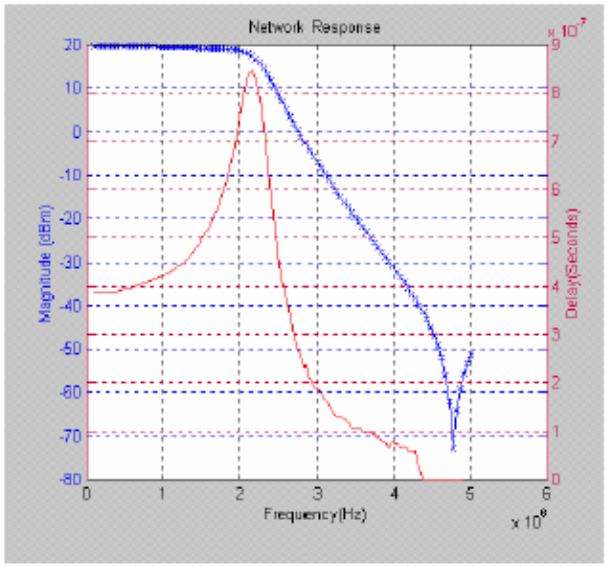

Figure 2 – 1.9 MHz Low Pass Filter

In Figure 2, a Mini-Circuits BLP-1.9 50 low pass filter is analyzed. Utilizing the high power output capability and variable gain on the input, over 90dB of dynamic range is realized with a 12 bit board. The significant group delay distortion across the filter passband is readily apparent.

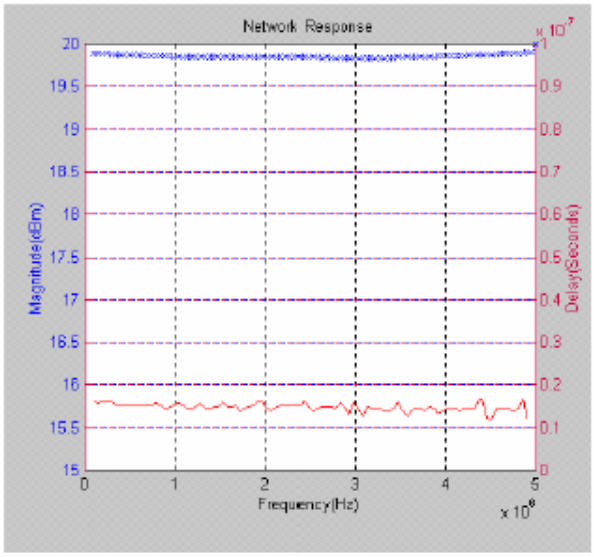

Figure 3 – Cable Length Test

In Figure 3, a three meter section of polyethylene dielectric cable is analyzed. With such dielectric, propagation velocity is 67%. The measured 15ns of flat group delay corresponds to three meters of cable. Phase resolution of well less than one degree is required for this measurement.

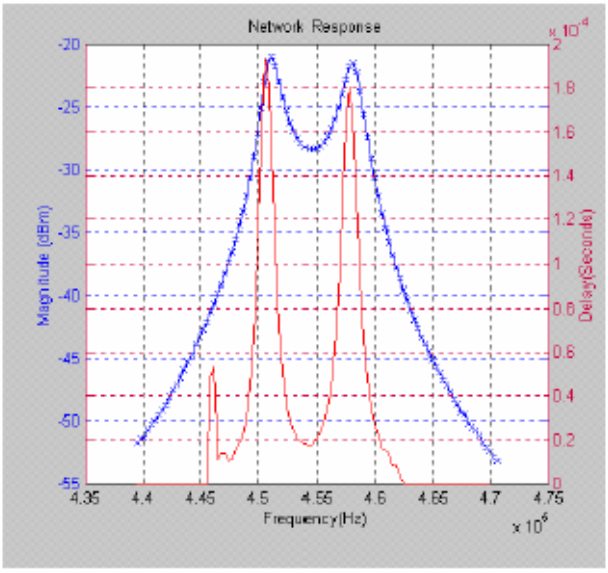

Figure 4 – 455 kHz Bandpass Filter

In Figure 4, a Toko AHCFM2-455EL ceramic filter intended for AM radio intermediate frequency filtering is analyzed. The plot clearly shows the 12 kHz bandwidth and 455 kHz center frequency, although there is substantial distortion since the filter's 2.5k input and output impedance were not matched to the board's 50 impedances.
The fine frequency resolution achieved with DDS-based input and output sample clocks is critical for narrowband analysis such as this.

Conclusion – The results shown in this Technical Note were generated using an Acquitek CH-3150 board with the Matlab MEX driver. This driver, as well as source code to the vector network analysis M-File, are included in the Acquitek Data Acquisition SDK